# DOUBLE DATA RATE (DDR) SDRAM

**MT46V32M8 – 8 MEG X 8 X 4 BANKS**
**MT46V16M16 – 4 MEG X 16 X 4 BANKS**

*For the latest data sheet revisions, please refer to the Micron Website: www.micron.com/dramds*

## Features

- 200 MHz Clock, 400 Mb/s/p data rate
- Low Latency DDR400B (3-3-3)
- $V_{DD}$ = +2.60V ±0.10V
- $V_{DD}Q$ = +2.60V ±0.10V
- Bidirectional data strobe (DQS) transmitted/ received with data, i.e., source-synchronous data capture
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data
- Programmable burst lengths: 2, 4, or 8
- Concurrent Auto Precharge option supported
- Auto Refresh and Self Refresh Modes
- $^{t}$RAS lockout ($^{t}$RAP = $^{t}$RCD)

| OPTIONS | Marking |
|---|---|
| • Configuration | |
| 32 Meg x 8 (8 Meg x 8 x 4 banks) | 32M8 |
| 16 Meg x 16 (4 Meg x 16 x 4 banks) | 16M16 |
| • Plastic Package | |
| 66-Pin TSOP (400mil with 0.65mm pin pitch) | TG |
| 66-Pin TSOP Lead-free (400mil with 0.65mm pin pitch) | P |
| • Timing - Cycle Time | |
| 5ns @ CL = 3(1) | -5B |
| • Self Refresh | |
| Standard | none |

NOTE:
1. Supports PC3200 modules with 3-3-3 timing

## General Description

The DDR400 SDRAM is a high-speed CMOS, dynamic random-access memory that operates at a frequency of 200 MHz (tCK=5ns) with a peak data transfer rate of 400Mb/s/p. DDR400 continues to use the JEDEC standard SSTL_2 interface and the 2*n*-prefetch architecture.

The base Micron 256Mb data sheet provides full specifications and functionality unless specified herein. This addendum data sheet concentrates on the critical parameters and key differences required to support the enhanced DDR400 speeds.

## Table 1: Configuration

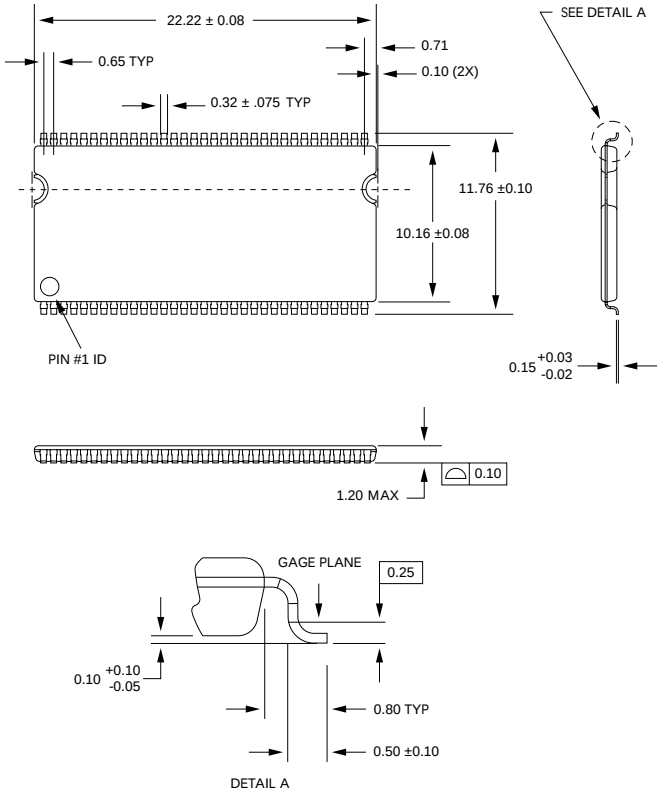
| ARCHITECTURE | 32 MEG X 8 | 16 MEG X 16 |
|---|---|---|
| Configuration | 8 Meg x 8 x 4 banks | 4 Meg x 16 x 4 banks |
| Refresh Count | 8K | 8K |
| Row Addressing | 8K (A0-A12) | 8K (A0-A12) |
| Bank Addressing | 4 (BA0, BA1) | 4 (BA0, BA1) |
| Column Addressing | 1K (A0-A9) | 512 (A0-A8) |

## Table 2: Key Timing Parameters

| SPEED GRADE | CLOCK RATE CL = 3[1] | DATA-OUT WINDOW[2] | ACCESS WINDOW | DQS-DQ SKEW |
|---|---|---|---|---|
| -5B | 200 MHz | 1.6ns | ±700ps | +400ps |

NOTE:
1. CL = CAS (Read) Latency
2. With a 50/50 clock duty cycle

## Figure 1: 66-pin TSOP Package Dimension




## Figure 2: 66-pin TSOP Package Pin Assignment

| x8 | x16 | | x16 | x8 |
|---|---|---|---|---|
| VDD | VDD | 1 • | VSS | VSS |
| DQ0 | DQ0 | 2 | DQ15 | DQ7 |
| VDDQ | VDDQ | 3 | VSSQ | VSSQ |
| NC | DQ1 | 4 | DQ14 | NC |
| DQ1 | DQ2 | 5 | DQ13 | DQ6 |
| VSSQ | VSSQ | 6 | VDDQ | VDDQ |
| NC | DQ3 | 7 | DQ12 | NC |
| DQ2 | DQ4 | 8 | DQ11 | DQ5 |
| VDDQ | VDDQ | 9 | VSSQ | VSSQ |
| NC | DQ5 | 10 | DQ10 | NC |
| DQ3 | DQ6 | 11 | DQ9 | DQ4 |
| VSSQ | VSSQ | 12 | VDDQ | VDDQ |
| NC | DQ7 | 13 | DQ8 | NC |
| NC | NC | 14 | NC | NC |
| VDDQ | VDDQ | 15 | VSSQ | VSSQ |
| NC | LDQS | 16 | UDQS | DQS |
| NC | NC | 17 | DNU | DNU |
| VDD | VDD | 18 | VREF | VREF |
| DNU | DNU | 19 | VSS | VSS |
| NC | LDM | 20 | UDM | DM |
| WE# | WE# | 21 | CK# | CK# |
| CAS# | CAS# | 22 | CK | CK |
| RAS# | RAS# | 23 | CKE | CKE |
| CS# | CS# | 24 | NC | NC |
| NC | NC | 25 | A12 | A12 |
| BA0 | BA0 | 26 | A11 | A11 |
| BA1 | BA1 | 27 | A9 | A9 |
| A10/AP | A10/AP | 28 | A8 | A8 |
| A0 | A0 | 29 | A7 | A7 |
| A1 | A1 | 30 | A6 | A6 |
| A2 | A2 | 31 | A5 | A5 |
| A3 | A3 | 32 | A4 | A4 |
| VDD | VDD | 33 | VSS | VSS |

NOTE:

1. All dimensions in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

## Table 3: Pin Descriptions

| PIN NUMBERS | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| 45, 46 | CK, CK# | Input | Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#. |
| 44 | CKE | Input | Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after $V_{DD}$ is applied and until CKE is first brought high. After CKE is brought high it becomes an SSTL_2 input only. |
| 24 | CS# | Input | Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code. |
| 23, 22, 21 | RAS#,CAS#, WE# | Input | Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the commandbeingentered. |
| 47<br>20, 47 | DM<br>LDM, UDM | Input | Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. For the x16 DM for DQ0–DQ7 and UDM is a DM for D08–D015. Pin 20 is a NC on x8. |
| 26, 27 | BA0, BA1 | Input | Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. |
| 29-31<br>32, 35, 36<br>37, 38, 39<br>40, 28, 41<br>42 | A0, A1, A2<br>A3, A4, A5<br>A6, A7, A8<br>A9, A10, A11<br>A12 | Input | Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command. |
| 2, 5, 8<br>11, 56, 59<br>62, 65 | DQ0-2<br>DQ3-5<br>DQ6-7 | I/O | Data Input/Output. **Data bus for x8** |
| 2, 4, 5,<br>7, 8, 10,<br>11, 13, 54,<br>56, 57, 59,<br>60, 62, 63,<br>65 | DQ0–DQ2<br>DQ3–DQ5<br>DQ6–DQ8<br>DQ9–DQ11<br>DQ12–DQ14<br>DQ15 | I/O | Data Input/Output: **Data bus for x16**<br>(Pins 4, 7, 10, 13, 54, 57, 60, 63 are NC for the x8) |

## Table 3: Pin Descriptions (Continued)

| PIN NUMBERS | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| 51<br>16, 51 | DQS<br>LDQS, UDQS | I/O | Data Strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data. for the x16, LDQS is DQS for DQ0–DQ7 and UDQS is DQS for DQ8–DQ15. Pin 16 is a NC on x8. |
| 14, 17, 25, 43, 53 | NC | - | No Connect: These pins should be left unconnected. |
| 19, 50 | DNU | - | Do Not Use: Must float to minimize noise on Vref |
| 3, 9, 15, 55, 61 | $V_{DD}Q$ | Supply | DQ Power Supply: +2.60V ±0.10V. Isolated on the die for improved noise immunity. |
| 6, 12, 52, 58, 64 | $V_{SS}Q$ | Supply | DQ Ground. Isolated on the die for improved noise immunity. |
| 1, 18, 33 | $V_{DD}$ | Supply | Power Supply: +2.60V ±0.10V. |
| 4, 48, 66 | $V_{SS}$ | Supply | Ground. |
| 49 | $V_{REF}$ | Supply | SSTL_2 reference voltage. |

## Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency should be set to 3 clocks, as shown in the CAS Latency Diagram and Mode Register Definition Diagram.

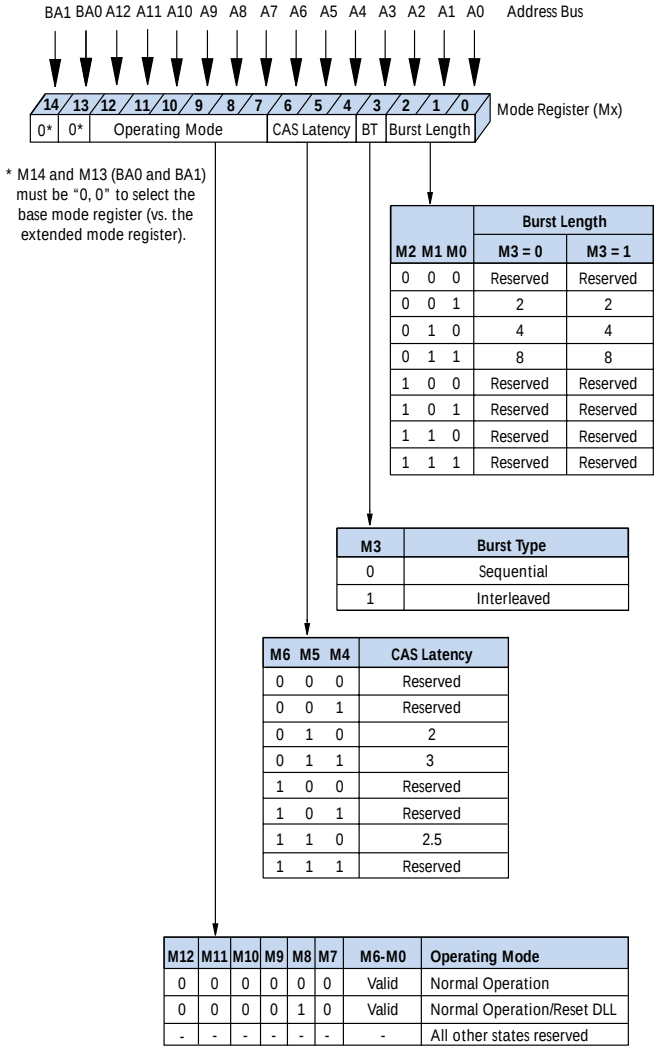
If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

## Table 4: CAS Latency (CL)

| SPEED | ALLOWABLE OPERATING CLOCK FREQUENCY (MHZ) | | |
|---|---|---|---|
| | CL = 3 | CL = 2.5 | CL = 2 |
| -5B | 133MHz ≤ f ≤ 200MHz | 75MHz ≤ f ≤ 167MHz | 75MHz ≤ f ≤ 133MHz |

## Figure 3: Mode Register Definition Diagram



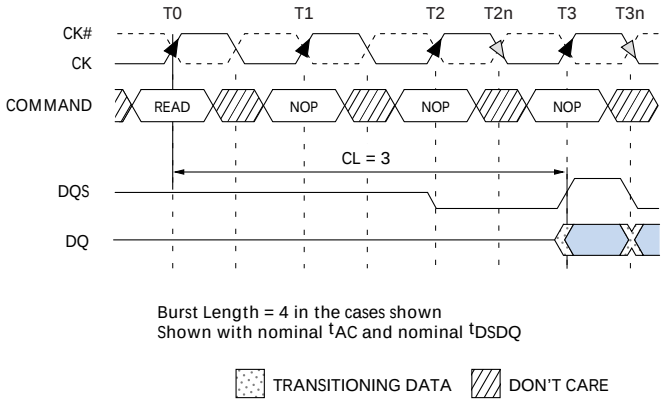

| | Burst Length | |
|---|---|---|
| M2 M1 M0 | M3 = 0 | M3 = 1 |
| 0 0 0 | Reserved | Reserved |
| 0 0 1 | 2 | 2 |
| 0 1 0 | 4 | 4 |
| 0 1 1 | 8 | 8 |
| 1 0 0 | Reserved | Reserved |
| 1 0 1 | Reserved | Reserved |
| 1 1 0 | Reserved | Reserved |
| 1 1 1 | Reserved | Reserved |

| M3 | Burst Type |
|---|---|
| 0 | Sequential |
| 1 | Interleaved |

| M6 M5 M4 | CAS Latency |
|---|---|
| 0 0 0 | Reserved |
| 0 0 1 | Reserved |
| 0 1 0 | 2 |
| 0 1 1 | 3 |
| 1 0 0 | Reserved |
| 1 0 1 | Reserved |
| 1 1 0 | 2.5 |
| 1 1 1 | Reserved |

| M12 | M11 | M10 | M9 | M8 | M7 | M6-M0 | Operating Mode |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Valid | Normal Operation |
| 0 | 0 | 0 | 0 | 1 | 0 | Valid | Normal Operation/Reset DLL |
| - | - | - | - | - | - | - | All other states reserved |

## Figure 4: Example CAS Latency Diagram with CL=3



## Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

VDD Supply Voltage
Relative to Vss .....-1V to +3.6V
VDDQ Supply Voltage
Relative to Vss .....-1V to +3.6V
VREF and Inputs Voltage
Relative to Vss .....-1V to +3.6V
I/O Pins Voltage
Relative to Vss ..... -0.5V to VDDQ +0.5V
Operating Temperature, $T_A$ (ambient)..... 0°C to +70°C
Storage Temperature (plastic) .....-55°C to +150°C
Power Dissipation.....1W
Short Circuit Output Current .....50mA

## Table 5: DC Electrical Characteristics and Operating Conditions

0°C ≤ $T_A$ ≤ +70°C; VDDQ = +2.6V ±0.1V, VDD = +2.6V ±0.1V

Notes: 1–5, 16, Refer to Base 256Mb Data Sheet, page 60-63 for all notes except 53 below.

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Supply Voltage | VDD | 2.5 | 2.7 | V | 36, 41, 53 |
| I/O Supply Voltage | VDDQ | 2.5 | 2.7 | V | 36, 41, 44,53 |
| I/O Reference Voltage | VREF | 0.49 x VDDQ | 0.51 x VDDQ | V | 6, 44 |
| I/O Termination Voltage (system) | VTT | VREF - 0.04 | VREF + 0.04 | V | 7, 44 |
| Input High (Logic 1) Voltage | VIH(DC) | VREF + 0.15 | VDD + 0.3 | V | 28 |
| Input Low (Logic 0) Voltage | VIL(DC) | -0.3 | VREF - 0.15 | V | 28 |
| INPUT LEAKAGE CURRENT<br>Any input 0V ≤ VIN ≤ VDD, VREF Pin 0V ≤ VIN ≤ 1.35V<br>(All other pins not under test = 0V) | II | -2 | 2 | µA | |
| OUTPUT LEAKAGE CURRENT<br>(DQs are disabled; 0V ≤ VOUT ≤ VDDQ) | IOZ | -5 | 5 | µA | |
| OUTPUT LEVELS: Full drive option<br>High Current (VOUT = VDDQ - 0.373V, minimum VREF, minimum VTT) | IOH | -16.8 | - | mA | 37, 39 |
| | IOL | -16.8 | - | mA | |
| OUTPUT LEVELS: Reduced drive option - x16 only<br>High Current (VOUT = VDDQ - 0.763V, minimum VREF, minimum VTT) | IOHR | -9 | - | mA | 38, 39 |
| Low Current (VOUT = 0.763V, maximum VREF, maximum VTT) | IOLR | 9 | - | mA | |

Note 53. This is the DC voltage supplied at the DRAM and is inclusive of all noise up to 20MHz. Any noise above 20MHz at the DRAM generated from any source other than the DRAM itself may not exceed the DC voltage range of 2.6V ± 100mV.

## Table 6: AC Input Operating Conditions

0°C ≤ $T_A$ ≤ +70°C; $V_{DD}Q$ = +2.6V ±0.1V, $V_{DD}$ = +2.6V ±0.1V

Notes: 1–5, 16, Refer to Base 256Mb Data Sheet, page 60-63 for all notes.

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input High (Logic 1) Voltage | $V_{IH}$(AC) | $V_{REF}$ + 0.310 | - | V | 14, 28, 40 |
| Input Low (Logic 0) Voltage | $V_{IL}$(AC) | - | $V_{REF}$ - 0.310 | V | 14, 28, 40 |
| I/O Reference Voltage | $V_{REF}$(AC) | 0.49 x $V_{DD}Q$ | 0.51 x $V_{DD}Q$ | V | 6 |

## Table 7: Capacitance (x8 TSOP)

Note: 13; Refer to Base 256Mb Data Sheet, page 60-63 for all notes.

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Delta Input/Output Capacitance: DQ0-DQ7 | $DC_{IO}$ | – | 0.50 | pF | 24 |
| Delta Input Capacitance: Command and Address | $DC_{I}1$ | – | 0.50 | pF | 29 |
| Delta Input Capacitance: CK, CK# | $DC_{I}2$ | – | 0.25 | pF | 29 |
| Input/Output Capacitance: DQs, DQS, DM | $C_{IO}$ | 4.0 | 5.0 | pF | |
| Input Capacitance: Command and Address | $C_{I}1$ | 2.0 | 3.0 | pF | |
| Input Capacitance: CK, CK# | $C_{I}2$ | 2.0 | 3.0 | pF | |
| Input Capacitance: CKE | $C_{I}3$ | 2.0 | 3.0 | pF | |

## Table 8: Capacitance (x16 TSOP)

Note: 13; Refer to Base 256Mb Data Sheet, page 60-63 for all notes.

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Delta Input/Output Capacitance: DQ0-DQ7, LDQS, LDM | $DC_{IOL}$ | – | 0.50 | pF | 24 |
| Delta Input/Output Capacitance: DQ8-DQ15, UDQS, UDM | $DC_{IOU}$ | – | 0.50 | pF | 24 |
| Delta Input Capacitance: Command and Address | $DC_{I}1$ | – | 0.50 | pF | 29 |
| Delta Input Capacitance: CK, CK# | $DC_{I}2$ | – | 0.25 | pF | 29 |
| Input/Output Capacitance: DQ, LDQS, UDQS, LDM, UDM | $C_{IO}$ | 4.0 | 5.0 | pF | |
| Input Capacitance: Command and Address | $C_{I}1$ | 2.0 | 3.0 | pF | |
| Input Capacitance: CK, CK# | $C_{I}2$ | 2.0 | 3.0 | pF | |
| Input Capacitance: CKE | $C_{I}3$ | 2.0 | 3.0 | pF | |

## Table 9: Electrical Characteristics and Recommended AC Operating Conditions

0°C ≤ $T_A$ ≤ +70°C; $V_{DD}Q$ = +2.6V ±0.1V, $V_{DD}$ = +2.6V ±0.1V

Notes: 1-5, 14–17, 33, 46; Refer to Base 256Mb Data Sheet, page 60-63 for all notes.

| AC CHARACTERISTICS | | | -5B | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | SYMBOL | MIN | MAX | UNITS | NOTES |
| Access window of DQs from CK/CK# | | $^tAC$ | -0.70 | +0.70 | ns | |
| CK high-level width | | $^tCH$ | 0.45 | 0.55 | $^tCK$ | 30 |
| CK low-level width | | $^tCL$ | 0.45 | 0.55 | $^tCK$ | 30 |
| Clock cycle time | CL=3 | $^tCK$ | 5 | 7.5 | ns | 45, 52 |
| | CL=2.5 | $^tCK$ | 6 | 13 | ns | 42,52 |
| | CL=2 | $^tCK$ | 7.5 | 13 | ns | 42, 52 |
| DQ and DM input hold time relative to DQS | | $^tDH$ | 0.40 | | ns | 26, 31 |
| DQ and DM input setup time relative to DQS | | $^tDS$ | 0.40 | | ns | 26, 31 |
| DQ and DM input pulse width (for each input) | | $^tDIPW$ | 1.75 | | ns | 31 |
| Access window of DQS from CK/CK# | | $^tDQSCK$ | -0.60 | +0.60 | ns | |
| DQS input high pulse width | | $^tDQSH$ | 0.35 | | $^tCK$ | |
| DQS input low pulse width | | $^tDQSL$ | 0.35 | | $^tCK$ | |
| DQS-DQ skew, DQS to last DQ valid, per group, per access | | $^tDQSQ$ | | 0.40 | ns | 25, 26 |
| Write command to first DQS latching transition | | $^tDQSS$ | 0.72 | 1.28 | $^tCK$ | |
| DQS falling edge to CK rising - setup time | | $^tDSS$ | 0.2 | | $^tCK$ | |
| DQS falling edge from CK rising - hold time | | $^tDSH$ | 0.2 | | $^tCK$ | |
| Half clock period | | $^tHP$ | $^tCH$,$^tCL$ | | ns | 34 |
| Data-out high-impedance window from CK/CK# | | $^tHZ$ | | +0.70 | ns | 18,42 |
| Data-out low-impedance window from CK/CK# | | $^tLZ$ | -0.70 | | ns | 18,43 |
| Address and control input hold time (slew rate = 1V/ns) | | $^tIH_F$ | 0.6 | | ns | |
| Address and control input setup time (slew rate = 1V/ns) | | $^tIS_F$ | 0.6 | | ns | |
| Address and control input hold time (slew rate = 0.5V/ns) | | $^tIH_S$ | 0.6 | | ns | |
| Address and control input setup time (slew rate =0.5V/ns) | | $^tIS_S$ | 0.6 | | ns | |
| Address and Control input pulse width (for each input) | | $^tIPW$ | 2.2 | | ns | |
| LOAD MODE REGISTER command cycle time | | $^tMRD$ | 10 | | ns | |
| DQ-DQS hold, DQS to first DQ to go non-valid, per access | | $^tQH$ | $^tHP$ -$^tQHS$ | | ns | 25, 26 |
| Data Hold Skew Factor | | $^tQHS$ | | 0.50 | ns | |
| ACTIVE to READ with Auto precharge command | | $^tRAP$ | 15 | | ns | |
| ACTIVE to PRECHARGE command | | $^tRAS$ | 40 | 70,000 | ns | 35 |
| ACTIVE to ACTIVE/AUTO REFRESH command period | | $^tRC$ | 55 | | ns | |
| AUTO REFRESH command period | | $^tRFC$ | 70 | | ns | 50 |
| ACTIVE to READ or WRITE delay | | $^tRCD$ | 15 | | ns | |
| PRECHARGE command period | | $^tRP$ | 15 | | ns | |
| DQS read preamble | | $^tRPRE$ | 0.9 | 1.1 | $^tCK$ | 42 |
| DQS read postamble | | $^tRPST$ | 0.4 | 0.6 | $^tCK$ | |
| ACTIVE bank *a* to ACTIVE bank *b* command | | $^tRRD$ | 10 | | ns | |
| DQS write preamble | | $^tWPRE$ | 0.25 | | $^tCK$ | |
| DQS write preamble setup time | | $^tWPRES$ | 0 | | ns | 20, 21 |
| DQS write postamble | | $^tWPST$ | 0.4 | 0.6 | $^tCK$ | 19 |
| Write recovery time | | $^tWR$ | 15 | | ns | |
| Internal WRITE to READ command delay | | $^tWTR$ | 2 | | $^tCK$ | |
| Data valid output window (DVW) | | N/A | $^tQH$ - $^tDQSQ$ | | ns | 25 |
| REFRESH to REFRESH command interval | | $^tREFC$ | | 70.3 | µs | 23 |
| Average periodic refresh interval | | $^tREFI$ | | 7.8 | µs | 23 |
| Terminating voltage delay to $V_{DD}$ | | $^tVTD$ | 0 | | ns | |
| Exit SELF REFRESH to non-READ command | | $^tXSNR$ | 70 | | ns | |
| Exit SELF REFRESH to READ command | | $^tXSRD$ | 200 | | $^tCK$ | |

## Table 10: IDD Specifications and Conditions

0°C ≤ $T_A$ ≤ +70°C; $V_{DD}Q$ = +2.6V ±0.1V, $V_{DD}$ = +2.6V ±0.1V

Notes: 1-5, 14–17, 33, 46, 53; Refer to Base 256Mb Data Sheet, page 60-63 for all notes.

| | | | MAX | | | |
|---|---|---|---|---|---|---|
| PARAMETER/CONDITION | | SYMBOL | -5B (X8) | -5B (X16) | UNITS | NOTES |
| OPERATING CURRENT: One bank; Active-Precharge; $^tRC$ = $^tRC$ (MIN); $^tCK$ = $^tCK$ (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles | | $I_{DD0}$ | 135 | 135 | mA | 22, 48 |
| OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 4; $^tRC$ = $^tRC$ (MIN); $^tCK$ = $^tCK$ (MIN); $I_{OUT}$ = 0mA; Address and control inputs changing once per clock cycle | | $I_{DD1}$ | 170 | 185 | mA | 22, 48 |
| PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $^tCK$ = $^tCK$ (MIN); CKE = (LOW) | | $I_{DD2P}$ | 4 | 4 | mA | 23, 32, 50 |
| IDLE STANDBY CURRENT: CS# = HIGH; All banks are idle; $^tCK$ = $^tCK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN}$ = $V_{REF}$ for DQ, DQS, and DM | | $I_{DD2F}$ | 60 | 60 | mA | 51 |
| ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $^tCK$ = $^tCK$ (MIN); CKE = LOW | | $I_{DD3P}$ | 40 | 40 | mA | 23, 32, 50 |
| ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank active; $^tRC$ = $^tRAS$ (MAX); $^tCK$ = $^tCK$ (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | | $I_{DD3N}$ | 70 | 70 | mA | 22 |
| OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $^tCK$ = $^tCK$ (MIN); $I_{OUT}$ = 0mA | | $I_{DD4R}$ | 200 | 260 | mA | 22, 48 |
| OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $^tCK$ = $^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle | | $I_{DD4W}$ | 185 | 215 | mA | 22 |
| AUTO REFRESH BURST CURRENT: | $^tRC$ = $^tRFC$(MIN) | $I_{DD5}$ | 260 | 260 | mA | 50 |
| | $^tRFC$ = 7.8us, | $I_{DD5A}$ | 6 | 6 | mA | 27, 50 |
| SELF REFRESH CURRENT: CKE ≤ 0.2V | Standard | $I_{DD6}$ | 4 | 4 | mA | 11 |
| | Low Power (L) | $I_{DD6A}$ | 2 | 2 | mA | 11 |
| OPERATING CURRENT: Four bank interleaving READs (Burst = 4) with auto precharge, $^tRC$ = minimum tRC allowed; $^tCK$ = $^tCK$ (MIN); Address and control inputs change only during Active READ, or WRITE commands | | $I_{DD7}$ | 470 | 510 | mA | 22, 49 |

**8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900**
**E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992**