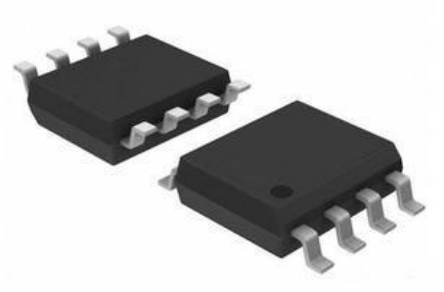
MORNSUN®

SCM1710A Highly Integrated PWM Controller

Features

- Maximum operating frequency is adjustable
- Input undervoltage protection
- Built-in compensation for opto-coupler
- Compensation for prefeedback
-
- Cycle-by-cycle current limit, overcurrent protection
- Amplitude and frequency reduction under light load condition
- Soft startup
-
- VDD overvoltage protection and undervoltage lockout
- Open loop and CS pin floating protection
- RI pin short circuit protection
- Input undervoltage protection
- Flexible drive technology
- Frequency jittering

Package



Mechanical package: SOP-8

(see "Ordering information" for details).

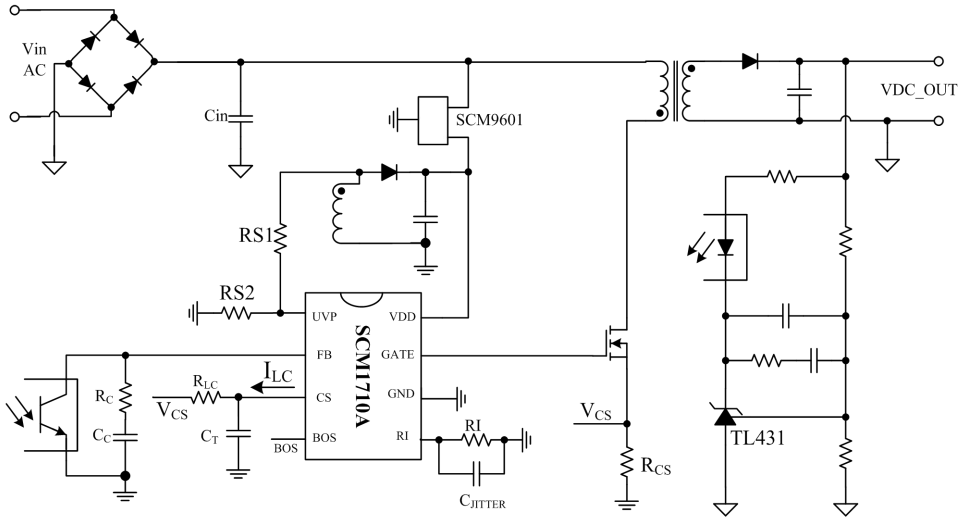
Applications

- Isolation AC-DC converters

Functional Description

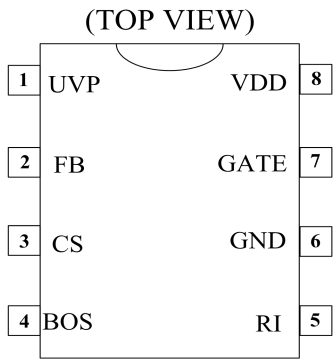
This highly integrated SCM1710A current model PWM controller is ideal for offline AC-DC converter designs. The chip's accurate operating frequency is achieved by trimming, its maximum switching frequency can be set by means of external resistor values. In case of a light load condition, the chip decreases the operating switching frequency as well as the CS peak current. Under no load (or nearly no load) condition, it operates intermittent, thus keeping the converter efficiency over the entire load range high which also results in a reduced standby power consumption. A number of compensation functions are integrated into the chip to guarantee extremely high output voltage accuracy, good dynamic response and extremely low output voltage temperature coefficient without device adding. The chip also incorporates a soft start function to improve the start stress and effectively avoiding output overshoot under light-load. EMI behavior is improved by means of flexible drive and frequency jittering technologies. A built-in management clock is preventing the loop from entering the dead zone due to interference. In additions, to increase the system reliability the SCM1710A design also includes protection features for VDD undervoltage lockout (UVLO), VDD overvoltage protection (OVP), open loop/output short circuit and overload protection (OLP), CS pin floating protection, RI pin short circuit protection, input undervoltage protection and overtemperature protection.

Typical Application Circuit

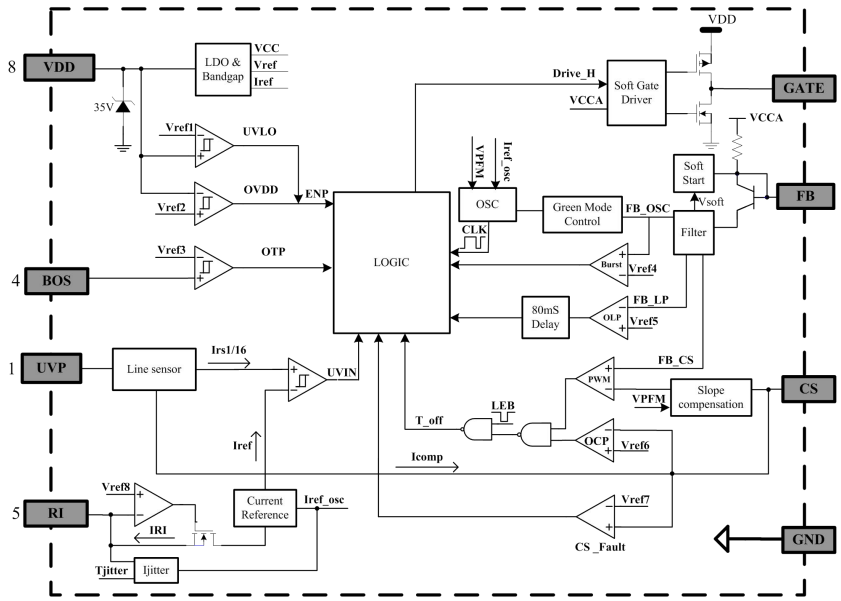


Contents

Pins



Internal Block Diagram



Pin descriptions

No.	Name	I/O	Description
1	UVP	I	The power supply line input voltage is sensed via a resistor for undervoltage protection
2	FB	I	The voltage feedback pin realizes loop feedback by means of opto-coupler signal and adjusts the PWM duty cycle ratio in combination with the current sampling (CS) signal.
3	CS	I	Current sampling input pin
4	BOS	I	BOS pin multiplexes: External NTC thermistor for overtemperature protection.
5	RI	I	PWM's operating frequency set by external resistor to ground which is connected in parallel with a capacitor for frequency jittering, thus improving full-load EMI.
6	GND	P	Ground reference
7	GATE	O	Power MOSFET gate drive pin
8	VDD	P	Chip power pin

Absolute Maximum Ratings

General test conditions: Free-air, normal operating temperature range (unless otherwise specified).

Parameter	Symbol	Min	Max	Unit
Bias mains voltage	V_{VDD}		35	V
Voltage of the GATE pin	V_{DRV}	-0.6	30	V
Voltage range	UVP,FB,CS,RI	-0.6	6	
	BOS	-0.6	30	
Storage temperature	T_{STG}	-40	150	℃
Operating junction temperature	T_J	-40	150	
Lead temperature for soldering	0.6mm from case for 10s		260	
Rated value of electrostatic discharge (ESD)	Human body model (HBM)	-2000	2000	V
	Charging device model (CDM)	-1000	1000	

Important: Exposure to Absolute Maximum Rated conditions for an extended period may severely affect the device reliability, and stress levels exceeding the "Absolute Maximum Ratings" may result in permanent damage.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Bias mains voltage	V_{DD}	8	25	V
VDD bypass capacitance	C_{VDD}	0.47	20	uF
Maximum operating switching frequency	F_{SW}	65	100	kHz
Operating junction temperature	T_J	-40	125	℃

Electrical Characteristics

General test conditions and VDD = 12V, GATE with no load (unless otherwise specified).

Symbol	Parameter	Test condition	Mini	Typ	Max	Unit
Chip power supply (VDD pin)						
$I_{STARTUP}$	VDD starting current	V_{VDD}<V_{VDD} off, current flowing into the VDD port	150	300	450	uA
I_{VDD_OP}	Chip's operating current	V_{FB}=3V, RI=24K	1.5	2.5	3.5	mA
V_{UVLO_ON}	VDD undervoltage lockout cancellation (enable)	V_{VDD}: increasing	14.8	16.1	17.4	V
V_{UVLO_OFF}	VDD undervoltage lockout	V_{VDD}: decreasing	6.8	7.4	8	V
V_{OVP_ON1}	VDD overvoltage protection trigger voltage	V_{VDD}:15V~21V FB=4V	22.3	24.2	26.2	V
V_{OVP_OFF}	VDD overvoltage protection recovery voltage	V_{VDD}: 21V~10V FB=1-4V	14.8	16.1	17.4	V
V_{OVP_HYS}	VDD overvoltage protection backlash voltage			8.1		V
V_{CLAMP}	VDD clamping voltage	Sudden improvement of the current absorption capability of VDD	30	35	40	V
Feedback voltage input (FB pin)						
A_{V_CS}	PWM input gain	$\triangle V_{FB}/\triangle V_{CS}$		2.75		V/V
V_{FB_OPEN}	FB open-circuit voltage			5.37		V
I_{FB_SHORT}	FB short-circuit current	FB grounding current	0.9	1.2	1.5	mA
V_{BURST_ON}	Frequency modulation mode entry level	VFB voltage increasing		1.25		V
V_{BURST_OFF}	Frequency modulation mode exit level	VFB voltage decreasing		1.65		V
V_{TH_PL}	FB threshold voltage during power limitation			4.55		V
Oscillator parameter (RI pin)						
F_{OSC}	Oscillator frequency	RI=24K		90.8		KHz
D_{MAX}	Maximum duty ratio		76	80	84	%
A_{JITTER}	Frequency jittering amplitude	RI=24K	86	90	95	KHz
F_{JITTER}	Frequency jittering trimming period	RI=24K	5	6	8	mS
F_{MIN1}	Minimum operating frequency during start	RI=24K		23.9		kHz
F_{MIN2}	Minimum operating frequency during steady output	RI=24K		23.9		kHz
R_{I_RANGE}	RI change range		15	24	48	KΩ
V_{RI_OPEN}	RI open-circuit voltage			2		V
Current detection input (CS pin)						
V_{CST_MAX}	Internal current limiting			0.8		V
$T_{BLANKING}$	Leading edge blanking time, RI=24K	External		-		nS
S_{COMP1}	Slope compensation	RI=24K, D∈(40%-60%)		33		mV/uS
S_{COMP2}	Slope compensation	RI=24K,		58		mV/uS

		D∈(60%-80%)				
Input voltage detection pin (UVP pin)						
I_{UVIN_ON}	Input undervoltage protection trigger current	RI=24K	150	167	184	uA
T_{UVIN1}	Input undervoltage protection trigger voltage hold time, start			3		Pulse number
T_{UVIN2}	Input undervoltage protection trigger voltage hold time, operating			2^{11}		Pulse number
K	Relation between the feedforward current from CS and the current from UVP			8		
V_{UVP_CLAMP}	UVP pin clamping voltage			5.375		V
Overtemperature protection pin (BOS pin)						
V_{OTP}	Temperature threshold voltage for overtemperature protection			2.4		V
V_{OTP_HYS}	Overtemperature protection temperature return difference			0.4		V
V_{BOS_OPEN}	BOS pin open-circuit voltage			5.135		V
Driving signal (GATE pin)						
V_{OL}	Output low level	I_O=20 mA (source) V_{VDD}=20V		0.14		V
V_{OH}	Output high level	I_O=20 mA(sink) V_{VDD}=20V		17.5		V
V_{CLAMP}	Clamping voltage	C_{GATE}=1nF		18.6		V
T_R	Output rise time	C_{GATE}=1nF V_{VDD}=20V		275		nS
T_F	Output fall time	C_{GATE}=1nF V_{VDD}=20V		47		nS
Time parameter (Timing)						
T_{D_PL}	V_{FB} overvoltage protection delay	RI=24K		$3*2^{11}$		Pulse number
T_{SLEEP}	V_{FB} overvoltage protection sleep time	RI=24K		2^{16}		S
T_{RI_SHORT}	RI pin short circuit protection detection time	RI=24K		6		Pulse number
$T_{SSTART1}$	Soft start time, V_{FB}=1.6V- 3V		7	9	11	mS

Typical Curves

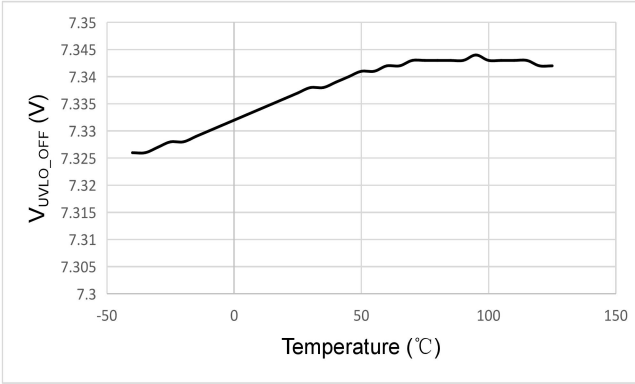


Fig.1: VDD Undervoltage Lockout vs Temperature

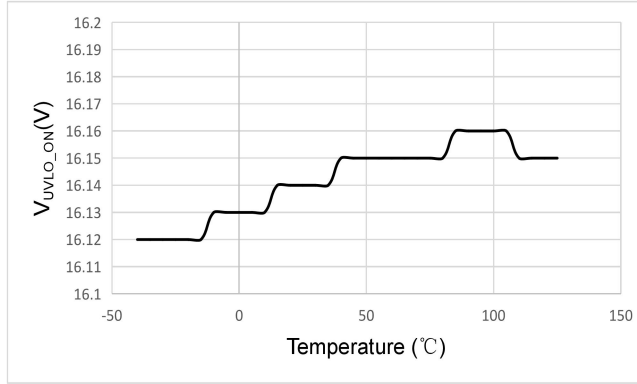


Fig.2: VDD Undervoltage Lockout Cancellation Voltage (start) vs Temperature

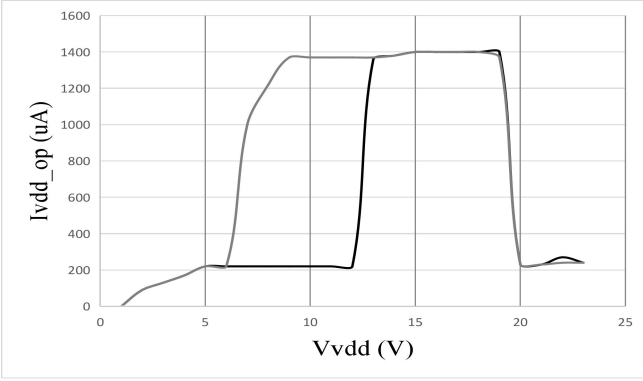


Fig.3: PWM Operating Current vs VDD Voltage

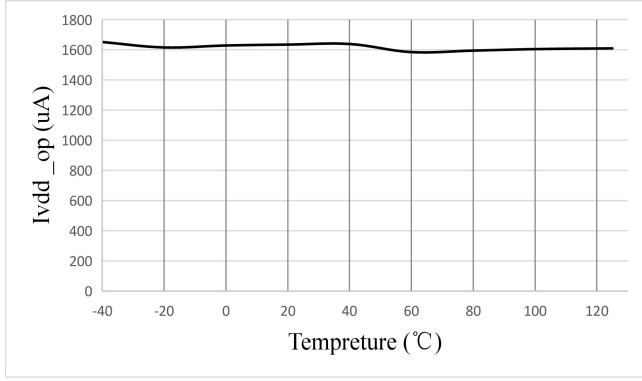


Fig.4: PWM Operating Current vs Temperature

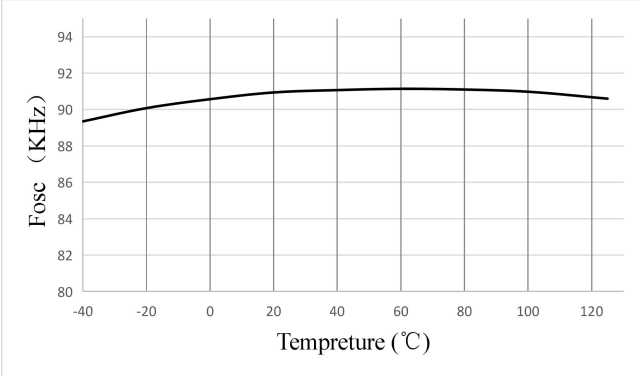


Fig.5: Operating Frequency vs Temperature

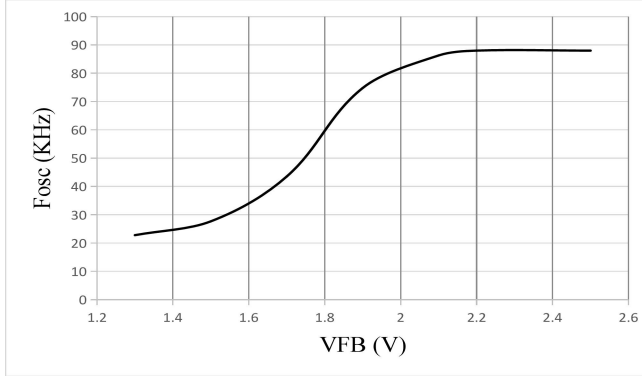


Fig.6: Operating Frequency vs V_{FB} Voltage

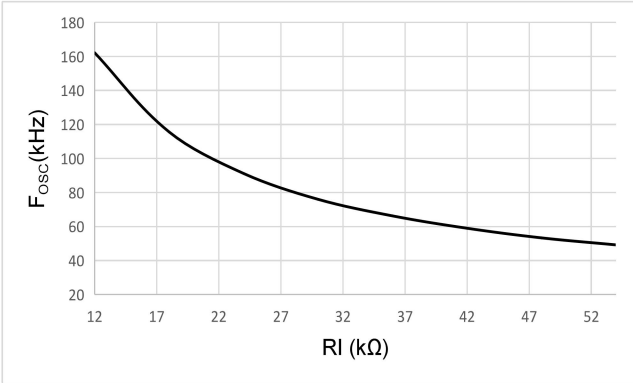


Fig.7: Operating Frequency vs RI Pin Resistance

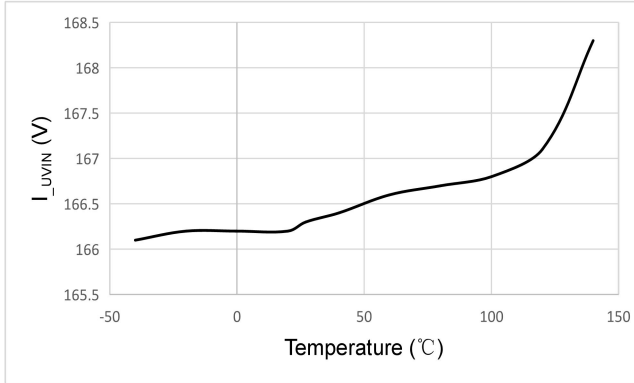


Fig.8: UVP (Input Undervoltage Protection) Pin Input Current vs Temperature

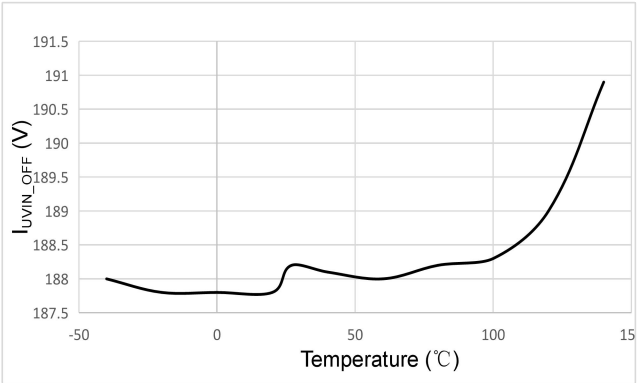


Fig.9: UVP (Input Undervoltage Protection) Cancellation Current vs Temperature

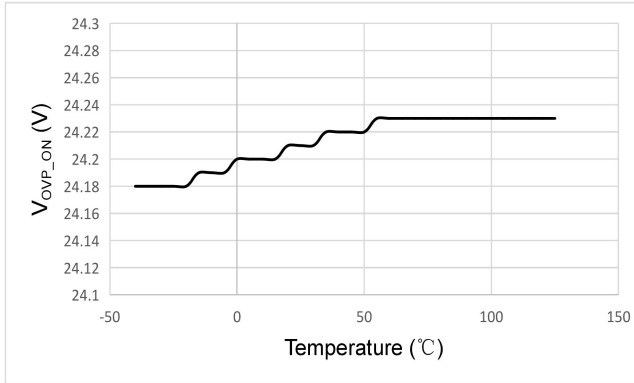


Fig.10: VDD Overvoltage Protection Voltage vs Temperature

Parameter measurement information

When testing the working current, starting and undervoltage point and other parameters related to VDD pin, see figure 11:
1) V1=6V, V2=0V, FB and BOS pins are suspended (V3 and V4 are not powered up, and a " × " in the figure indicates that the suspension is not powered up), GATE pins are suspended, and CS pins are grounded. Test the input current of VDD port, namely I_Startup;
2) Keep V2=0V, V1 increases the voltage from 0V, and the V1 value corresponding to the moment when Ivdd suddenly increases the VDD starting voltage (undervoltage lock cancellation point) of the chip;
3) Keep V2=0V, V1 reduces the voltage from 20V, and the V1 value corresponding to the moment when the input current Ivdd of VDD port suddenly decreases is the VDD undervoltage locking voltage (undervoltage point) of the chip;

When testing parameters such as chip working frequency and duty ratio, it is necessary to ensure that the under-voltage protection function of UVP pin is not triggered, as shown in figure 12:
1) V1=18V, V2= -2.25v, V3=3V. GATE is connected to the oscilloscope probe. When GATE has square wave output, the duty ratio of square wave is tested.
2) V1=18V, V2= -2.25v, V3=3V, and other Settings remain unchanged. The frequency of GATE square wave is directly tested.

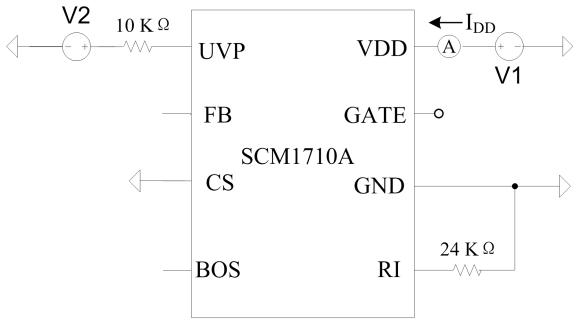


Fig.11 Principle diagram of VDD related function curve test circuit

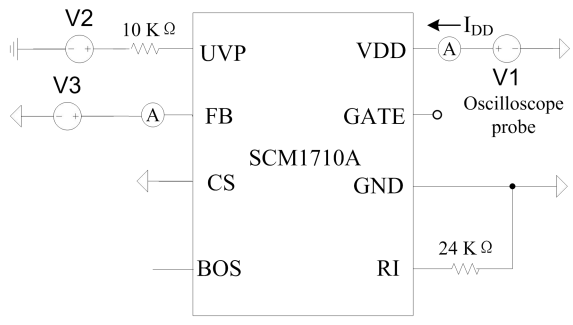


Fig.12 Principle diagram of Duty ratio and frequency test circuit

Product model overview

In SCM1710A, the chip working frequency is adjusted, with high precision, and the maximum working frequency can be changed by external resistance with different resistance values. Under light load, the working frequency and peak current amplitude of the chip will decrease with the decrease of load. When it is close to no load, the chip will work in burst mode, so that the converter can maintain high efficiency in the whole load range and reduce standby power consumption.When the voltage of FB port V_{FB} is greater than 4.55v and the cumulative time exceeds the shut-off timing T_{D_PL}, V_{FB} is considered to be overvoltage, and the GATE is immediately forced to be shut off, entering the resting state of VFB overvoltage protection. If V_{FB} is less than 4.55v before T_{D_PL}, VFB overvoltage protection will not be triggered.The rest duration of V_{FB} overvoltage protection is T_{SLEEP}. After TSLEEP, the overvoltage protection of VFB is cancelled, and the shutdown effect on GATE is cancelled. Meanwhile, the soft-start reset pulls the V_{FB} down. Overpower protection (OPP)/output short-circuit protection (OSP)/open-loop protection (OLP) can be achieved by VFB overvoltage protection, because overpower, output short-circuit and open-loop protection can cause V_{FB} to rise above 4.55v.

Recommended Application Circuit

In the practical application of SCM1710A, it is recommended to match our company's SCM9601A as the high-voltage starting circuit. For details, please refer to application circuit 13. When the input voltage reaches 40VDC, SCM9601A begins to charge the CVDD of SCM1710A bypass capacitor, and when the threshold voltage V_{UVLO_ON} of SCM1710A is reached, the GATE pin starts to output pulse signal, drive the MOS tube to conduct, and the primary side inductance storage the energy.After that, the MOS tube was turned off, and the excitation inductor on the primary side was demagnetized. Through coupling of the primary and secondary sides of the transformer, energy was transferred to the output. The output voltage gradually rose, and the feedback loop began to work. After SCM9601A reaches the timing cycle, SCM9601A is off. The product charges the C_{VDD} of SCM1710A bypass capacitor through the auxiliary winding, and the output voltage continues to rise until the output voltage is stable at the set value.

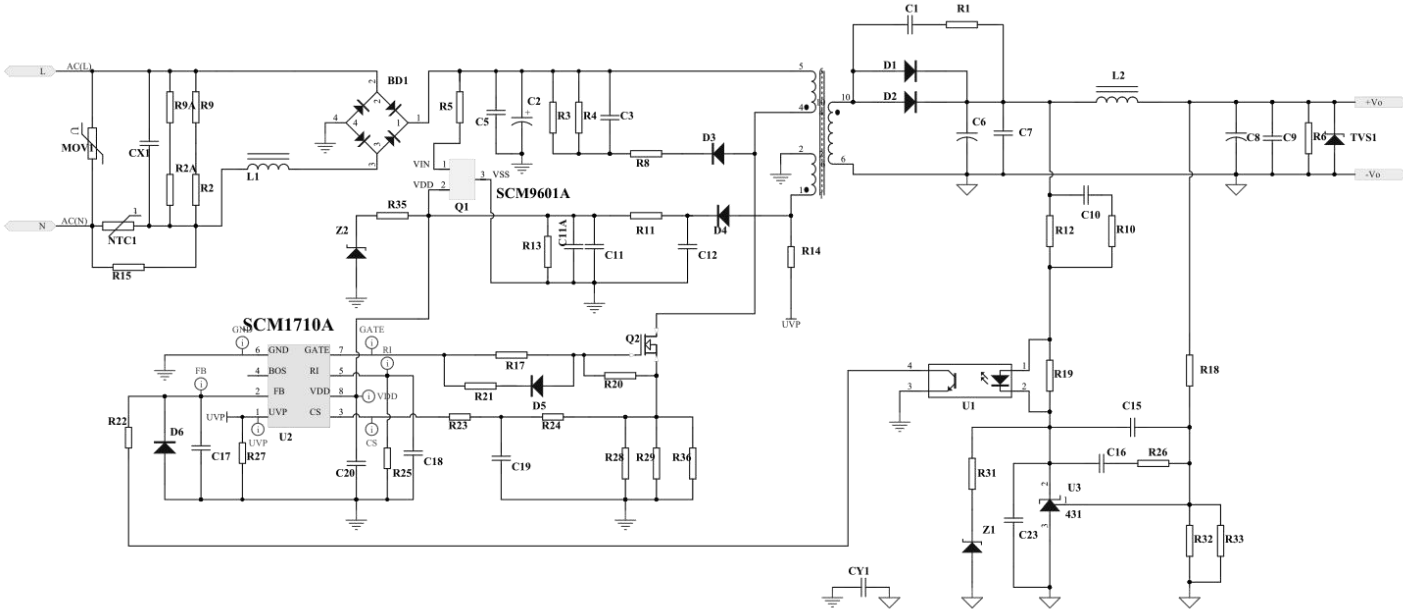


Fig.13 recommended application circuit

Functional Description

SCM1710A is a highly integrated current and voltage PWM controller applicable to offline AC-DC controllers. Viewed from its main features: In the case of a light load, the chip's operating frequency and peak current decrease with the load; in the case of nearly no load, it is in the intermittent operation, keeping high efficiency for the converter in the whole load range and reducing the standby power consumption; its chip integrates various compensators for extremely high output voltage accuracy, good dynamic response and extremely low output voltage temperature coefficient without device adding. Unless it is otherwise specified, the following values are all on the following basis: V_{VDD}=12V; RI=24kΩ; ambient temperature; ambient pressure.

VDD Undervoltage Lockout Protection

The VDD pin of the SCM1710A chip is connected via a charging capacitor to ground. Because of the VDD undervoltage lockout circuit, the chip can either be connected, disconnected or operate with changes of the VDD voltage.
The chip is connected, when V_{VDD} is greater than V_{UVLO_ON} (VDD voltage greater than undervoltage lockout cancellation voltage).
The chip operates normally when V_{VDD} is greater than V_{UVLO_OFF} (VDD is between start point and undervoltage point).
The chip is disconnected when V_{VDD} is smaller than V_{UVLO_OFF} (VDD voltage smaller than undervoltage lockout voltage).

VDD Overvoltage Protection

If the VDD voltage exceeds the overvoltage protection threshold V_{OVP_ON} for more than 200us, the chip enters the VDD overvoltage protection mode and be the GATE signal will be disabled; once the VDD voltage becomes smaller than the overvoltage protection recovery point V_{OVP_OFF}, the overvoltage protection signal is logically cancelled and the chip becomes enabled again, after soft start reset and soft start sequence the GATE output signal will start working in normal operation.

Built-in Loop Compensation

The secondary-side feedback circuit controlled by SCM1710A, consists of a TL431 providing the whole loop with maximum grain. To avoid bandwidth impact by zero poles in other positions, a zero pole is set for the TL431 to compensate the loop into a simple pole system before the crossover frequency (1/6 to 1/10 switching frequency). To compensate the impact by the pole introduced to the FB pin due to optical coupling, an internal compensation loop is set to save the external devices needed by the FB pin.

Transfer function of the SCM1710A's built-in compensation is:

$$H(s) = \frac{1 + \frac{R4}{R3+R2} \cdot S \cdot C1 \cdot (R1+R2)}{1 + S \cdot C1 \cdot (R1+R2)} \quad (1)$$

Solving zero frequency and pole frequency:

$$f_Z = \frac{T_P}{2\pi \cdot (R1+R2) \cdot \frac{R4}{R3+R4} \cdot C1 \cdot T_{SW}} \quad (2)$$

$$f_P = \frac{T_P}{2\pi \cdot (R1+R2) \cdot C1 \cdot T_{SW}} \quad (3)$$

In the expressions above: R1+R2=1.15MΩ, R3=192kΩ, R4=96kΩ, C1=10.56pF, Tp=230nS

Expression of the internal compensation zero pole:

$$f_Z = 9.05 \cdot 10^{-4} \cdot f_{sw} \quad (4)$$

$$f_P = 27.15 \cdot 10^{-4} \cdot f_{sw} \quad (5)$$

In the expression: fsw refers to operating frequency of the switch.

Built-in Soft Start

For start-up overshoot improvement under light-load conditions and to reduce start stress, the SCM1710A conducts soft start by slowly increasing the V_{FB} voltage. The V_{FB} voltage increases gradually and almost continuously. After soft start, V_{FB} is not limited by the soft start circuit, but effectively initialized during restart following the first time of start and protection. Because of different initial FB voltages, the soft start duration varies with the load (usually between 7ms and 11ms).

Intelligent Frequency Modulation Green Mode

SCM1710A can adjust the oscillator frequency, that is the frequency of the chip's GATE output signal is adjusted by detecting the V_{FB} voltage on the FB port under following scenarios : The process of FB voltage change from high to low:
V_{FB} is greater than 4.4V while FB is decreasing is interpreted by the chip as an overpower stage;V_{FB} is between 3V and 4.4V; the chip operates with maximum frequency and maximum CS peak voltage.
V_{FB} is between 2.1V and 3V; the chip is in PWM mode and only the CS pin peak voltage is adjusted, while the frequency remains unchanged at maximum.
V_{FB} is between 1.25V and 2.1V; the chip is in PWM+PFM mode in which both, the CS peak voltage and the chip's operating frequency are adjusted, and the frequency gradually decreases with the load.
V_{FB} reaches 1.25V; the chip is operating at its minimum frequency, the cs peak voltage reduces to 1/5 of $V_{CST\_MAX.}$.
V_{FB} is smaller than 1.25V; the chip is in Burst mode and the GATE output signal stops .The curce of working mode chenging with time is shown in the figure14.

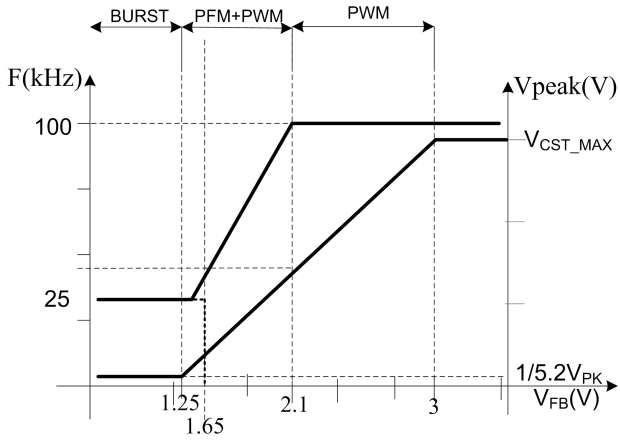


Fig.14 V_{FB} VS switching frequency and CS peak voltage

Burst Mode

The SCM1710A design includes an intermittent mode (also called the frequency hopping mode) that reduces the no-load losses. It activates once V_{FB} drops to 1.25V and the chip cuts off the GATE output. The output voltage drops caused by the power consumption of the load. The opto-coupler current decreases and the V_{FB} voltage start to increase again. Once the V_{FB} voltage level reaches 1.65V, the GATE output signal resumes at its minimum frequency (one fourth of the maximum frequency), which ideally should be above 22kHz to avoid audible noise. In this stage with the GATE drive signal output enabled, the power supply's output voltage starts to increase and only if V_{FB} becomes smaller than 1.25V again, the SCM1710A re-enters its intermittent mode once (see Fig.15).

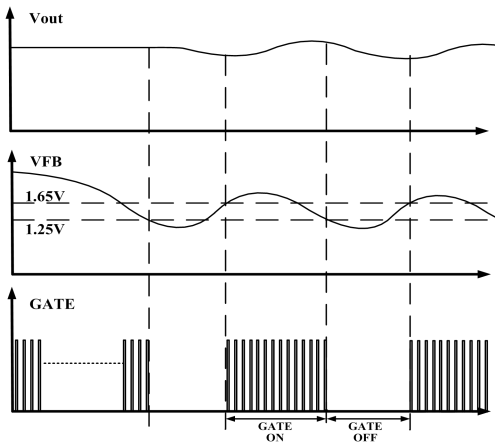


Fig.15 Burst mode time sequence

Note: Burst mode has a delay time of about 80us leaving some response time for the loop.

Full-load Frequency Jittering

For EMI improvement under full-load condition, a frequency jittering function is used when operating with the maximum frequency. The RI pin is connected to ground via paralleled external resistor and capacitor to realize this function (recommended value of C_{JITTER} = 1nF to 2nF, see typical application circuit). This spreads the energy to a range larger than the bandwidth of the EMI tester. With an RI value of 24kΩ, the frequency jittering has a period of about 5ms to 8ms and an amplitude of -4.2% to +5.3%.

Note: Frequency jittering function is disabled with RI pin without connect capacitor.

Built-in Slope Compensation

A two-stage compensation design is used. The slop is 33mV/uS when the duty cycle is between 40% and 60%, or 58mV/uS when the duty cycle is in the range from 60% to 80%. This design by segment avoids the slope compensation's impact on the load capacity. The slopes described above are typical values measured when the external resistor connected to the RI pin has a value of 24kΩ.

Oscillator Frequency

The chip's maximum operating frequency (oscillator frequency) F_{max} can be set through the external resistor connected to the RI pin as follows.

$$F_{MAX}(kHz) = 12.7 + \frac{1874}{RI(k\Omega)} \quad (6)$$

The recommended maximum operating frequency of the chip is between 65kHz and 100kHz (see also section "Recommended Operating Conditions"). Having the maximum operating frequency of the chip too low, can result in a large RI resistance and interference on the RI pin. With the chips' maximum operating frequency too high, affects the chip's power consumption (increase) and the frequency accuracy (decrease). When the minimum frequency is below about 20kHz can result in possible audible noise especially in the event of an extremely small loads.

The following equation is for calculating the minimum operating frequency.

$$F_{MIN}(kHz) = 12.7 + \frac{268}{RI(k\Omega)} \quad (7)$$

Maximum Peak Current

Compensator and related logic circuit inside the SCM1710A are limiting the maximum CS pin voltage to a value of VCST_Max. The primary side inductor's maximum peak current I_{PL_MAX} meet is calculated by the following equation (slope compensation NOT considered):

$$I_{PK\_MAX} = \frac{0.8 - V_{RLC}}{R_{CS}} \quad (8)$$

Where: R_{CS} refers to the current sampling resistor; V_{RLC} refers to the voltage across the feed-forward resistor which can be solved per following equation:

$$V_{RLC} = \frac{V_{IN} \cdot T_D}{L_P} \cdot R_{CS} \quad (9)$$

T_D refers to the current detection delay including the on-off delay of the switch. L_P refers to primary side inductance of transformer.

Input Undervoltage Protection

An input undervoltage protection can be designed around the UVP pin. Suppose that RS1 is a pull-up resistor at the UVP end (refer to the Typical Application diagram), that the primary-side and secondary-side windings have a turn ratio of NP/NA and that the external resistor connected to the RI pin is RI (kΩ), then the input undervoltage point can be solved through the following equation:

$$V_{IN\_ON} = \frac{N_P}{N_A} \cdot \frac{4 \cdot R_{S1}}{RI} \quad (10)$$

The input undervoltage recovery point can be solved through the following equation.

$$V_{IN\_OFF} = \frac{9}{8} \cdot \frac{N_P}{N_A} \cdot \frac{4 \cdot R_{S1}}{RI} \quad (11)$$

If there is an input undervoltage during start (input voltage is still below the undervoltage recovery point), the output will be directly stoped after outputting three pulses. If the chip detects an input undervoltage during normal operation of the converter, it enters a off timing sequence and detects whether the input undervoltage is still present after 2^{11} switching periods. If the input undervoltage is still detected, the chip continues with the off timing after outputting two pulses until the input voltage is detected to be above the undervoltage recovery point and subsequently, the chip will begin to output normal continuous pulses again.

Note that the RS2 resistor value must be guaranteed under following two conditions：

(1)The partial voltage of the auxiliary winding on RS2 is less than 6V during degaussing stage；

(2)RS2≥10KΩ is true (the error of the input undervoltage point is less than 5%).

Feed-forward Compensation

Input voltage sampling is realized by the UVP pin and the feedforward resistor RLC generates a compensation voltage VRLC for feedforward compensation with the purpose of equal overcurrent corresponding to high or low input voltage. RS1 is the pull-up resistor at the UVP end. Solving the resulting Rcs voltage after compensation:

$$V_{RCS} = V_{RCS\_IDEAL} + \left(\frac{R_{CS} \cdot T_D}{L} - K \cdot \frac{N_A}{N_P} \cdot \frac{R_{LC}}{R_{S1}} \right) \cdot V_{IN} \quad (12)$$

V_{RCS_IDEAL} is the ideal voltage in R_{CS}.

Supposing the content in the brackets is zero, then:

$$\frac{R_{CS} \cdot T_D}{L} = K \cdot \frac{N_A}{N_P} \cdot \frac{R_{LC}}{R_{S1}} \quad \frac{R_{CS} \cdot T_D}{L} = K \cdot \frac{N_A}{N_P} \cdot \frac{R_{LC}}{R_{S1}} \quad (13)$$

The feedforward resistor value R_{LC} can be solved by following equation:

$$R_{LC} = \frac{R_{CS} \cdot T_D \cdot R_{S1}}{K \cdot L \cdot N} \quad (14)$$

In the equation above:

- Td is the current detection delay including the on-off delay of the switch.
- LP is the primary side inductance of the transformer.
- RS1/RCS is input resistance and current sampling resistance respectively (see the Typical Application diagram).

V_{FB} Overvoltage Protection

When the total time during which the V_{FB} voltage at the FB port is above 4.55V exceeds the switch off time Td_PL (i.e. $3*2^{11}$TOSC), it will be assumed that V_{FB} is in overvoltage state and the chip will immediately be forced to enter the V_{FB} overvoltage protection sleep mode and stop the GATE. In case the

V_{FB} voltage falls below 4.55V before the total time reaches T_{D_PL}, then the V_{FB} overvoltage protection will not be triggered. After the duration of the V_{FB} overvoltage protection sleep mode T_{SLEEP} (i.e. 2^{16}TOSC) is reached, the chip will deactivate the V_{FB} overvoltage protection, decrease the V_{FB} voltage with the help of the soft starter and, successively entering a soft start sequence assuming there is no other protection mode detected.

The V_{FB} overvoltage protection function can also be used to detect protection from overpower (OPP), output short circuit (OSP) and open loop (OLP) situations because if the VFB voltage increases to a level of 4.55V or higher due to overpower, output short circuit or open loop, the protection is being activated.

The figure below shows the sequence of V_{FB} and GATE signal in case of an output short circuit condition. T1 indicates the soft start process, V_{FB} changes with the capacitor charging voltage V_{SOFT} during soft start sequence. T2 denotes V_{FB} overvoltage protection delay time, with GATE signal not yet forced to be stoped. T3 shows V_{FB} overvoltage protection sleep time duration, after which the chip resets and re-initiates a soft start sequence.T4 is the initial blanking time, it contains 4 periods of internal clock.

If an output fault condition remains, the above process will repeat itself periodically.

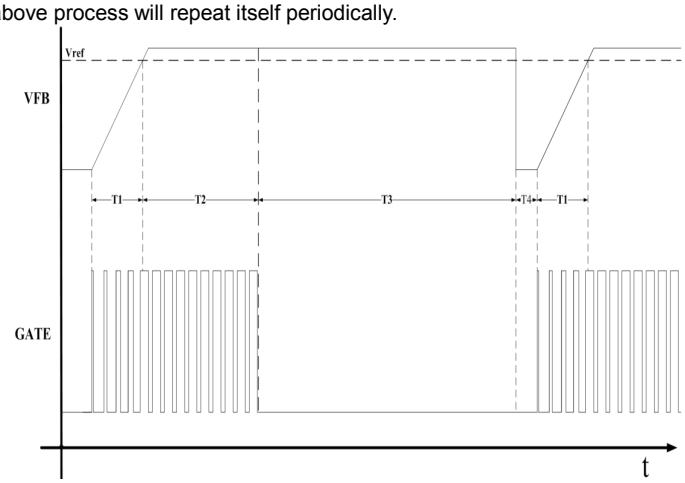


Fig.16 V_{FB} overvoltage protection sequence

Overtemperature Protection

The BOS pin is connected to a NTC thermistor which realizes the overtemperature protection.

The overtemperature protection is enabled when the voltage at the BOS pin is below 2.4V and disabled when the BOS pin voltage is above 2.4V.

$$I_{BOS} = \frac{2V}{RI} \quad (15)$$

Current from BOS pin with a voltage greater than 2.4V:

$$I_{BOS} = \frac{3}{4} \cdot \frac{2V}{RI} \quad (16)$$

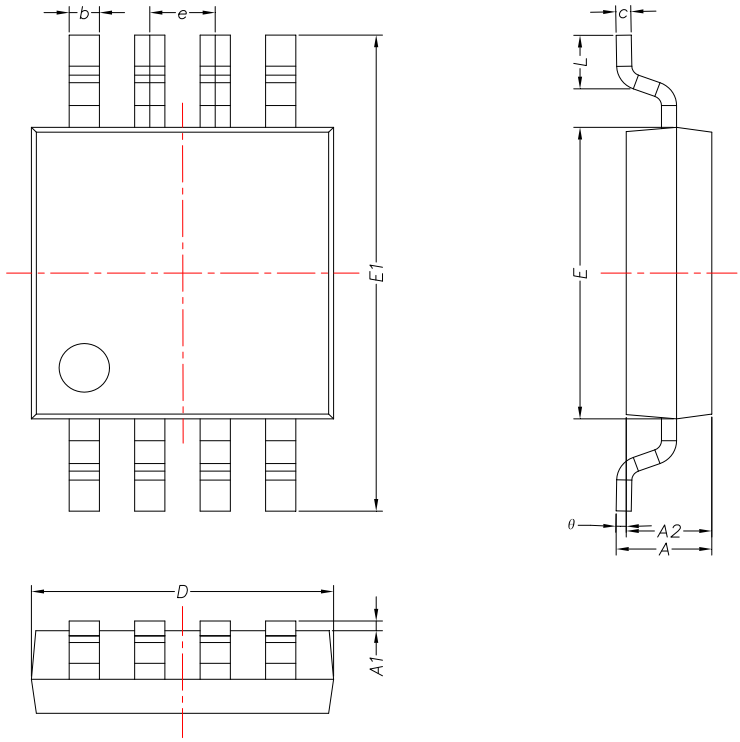
Current from the BOS pin with a voltage lower than 2.4V:

Ordering Information

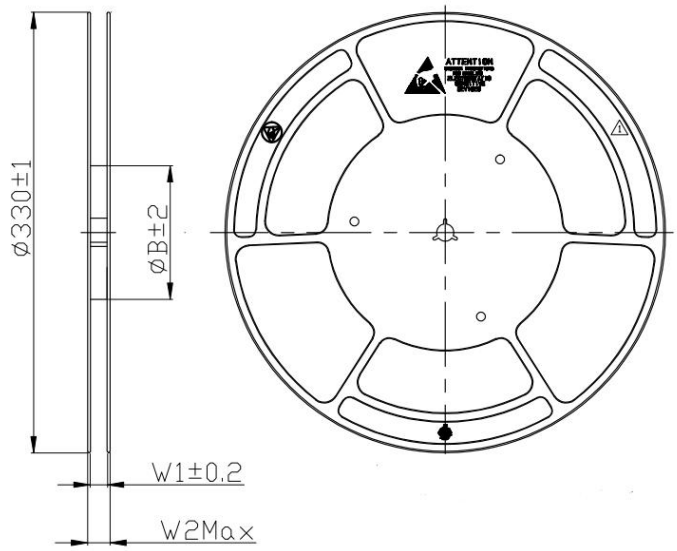
Part number	Package type	Number of Pins	Product marking	Tape & Reel
SCM1710ASA	SOP-8	8	SCM 1710ASA YM	3K/reel

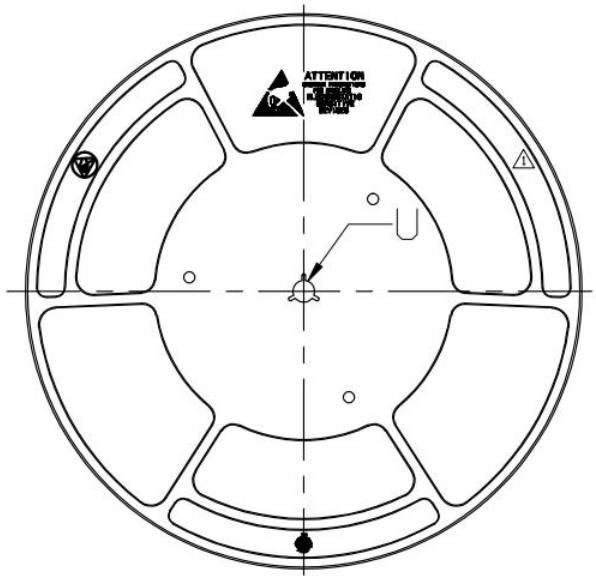
Product marking and date code
SCM1710XYZ:
(1) SCM1710 = Product designation
(2) X = Version code information (A-Z)
(3) Y = Packaging definition code; S for SOP package, M for MSOP package
(4)Z = Operating temperature range (C = 0℃ to +70℃, I =-40℃ to +85℃, A =-40℃ to +125℃, M = -55℃ to +125℃) .
(5) YM = Date code for product traceability; Y = code for production year; M = code for production month

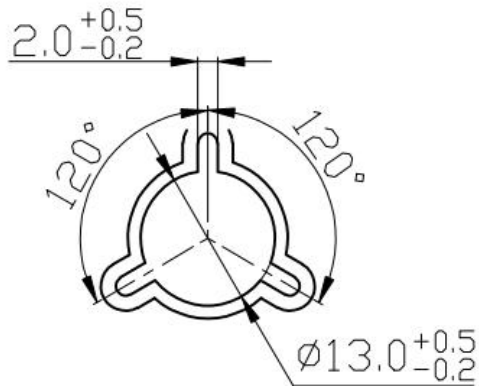
Package Information (SOP-8)



SOP-8				
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
L	0.400	0.800	0.016	0.032
θ	0°	8°	0°	8°







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Disc dimensions (mm)				
Package type	Carrier tape width	B	W1	W2Max
SOP-8	12	180	12.4	18.4

Technical requirements:

1.Color: Blue (color numbers for reference):

PANTONE DS 196-1 C; C100 M70 Y0 K0
PANTONE DS 197-1 C; C100 M70 Y0 K10
PANTONE DS 205-1 C; C100 M60 Y0 K20
PANTONE DS 205-2 C; C85 M50 Y0 K20
PANTONE DS 206-2 C; C85 M50 Y0 K35
PANTONE DS 219-1 C; C90 M50 Y5 K15)

2.Dimensions and tolerances according to ANSI/EIA-481-C-2003;

3.The disc should be glossy and without warping;

4.The outer package should be in good condition and without damage or contamination.

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