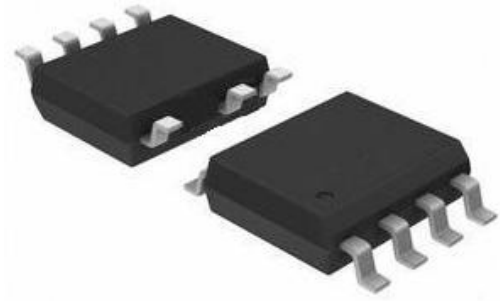
MORNSUN®

SCM1725A Control Chip for the Power Supply of Cost Control Switch

Features

- Built-in 650V power MOSFET
- Built-in VDD quick start function
- Frequency Reduction at Light Load and Burst Mode Control under no load
- The maximum operating frequency of the chip is fixed at 122kHz, and provided with built-in frequency jitter function
- Built-in slope compensation
- Current limit per cycle
- Current mode control
- Built-in soft start function
- VDD Over-Voltage Protection (OVP)
- VDD Under-Voltage Lockout (UVLO)
- Open-loop and output short-circuit protection
- Chip power consumption is less than 20μA in turn-off mode
- Peak power up to 20W

Packaging



Mechanical package: SOP-7, (see “Ordering Information” for details).

Application

- Control system for cost control switch
- ACDC non-isolated power supply

Functional Description

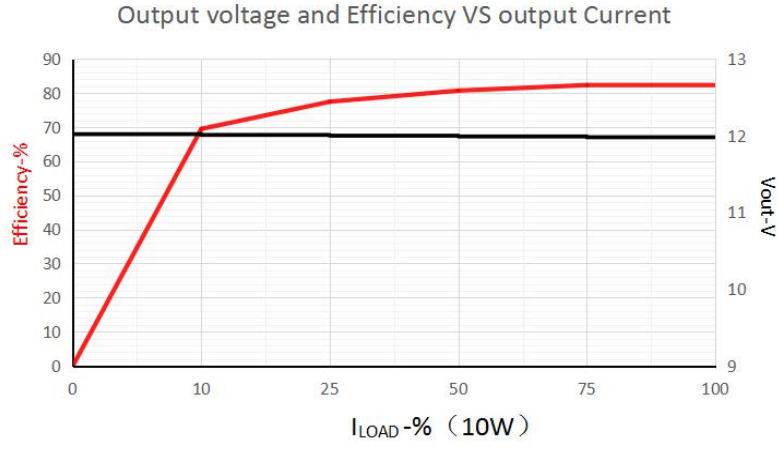
SCM1725A is a high-performance current-mode PWM control chip, which is built-in a 2A power MOSFET with minimum drain voltage up to 650V. The chip's high voltage start pin is connected directly to the power bus voltage to realize the fast charging of VDD by-pass capacitor. In addition, after the chip is provided with short circuit protection, the VDD capacitor voltage drops to the undervoltage point of VDD, and the high voltage fast start circuit is restarted to charge the VDD by-pass capacitor until VDD start voltage is reached, then the start circuit stops working and the chip’s power consumption remains relatively low.

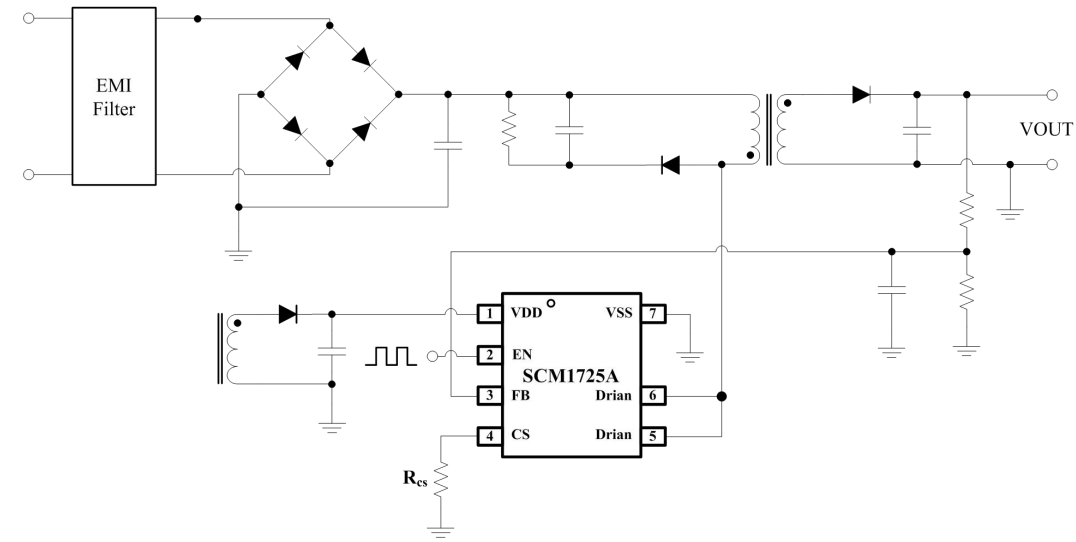
With built-in light-load frequency hopping mode, the chip has good efficiency performance under light load. Furthermore, designed with the built-in duty cycle slope compensation, internal loop compensation circuit, etc, the chip can provide more stable system loop operation. The chip also integrates a series of protection functions to improve system reliability.

In addition, the chip integrates EN pins and when externally connected to the logic high-level control chip, can enable the ultra-low power mode, with the voltage of VDD pin controlled around 8.6V.

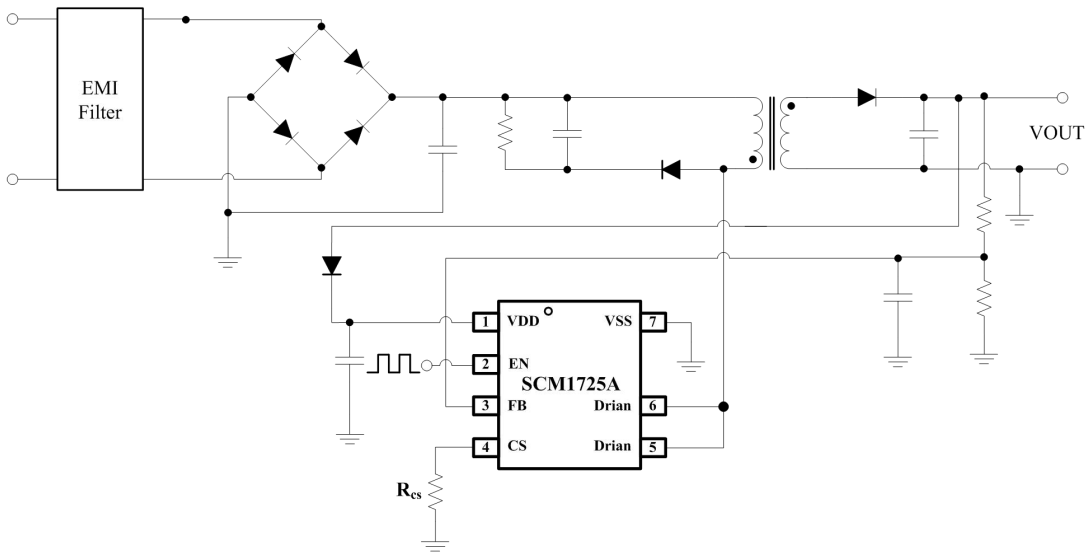
When the IC have sufficient heat dissipation conditions,the maximum output peak power is up to 20W when the intermittent opration is performed at an open temperature of 75 ℃ for 3S on and 3S off.

Function Curve





Typical application circuit 1



Typical application circuit 2

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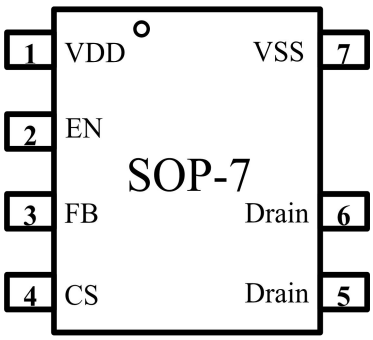
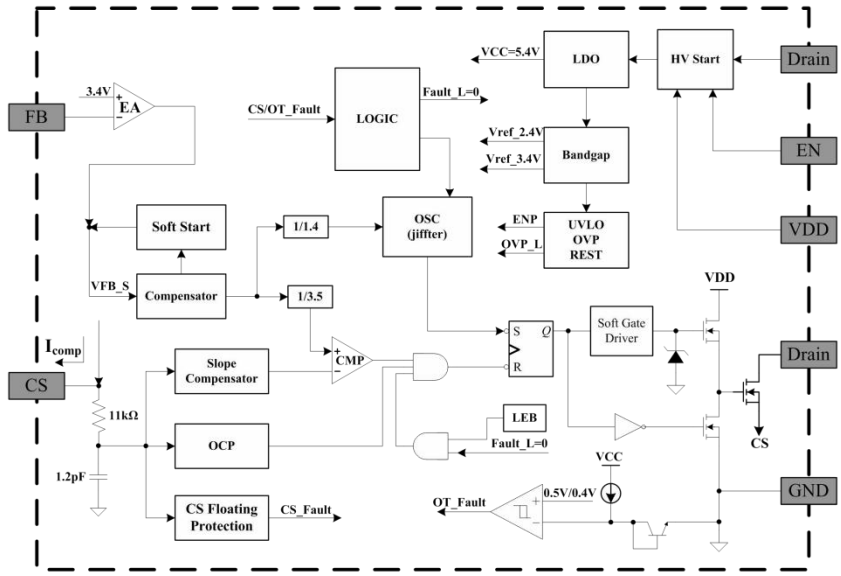
Pin



Internal Block Diagram



Pin Description

No.	Name	I/O	Description
1	VDD	I	The VDD input pin is the bias-supply from the transformer auxiliary winding to the controller. It requires a bypass capacitor to GND (VSS)
2	EN	I	High-voltage start-up circuit control terminal, when externally connected to high level, the chip is internally in turn-off low-power mode
3	FB	I	Voltage feedback pin, inverted input terminal of EA in chip
4	CS	I	Current sense input
5	Drain	O	This connects to the internal MOSFET drain and the high voltage (D) pin may be connect directly to the transformer, providing the charge current to the VDD capacitor for starting up the power supply
6	Drain	O	
7	VSS	P	The VSS ground (GND) pin is both, the controller reference pin and the drive outputs low-side return. Special care must be taken to keep all AC-decoupling capacitors returns as close as possible to this pin and avoiding any lengthy common traces with analog signal return paths

Absolute Maximum Ratings

Test conditions: Free-air, normal operating temperature range (unless otherwise specified), voltage reference is ground.

Parameter	Symbol	Min	Max	Unit
Bias supply voltage	V_{VDD}		30	V
Voltage range	V_{FB},V_{CS},V_{EN}	-0.6	6	V
Storage temperature Range	T_{STG}	-55	150	℃
Soldering Temperature (Allowable reflow soldering temperature of chip within 10 seconds)			260	
Moisture Sensitivity Level	MSL	MSL3		
Electro Static Discharge (ESD) rating	Human body model (HBM)		3500	V
	Charged device model (CDM)		1000	
Operating junction temperature	T_J	-40	150	℃

Note: Exposure to absolute-maximum-rated conditions for extended periods may severely affect device reliability, stress levels exceeding the “Absolute Maximum Ratings” may result in permanent damage.

Recommended Operating Parameters

Test conditions: Free-air, normal operating temperature range (unless otherwise specified), V_{VDD}=12V.

Parameter	Symbol	Min	Max	Unit
Bias supply voltage	V_{VDD}	9	23	V
VDD bypass capacitor	C_{VDD}	0.047	22	uF
Full Load Operating frequency	F	111	133	kHz
Operating junction temperature	T_J	-40	125	℃

Electrical Characteristics

Test conditions: Free-air, normal operating temperature range (unless otherwise specified), V_{VDD}=12V.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
High voltage start (Drain pin)						
I_{START}	Current flowing out of the VDD pin	H_{VIN}=40V, V_{VDD}=5V	0.6	1	5	mA
I_{VDD_DOWN}	The current flowing in from the Drain pin when the EN is connected to a high level	H_{VIN}=40V, V_{EN}=3.3V	6	9	20	uA
V_{VDD_ENH}	After power-up, make EN = 3.3V, VDD connect 1uF capacitance	H_{VIN}=40V, V_{EN}=3.3V	7.8	8.65	9.4	V
$V_{VDD\_ENH\_0.5mA}$	After power-up, make EN = 3.3V, VDD connect 1uF capacitance and 0.5mA load	H_{VIN}=40V, V_{EN}=3.3V	5.8	6.5	7.2	V
I_{STLKG}	Leakage current	V_{Drain}=400V, run state		1		uA
T_{J_STOP}	Thermal Shutdown Temperature	Internal junction temperature		152		℃
$T_{J\_RESTART}$	Thermal Restart Temperature	Internal junction temperature		101		℃
Supply Section (VDD pin)						
I_{VDD_OP}	operating supply current	F_{OSC}=122kHz, V_{VDD}=12V	0.7	1.0	2.0	mA
V_{VDD_ON}	VDD Turn-on Threshold	V_{VDD} increasing	16.1	17.52	19.2	V
V_{VDD_OFF}	VDD Turn-off Threshold	V_{VDD} decreasing	8.5	9.56	10.6	V
V_{VDD_OVP}	VDD OVP Threshold	V_{VDD} from 18V~30V	25.0	26.0	27.0	V
$V_{VDD\_OVP\_HYS}$	VDD OVP Hysteresis			3		V
Enable control Section (EN pin)						
V_{TH+}	Forward threshold voltage of EN pin	V_{VDD_MAX}=15V			2.5	V
V_{TH-}	Negative threshold voltage of EN pin		0.75			V
R_{IN_EN}	EN pull-down resistance			725		kΩ
Feedback voltage input Section (FB pin)						
V_{REF_FB}	FB feedback voltage		3.350	3.380	3.410	V
A_{EA}	Error amplifier gain			200		V/V
A_{VCS}	PWM gain	$\triangle V_{EA\_O}/\triangle V_{CS}$		3.5		V/V
R_{IN_FB}	FB Input Impedance			∞		Ω
Drain of power MOS (Drain pin)						
R_{DS_ON}	Power MOS ON-state resistance	V_{GS}=10V, I_D=1A			5	Ω
V_{BR_DSS}	Power MOS breakdown voltage	V_{GS}=0V, I_D=250uA	650			V
I_{DSS}	OFF-state current	V_{DS}=650V,V_{GS}=0V			1	uA
I_D	Maximum continuous drain current			2		A
V_{GS_TH}	Threshold voltage	V_{GS}=V_{DS},I_D=250uA	2		4	V
Oscillator part						
F_{OSC}	Oscillator frequency		111	122	133	kHz
D_{MAX}	Maximum duty cycle		73	77	81	%
A_{JITTER}	Frequency jitter amplitude	F_{OSC}=122kHz		±4		kHz
F_{JITTER}	Adjustment range of frequency jitter	F_{OSC}=122kHz		125		Hz
F_{MIN}	Minimum operating frequency			30		kHz
Current sense input Section (CS pin)						
$V_{TH\_OC\_MAX}$	Internal current limit threshold		0.75	0.8	0.85	V
V_{CS_FAULT}	Fault trigger voltage of CS pin		-	1.5	-	V
t_{LEB}	Leading edge blanking time		-	210	-	ns
S_{COMP}	Slope compensation	F_{OSC}=122kHz	-	78	-	mV/us
Time parameters						
$T_{SOFTSTART}$	System soft start-up time			7.6		mSec
T_{D_PL}	Power limit delay time	F_{OSC}=122kHz		76		mSec

Overview of chip

SCM1725A is a high performance and high integrated control chip for current mode PWM, suitable for non-isolated AC-DC flyback converter and cost-control switch control system. The chip has the fixed maximum operating frequency of 122 kHz and when working at a lighter load, the chip will reduce the operating frequency to achieve higher power efficiency, and the chip also internally realizes operating frequency jitter.

Without special instructions, the following values are typical values under free-air, normal operating temperature range, V_{VDD} = 12V, F_{OSC} = 122kHz.

High-voltage start-up operation

The controller takes power from the input voltage through the Drain pin and charges the VDD bypass capacitor to complete the start-up, as shown in Figure 1, the converter is energized and starts the circuit to enable the current ISTART to charge the bypass capacitor until the V_{VDD} = V_{VDD_ON}, then the GATE drive signal (the internal signal of SCM1725A) is output and the start-up circuit closed, the V_{VDD} voltage will drop.Before V_{VDD} drops to V_{VDD} <V_{VDD_OFF}, the output voltage can give VDD bypass capacitors feedback energy and V_{VDD}> V_{VDD_OFF}, then SCM1725A can start switching power supply, otherwise the start-up cannot be completed.

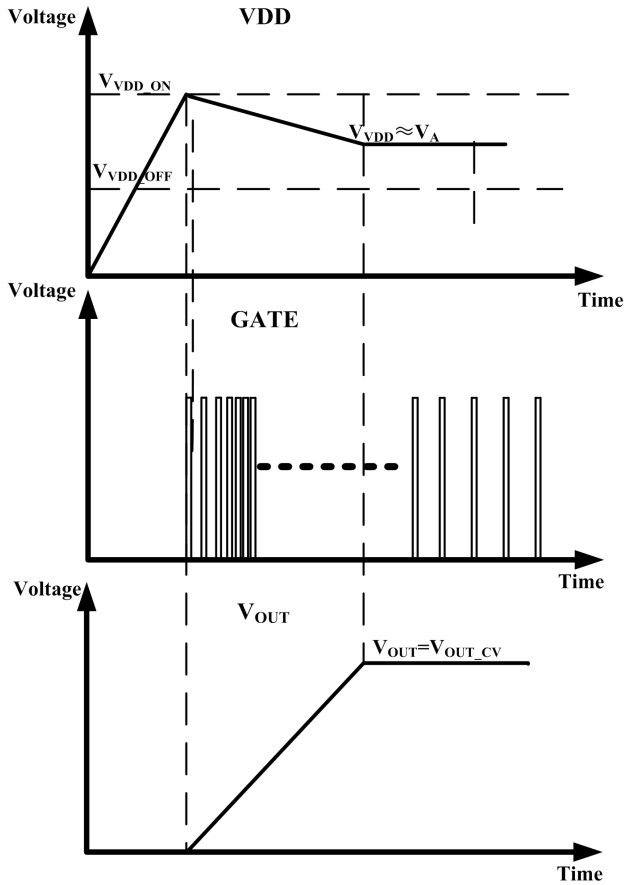


Figure 1 Wave diagram of high voltage start-up process

VDD (supply section)

The controller's power supply port is externally connected to bypass capacitance C_{VDD}. After energizing, the built-in start-up circuit charges the capacitor C_{VDD}, and the voltage of VDD pin rises. When VDD voltage is charged to the turn-on threshold V_{VDD_ON}, the controller starts to work, and the static power consumption of controller is about 750uA when the drive's power dissipation is ignored. In the absence of feedback (e.g. output short circuit, no drive output when in the protected state, etc.), since the controller's power consumption will eventually make the VDD voltage drop to the turn-off threshold V_{VDD_OFF}, at this point the controller stops outputting drive signal, the controller is quickly charged internally, and the system starts to charge the capacitor C_{VDD} again, it is required to repeat above operations until the output is maintained at a stable value (higher than V_{VDD_OFF}) for VDD capacitive C_{VDD} power supply.

Operate at sleep mode

Grounded or vacant EN pin does not affect the normal operation of chip and the sleep mode at very low-power dissipation without external control; when connected to a high level, EN controls the charging path of internal high voltage start circuit and turns off the internal power supply and all the modules so that the chip has the power consumption lower than 20μA. VDD pin has the voltage of 8.6V when not loaded, and will decrease after loaded.

Intelligent frequecy reduction mode

For the power supply before start-up, the FB pin voltage is 0V (when the power output voltage is 0V), then the chip's internal control is subject to soft start, the switching frequency rises from the minimum value to 122kHz. After the soft start-up process is finished and output voltage reaches a stable value, FB pin has the voltage remained about 3.4V. Overload protection, frequency reduction and frequency modulation are realized by comparing the output voltage V_{EA_O} of EA with the reference voltage. The oscillation frequency of cost-control switch chip is determined by the chip internally, with the maximum operating frequency of 122kHz. In addition, the chip is internally integrated with the frequency jitter function to improve wthe EMI performance.

The cost-control switching chip can adjust the frequency of oscillator by comparing the FB port voltage with the reference voltage, i.e. the frequency of output signal of the chip, and perform different operating modes in different voltage ranges by judging the output voltage of internal EA, as shown in Figure 2. When 2.4V <V_{EA_O} <3.45V, the chip is in PWM mode and only adjusts the peak voltage at CS, remains at the maximum frequency and constant; when 1.24V <V_{EA_O} <2.4V, the chip is in PWM+PFM mode, adjusts both the peak voltage at CS and the operating frequency of chip. The frequency decreases gradually as the load decreases. When 1.1V <V_{EA_O} <1.24V, the chip is in PWM mode, and the chip remains at the minimum operating frequency of 30kHz.

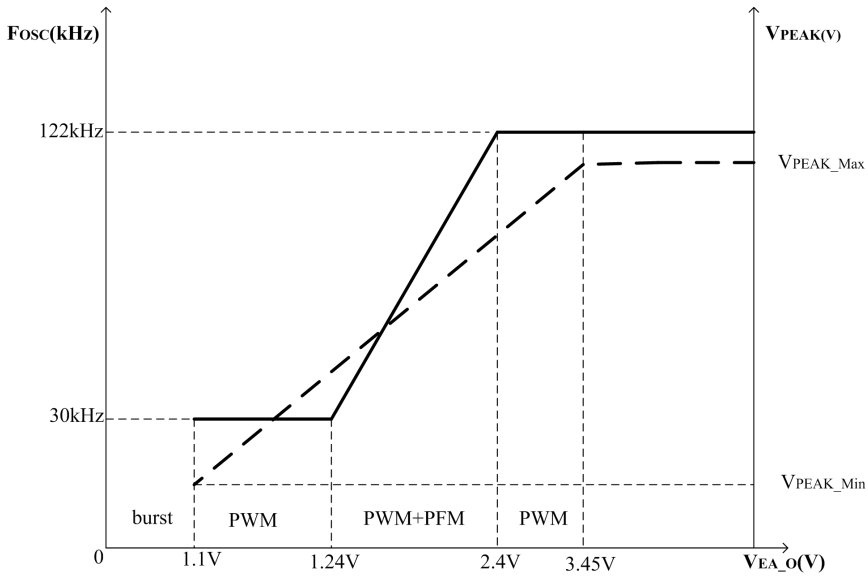


Figure 2 Down-conversion mode curve

Light-load Frequency Hopping

In addition to intelligent frequency reduction, the chip is also internally designed with frequency hopping mode and when the V_{EA_O} drops to 1.1V, the chip is in the burst mode, also known as frequency hopping mode. After the chip enters the burst operating mode, the chip turns off the GATE drive signal (SCM1725A internal signal), and since the output voltage drops due to load consumption, the feedback voltage drops, V_{EA_O} starts to rise again. When V_{EA_O} rises to 1.24V again, the chip jumps out of the burst operating mode, GATE (SCM1725A internal signal) starts to output pulse, the frequency remains at the minimum value (30kHz), and in order to avoid sound, the minimum frequency should be more than 22kHz. After outputting drive signal, the output voltage of power supply starts to pick up and if the product is still very light loaded or not loaded, it will go to burst operating mode again, forming a cycle (see Figure 3). This design aims to reduce the loss during light load and no-load, and also to prevent output overvoltage when the voltage feedback loop is normal.

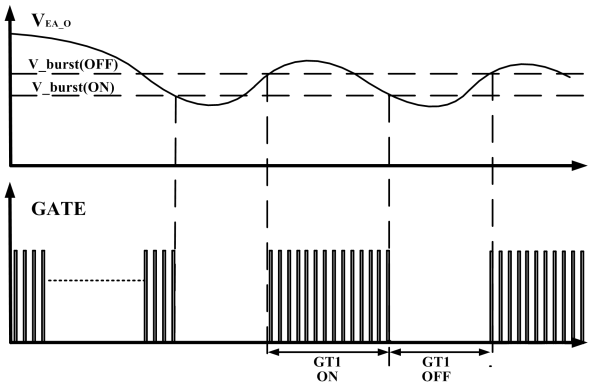


Figure 3 Light Load burst Mode

Built-in slope compensation

As single-stage compensation mechanism is applied, the slope is 78mV/us when the duty cycle is 42% ~ 77% and the operating frequency is 122kHz. This design improves the anti-interference performance and precision, and avoids the influence of carrying capacity. After slope compensation, the sub-harmonic oscillation can be prevented under the condition of large duty cycle.

CS fault protection

When the chip is used in high power supply, short circuit protection will cause relatively high power consumption and power MOS crack, since when the minimum lead time is fixed for short circuit protection, the primary side current will be deeply continuous, the larger the primary side current, the larger the leakage inductance energy will be. In the moment of power MOS turn-off, the larger voltage peak will result in power MOS crack. In order to prevent transformer saturation in deep continuous mode, it is necessary to take some measures, i.e. adding a 1.5V fast comparator at the CS terminal, to lock and shut off drive output and wait for restart when CS voltage exceeds 1.5V for 8 consecutive cycles.

Overload Protection (OLP)

V_{EA_O} will be further greater than 4.5V when overload (overpower), output short circuit or the disconnection of secondary side feedback loop occurs. If the V_{EA_O} is greater than 4.5V in 76ms consecutively (the time is timed by the internal timer, and once V_{EA_O} is less than 4.5V, the timer will re-count), then the case is deemed abnormal condition, accompanied with output short circuit/open loop protection and drive output stop. VDD capacitor cannot be supplied power by the output, and VDD voltage starts to drop and when the chip's VDD voltage drops to the VDD Turn-off Threshold, the chip retries to start and restart the soft-start process. If the above exception still exists and in the period of 76ms, the V_{EA_O} has been constantly higher than 4.5V, it will again enable the protection state and maintain the cycle continuously; If the exception has been excluded, the output voltage will be gradually established after starting a period of time, and feedback to EA's inverted input terminal through FB, so that the V_{EA_O} is lower than 4.5V, the chip will not be in the protection state, and can be started normally.

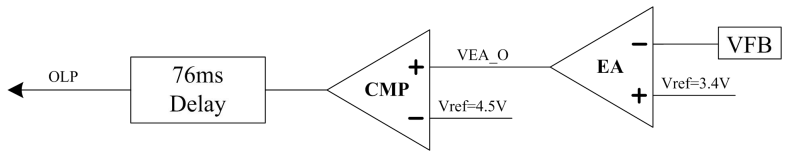


Figure 4 Architectural diagram of overpower protection

Schematic diagram

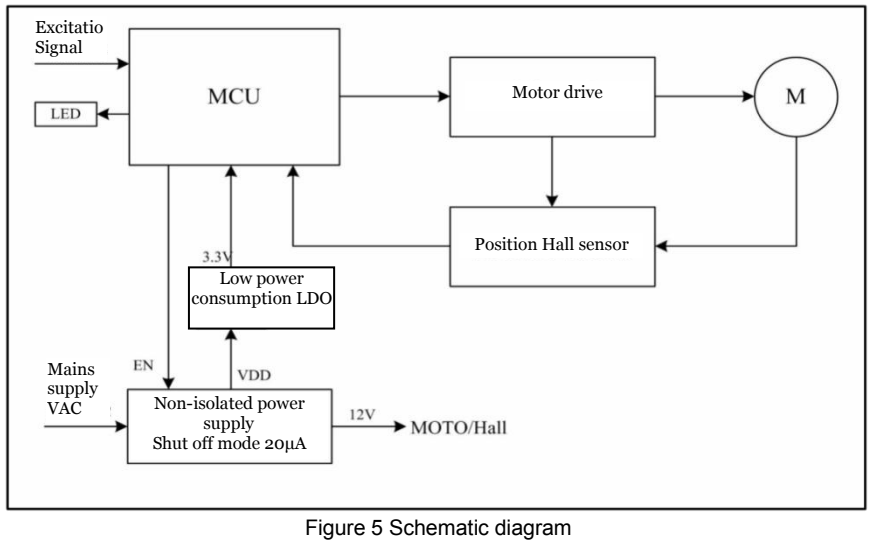


Figure 5 Schematic diagram

Suggestions of Power Use

EN pin is connected to the appropriate capacitor.

Ordering Information

Part number	Package	Number of pins	Silk Screen Marking	Reel information
SCM1725ASA	SOP-7	7	SCM 1725ASA YM	3K/pack

Product marking and date code

SCM1725XYZ

（1）SCM1725, product designation.

（2）X = A-Z, version code.

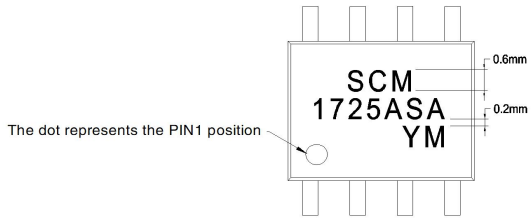
（3）Y = S, package definition code. S: SOP package.

（4）Z = C, I, A, M, Operating temperature range. C: 0℃-70℃, I: -40℃-85℃, A: -40℃-125℃, M: -55℃-125℃

Silk screen:

（5）YM:Date code for product traceability. Y = code for production year, M = code for production month

Silk Screen Information



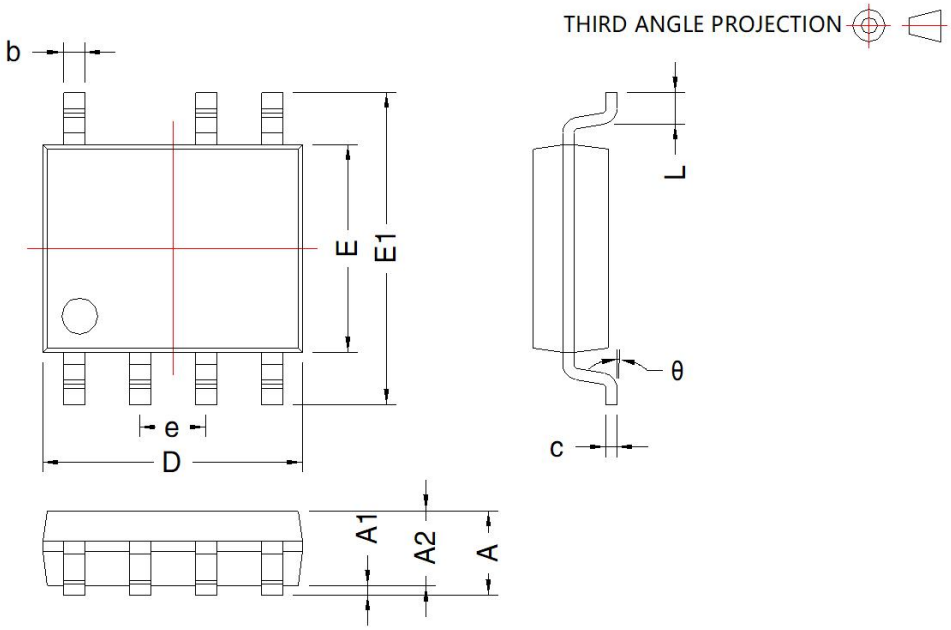
Note：

1、Typeface：Arial；

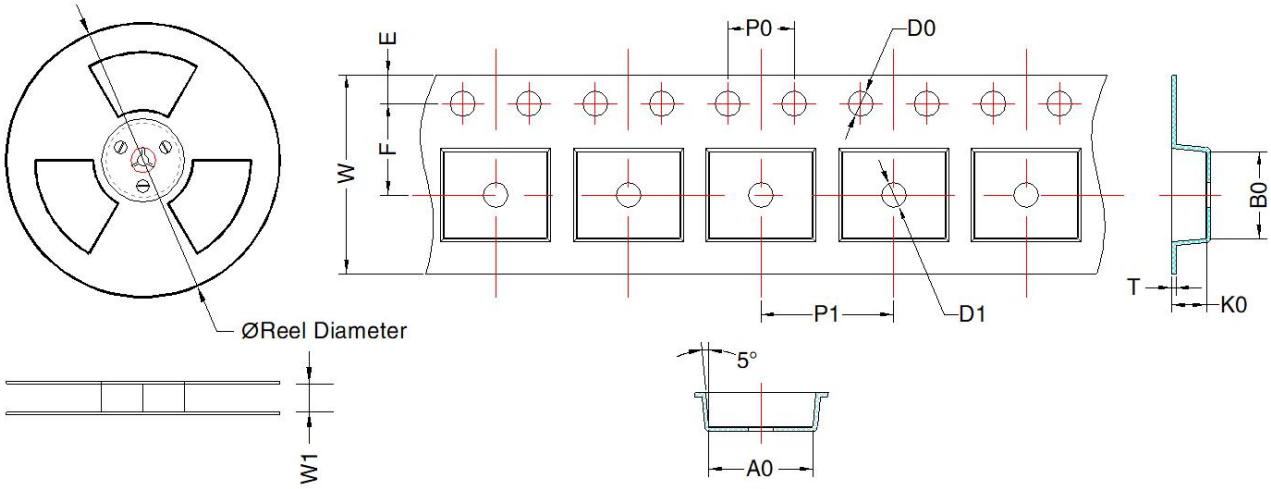
2、Character size：

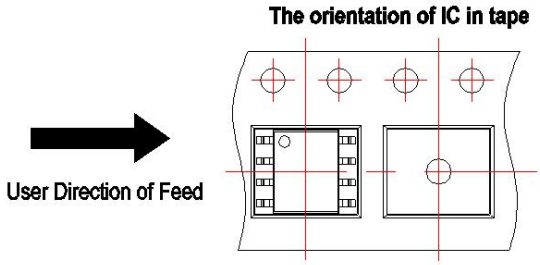
Height：0.6mm，Spacing：0.1mm，LineSpacing：0.2mm；

Packaging Information



SOP-7				
Mark	Dimension(mm)		Dimension(inch)	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.1	0.25	0.004	0.010
A2	1.35	1.55	0.053	0.061
D	4.7	5.1	0.185	0.201
E	3.8	4.0	0.150	0.157
E1	5.8	6.2	0.228	0.244
L	0.4	0.8	0.016	0.032
b	0.33	0.51	0.013	0.020
e	1.27TYP		0.05TYP	
c	0.17	0.25	0.007	0.010
θ	0°	8°	0°	8°





Device	Package Type	MPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	T (mm)	W (mm)	E (mm)	F (mm)	P1 (mm)	P0 (mm)	D0 (mm)	D1 (mm)
SCM1725ASA	SOP-7	3000	330.0	12.4	6.5 ± 0.2	5.45 ± 0.2	2.0 ± 0.2	0.3 ± 0.05	12.0 ± 0.3	1.75 ± 0.1	5.5 ± 0.1	8.0 ± 0.1	4 ± 0.1	1.5 ± 0.1	1.5 ± 0.1

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