National Semiconductor

CLC114
Quad, Low-Power Video Buffer

General Description

The CLC114 is a high-performance, closed-loop quad buffer intended for power sensitive applications. Requiring only 30mW of quiescent power dissipation per channel (±5V supplies), the CLC114 offers a small signal bandwidth of 200MHz ($0.5V_{pp}$) and a slew rate of 450V/μs.

Designed specifically for high density crosspoint switch and analog multiplexer applications, the CLC114 offers excellent linearity and wide channel isolation (62dB @ 10MHz). Driving a typical crosspoint switch load, the CLC114 offers differential gain and phase performance of 0.08% and 0.1%; gain flatness through 30MHz is typically 0.1dB.

With its patented closed-loop topology, the CLC114 has significant performance advantages over conventional open-loop designs. Applications requiring low output impedance and true unity gain stability through very high frequencies (active filters, dynamic load buffering, etc.) will benefit from the CLC114's superior performance.

Constructed using an advancd, complementary bipolar process and National's proven high-speed architectures, the CLC114 is available in several versions to meet a variety of requirements.

CLC114AJP	-40°C to +85°C	14-pin plastic DIP
CLC114AJE	-40°C to +85°C	14-pin plastic SOIC
CLC114ALC	-40°C to +85°C	dice
CLC114AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B
CLC114A8B	-55°C to +125°C	14-pin CERDIP, MIL-STD-883, Level B

DESC SMD number: 5962-92339

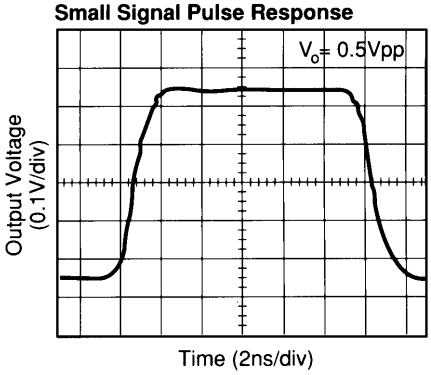
Features

- Closed-loop, quad buffer
- 200MHz small-signal bandwidth
- 450V/µs slew rate
- Low power, 30mW per channel (±5V sup.)
- 62dB channel isolation (10MHz)
- Specified for crosspoint switch loads

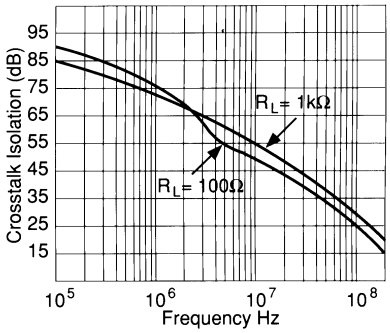
Applications

- Video crosspoint switch driver
- Video distribution buffers
- Video switching buffers
- Video signaling multiplexing
- Instrumentation amps
- Active filters

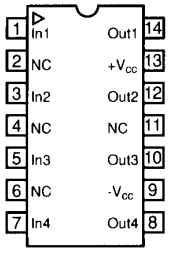
Small Signal Pulse Response



Typical Application



Pinout



CLC114 Electrical Characteristics (V_{cc} = ±5V, R_L = 100Ω unless specified)

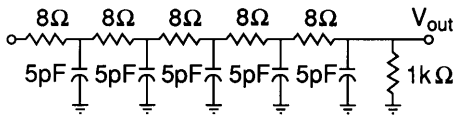
PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC114AI	+25°C	−40°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
−3dB bandwidth	V_{out}<0.5V_{pp}	200	>135	>135	>120	MHz	SSBW
	V_{out}<2V_{pp}	95	>70	>70	>70	MHz	LSBW
gain flatness	V_{out}<0.5V_{pp}						
peaking	DC to 30MHz	0.0	<0.3	<0.2	<0.3	dB	GFPL
peaking	30MHz to 200MHz	0.0	<1.3	<0.7	<0.7	dB	GFPH
rolloff	DC to 60MHz	0.1	<0.8	<0.8	<1.0	dB	GFR
crosstalk (all hostile)	10MHz	62	>58	>58	>60	dB	XT
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	1.8	<2.8	<2.8	<3.0	ns	TRS1
	2V step	5	<7	<7	<8	ns	TRS2
settling time to 0.1%	2V step	10	<15	<15	<20	ns	TS1
to 0.01%	2V step	20	<30	<30	<40	ns	TS01
overshoot	0.5V step	3	<15	<10	<15	%	OS
slew rate		450	>180	>200	>180	V/μs	SR
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 20MHz	−50	<−34	<−38	<−38	dBc	HD2
3rd harmonic distortion	2V_{pp}, 20MHz	−58	<−50	<−50	<−45	dBc	HD3
equivalent noise input							
noise floor	>1MHz	−155	<−153	<−153	<−153	dBm_{1Hz}	SNF
STATIC, DC PERFORMANCE							
small signal gain	100Ω load	0.97	>0.95	>0.96	>0.96	V/V	GA
integral endpoint linearity	±1V, full scale	0.4	<1.0	<0.6	<0.5	%	ILIN
*output offset voltage		±0.5	<±8.2	<±5.0	<±8.0	mV	VIO
average temperature coefficient		±9.0	<±40	—	<±30	μV/°C	DVIO
*input bias current		±1.0	<±10	<±5	<±4	μA	IBN
average temperature coefficient		±6.0	<±62	—	<±25	nA/°C	DIBN
power supply rejection ratio		56	>48	>48	>46	dB	PSRR
*supply current, total	no load, quiescent	12.0	<17.0	<16.5	<16.0	mA	ICC
MISCELLANEOUS PERFORMANCE							
input resistance		1.5	>0.3	>1.0	>2.0	MΩ	RIN
input capacitance		1.8	<3.5	<3.0	<3.5	pF	CIN
output impedance	DC	2.5	<5.0	<3.5	<3.5	Ω	RO
output voltage range	no load	±4.0	>±3.6	>±3.8	>±3.8	V	VO
output current		25	>12	>20	>25	mA	IO

Performance Driving a Crosspoint Swtich

PARAMETERS	CONDITIONS	TYP	UNITS
gain flatness V_{out}<2V_{pp}	DC to 5MHz	±0.02	dB
V_{out}<2V_{pp}	DC to 30MHz	±0.1	dB
differential gain	3.58 & 4.43MHz	0.08	%
differential phase	3.58 & 4.43MHz	0.1	°
2nd harmonic distortion	5MHz, 2V_{pp}	−60	dBc
	30MHz, 2V_{pp}	−43	dBc
3rd harmonic distortion	5MHz, 2V_{pp}	−58	dBc
	30MHz, 2V_{pp}	−43	dBc
crosstalk (all hostile)	5MHz	58	dB
	10MHz	54	dB
	30MHz	42	dB

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Test Load



Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	30mA
input voltage	±V_{cc}
maximum junction temperature	+150˚C
operating temperature range	
AJ:	–40˚C to + 85˚C
storage temperature range	–65˚C to + 150˚C
lead temperature (soldering 10 sec)	+300˚C
EDS rating	500V

Miscellaneous Ratings

NOTES:

* AJ 100% tested at +25˚C.

Package Thermal Resistance

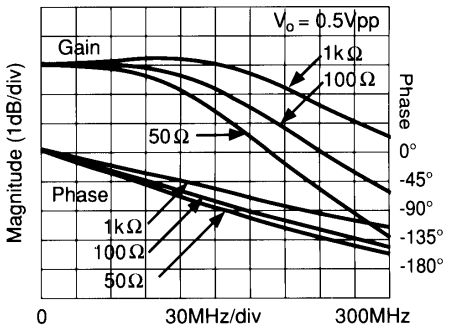
Package	θ_{JC}	θ_{JA}
Plastic (AJP)	65°C/W	115°C/W
Surface Mount (AJE)	55°C/W	125°C/W
CERDIP	35°C/W	90°C/W

Reliability Information

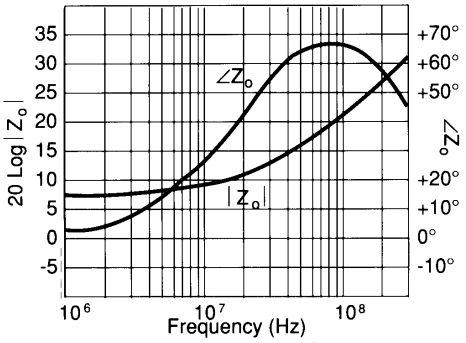
Transistor Count	64

CLC114 Typical Performance Characteristics

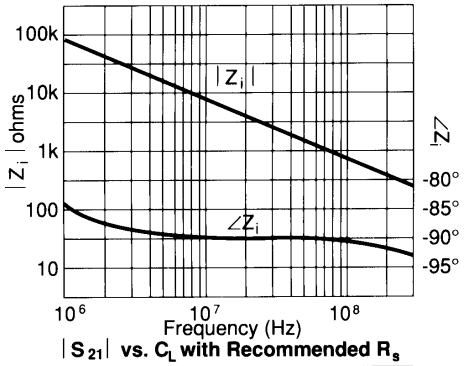
Gain and Phase vs. Load



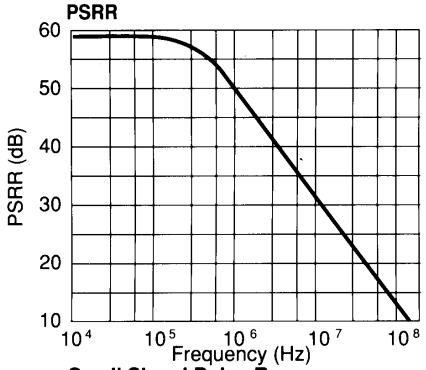
Output Impedance



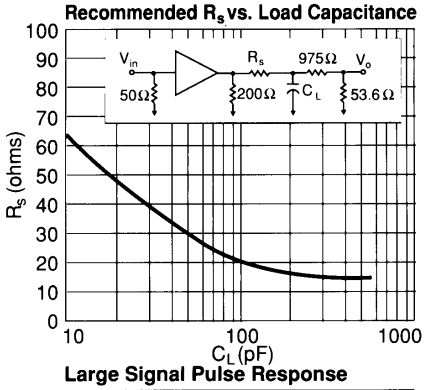
Input Impedance



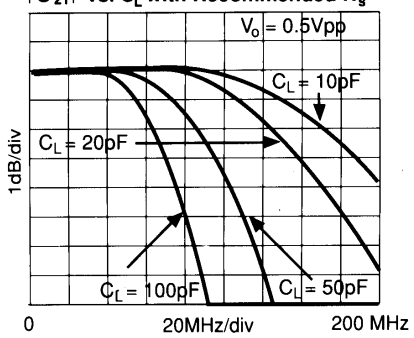
PSRR



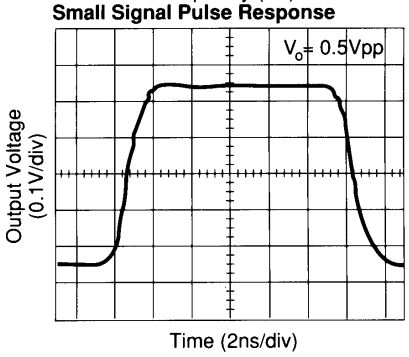
Recommended R_s vs. Load Capacitance



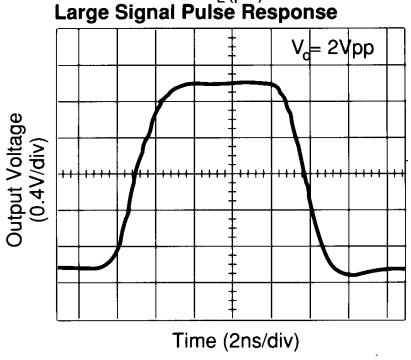
|S_{21}| vs. C_L with Recommended R_s



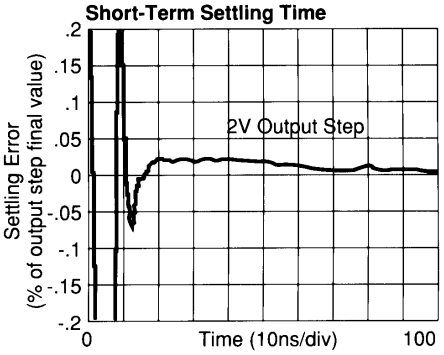
Small Signal Pulse Response



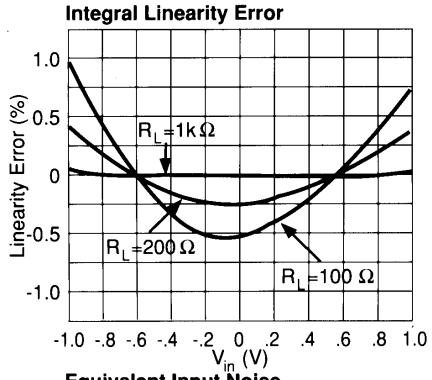
Large Signal Pulse Response



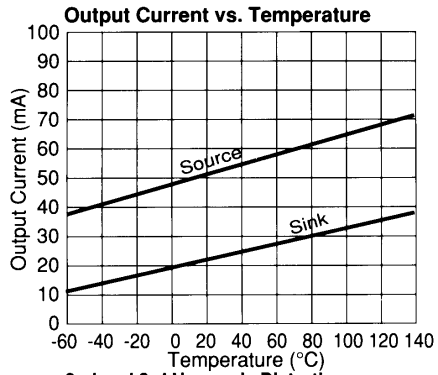
Short-Term Settling Time



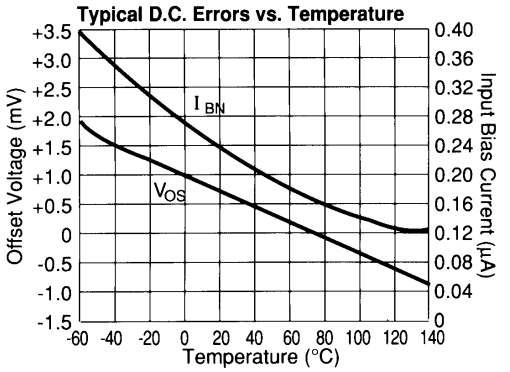
Integral Linearity Error



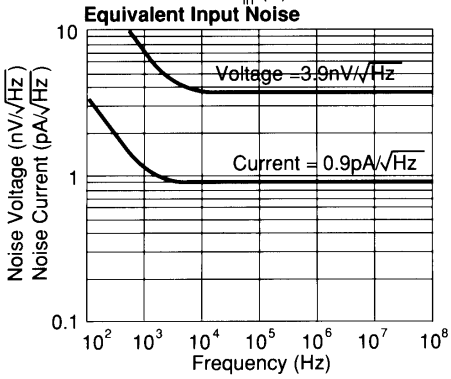
Output Current vs. Temperature



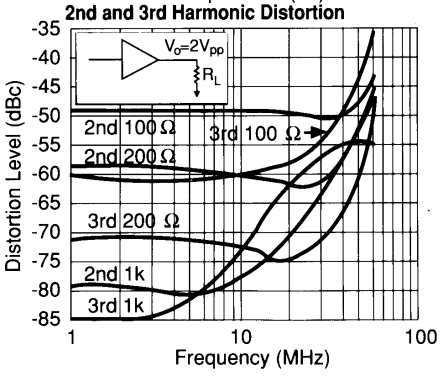
Typical D.C. Errors vs. Temperature



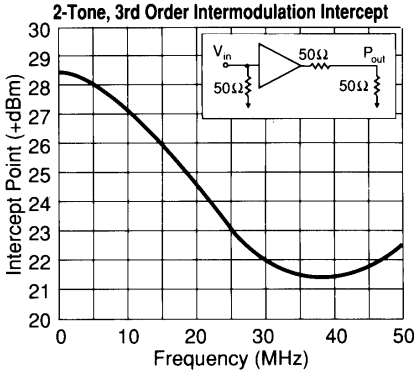
Equivalent Input Noise



2nd and 3rd Harmonic Distortion



2-Tone, 3rd Order Intermodulation Intercept



Operation

The CLC114 is a quad, low-power, high-speed, unity-gain buffer. The closed loop topology provides accuracy not found in open loop designs. The input stage incorporates a slew-enhancement circuit which allows low quiescent power without sacrificing ac performance.

PC Board Layout and Crosstalk

High frequency devices demand a good printed circuit board layout for optimum performance. The CLC114, with power gain to 200 MHz, is no exception. A ground plane and power supply bypassing with good high-frequency ceramic capacitors in close proximity to the supply pins is essential. Second harmonic distortion can be improved by ensuring equal current return paths for both the positive and the negative supplies. This can be accomplished by grounding the bypass capacitors at the same point in the ground plane while keeping the power supply side of the bypass capacitors within 0.1" of the CLC114 supply pins.

Crosstalk (undesired signal coupling between buffer channels) is strongly dependent on board layout. Closely spaced signal traces on the circuit board will degrade crosstalk due to intertrace capacitance. For this reason it is recommended that unused package pins (2, 4, 6, 11) be connected to the ground plane for better channel isolation at the device pins. Similarly, crosstalk can be improved by using a grounded guard trace between signal traces. This will reduce the distributed capacitance between signal lines.

Following are two graphs depicting the effects of crosstalk. All-hostile crosstalk is measured by driving three of the four buffers simultaneously while observing the fourth, undriven, channel. Figure 2, "All-Hostile Crosstalk Isolation", shows this effect as a function of input signal frequency. R_L is the resistive load for each driven channel. Figure 3, "Most Susceptible Channel-to-Channel Pulse Coupling", describes one effect of crosstalk when one channel is driven with a 2Vpp step (tr = 5ns) while the output of the undriven channel is measured. From Figure 2 it can be observed that crosstalk decreases as the signal frequency is reduced. Similarly, the pulse coupling crosstalk will decrease as the rise time increases.

Evaluation Board

An evaluation board for the CLC114 is available. This board may be ordered as part CLC730023.

Unused Buffers

It is recommended that the inputs of any unused buffers be tied to ground through 50Ω resistors.

Differential Gain and Phase

The CLC114 was designed to minimize differential gain and phase errors when driving the distributed capacitance of a video crosspoint switch. Refer to the section "Performance Driving a Crosspoint Switch" for typical values.

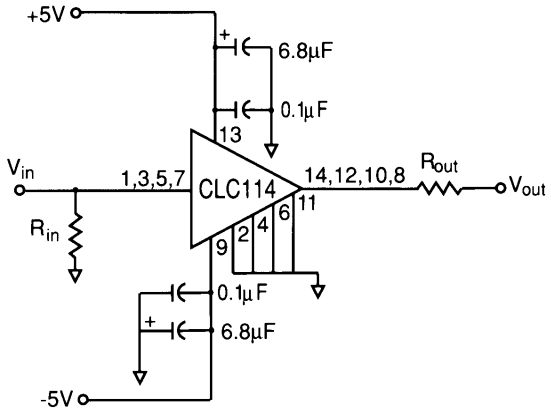


Figure 1: Recommended Circuit

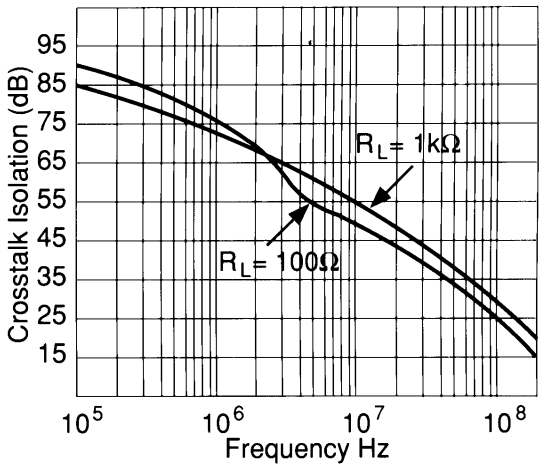


Figure 2: All-Hostile Crosstalk Isolation

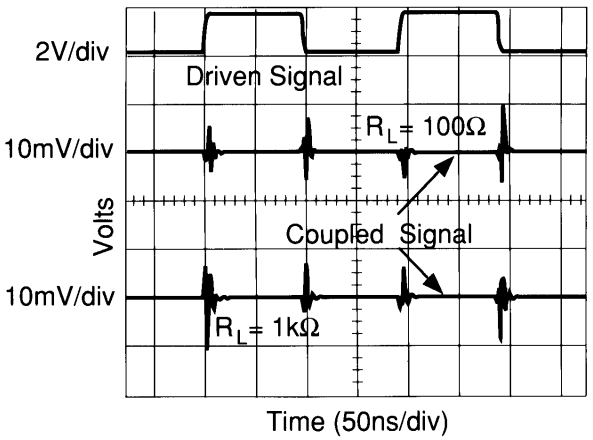


Figure 3: Most Susceptible Channel-to-Channel Pulse Coupling

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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