National Semiconductor

Comlinear CLC436
200MHz, ±15V, Low-Power Voltage Feedback Op Amp

General Description

The Comlinear CLC436 is a high-performance, low power, voltage-feedback operational amplifier that has been designed for a wide range of low-cost applications. The CLC436 is specified to operate from dual ±5V to dual ±15V power supplies. Operating from ±5V supplies, the unity gain stable CLC436 consumes a mere 23mW of power and features a 150MHz bandwidth and 850V/µs slew rate. Operating from ±15V power supplies, the CLC436 consumes only 69mW (I_{cc} = 2.3mA) to provide a 200MHz unity-gain bandwidth, a very fast 2400V/µs slew rate and 13ns rise/fall times (5V step). At ±15V, the device also provides large signal swings (>20V_{pp}) to give high dynamic range and signal-to-noise ratio.

As a low-power NTSC or PAL video line-driver, the CLC436 delivers low differential gain and phase errors (0.2%, 1.2°) and very high output drive current of 80mA. When used as a video ADC driver, the CLC436 offers low Total Harmonic Distortion (THD) and high Spurious Free Dynamic Range (SFDR). Because of it's voltage feedback topology, the CLC436 allows use of reactive elements in the feedback path and can be configured as an excellent active filter for video-reconstruction DACs.

The CLC436's combination of low cost and high performance in addition to its low-power voltage-feedback topology make it a versatile signal conditioning building block for a wide range of price-sensitive applications.

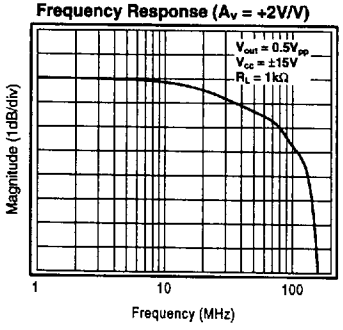
Features

- 2.3mA supply current
- 200MHz unity-gain bandwidth
- 2400V/µs slew rate
- Unity gain stable
- 110dB common-mode rejection ratio
- 80mA drive current
- >20V_{pp} output swing
- ±5V to ±15V supplies

Applications

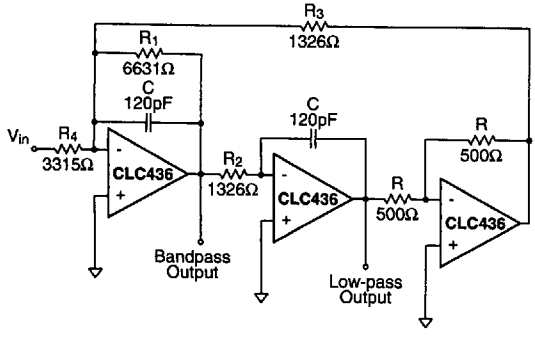
- Video line driver
- Video ADC driver
- Desktop Multimedia
- Low powered cable driver
- Video DAC buffer
- Active filters/integrators
- NTSC & PAL video systems

Frequency Response (A_v = +2V/V)

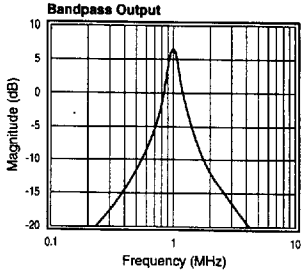


Typical Application

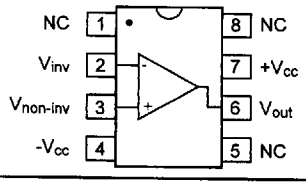
State-Variable Filter (1MHz, Q = 5, G = 2)



Bandpass Output



Pinout
DIP & SOIC



CLC436 Electrical Characteristics (V_{CC} = ±15V, A_V = +2, R_f = 499Ω, R_L = 1kΩ; unless specified)

PARAMETERS	CONDITIONS	V_{CC}	TYP	MIN/MAX RATINGS			UNITS	NOTES
	CLC436AJ		25°	25°	0° to +70°	-40° to +85°		
FREQUENCY DOMAIN RESPONSE								
-3dB bandwidth	V_{out} < 0.5V_{pp} (AJP)	±15, ±5	96,55	50	50	50	MHz	B
	V_{out} < 0.5V_{pp} (AJE)	±15, ±5	96,55	50	60	40	MHz	B
	V_{out} < 10V_{pp}		25	21	20	16	MHz	
-3dB bandwidth A_V = +1	V_{out} < 0.5V_{pp}, R_f = 0	±15, ±5	200,150				MHz	
gain flatness	V_{out} < 0.5V_{pp}							
rolloff	DC to 20MHz		0.6	1.2	1.2	1.2	dB	B
peaking	DC to 10MHz		0	0.03	0.03	0.03	dB	B
linear phase deviation	DC to 10MHz		0.5				deg	
differential gain	4.43MHz, R_L=150Ω		0.2				%	
differential phase	4.43MHz, R_L=150Ω		1.2				deg	
gain bandwidth product	V_{out} < 2.0V_{pp}	±15, ±5	200,100				MHz	
TIME DOMAIN RESPONSE								
rise and fall time	2V step, t_r(in) = 5ns		11	13	14	18	ns	
	5V step, t_r(in) = 5ns		13	16	18	20	ns	
settling time to 0.05%	2V step, t_r(in) = 5ns	±15, ±5	36,48	42	65	85	ns	
overshoot	2V step, t_r(in) = 5ns		0.5	1	2	2	%	
slew rate	5V step, t_r(in) = 5ns	±15, ±5	2400,850	2000	1900	1600	V/µs	
DISTORTION AND NOISE RESPONSE								
2nd harmonic distortion	1V_{pp}, 1MHz		-72	-65	-62	-62	dBc	
3rd harmonic distortion	1V_{pp}, 1MHz		-70	-62	-60	-60	dBc	
2nd harmonic distortion	1V_{pp}, 5MHz		-65	-56	-56	-53	dBc	B
3rd harmonic distortion	1V_{pp}, 5MHz		-63	-54	-54	-54	dBc	B
input voltage noise	@1kHz		11	12.6	13.5	14.1	nV/√Hz	
current noise	@1kHz		0.8	1.5	1.9	2.3	pA/√Hz	
STATIC DC PERFORMANCE								
input offset voltage		±15, ±5	1.5,1.5	5	5	5	mV	A
average drift			6	–	40	70	µV/°C	
input bias current		±15, ±5	1,1.2	3	3	4	µA	A
average drift			4	–	50	70	nA/°C	
input offset current		±15, ±5	0.1,0.1	1	1	3	µA	A
power supply rejection ratio	DC		95	75	75	75	dB	B
common-mode rejection ratio	DC		110	75	73	70	dB	
supply current	R_L= ∞		2.3	4	4	4	mA	A
open loop gain		±15, ±5	85,80				dB	
MISCELLANEOUS PERFORMANCE								
input resistance	common-mode		40	20	15	10	MΩ	
input capacitance	common-mode		2	3	3	5	pF	
input resistance	differential-mode		4.9	4.0	3.0	2.5	MΩ	
input voltage range	common-mode	±15	±12	±11	±10.5	±10	V	
input voltage range	common-mode	±5	±3				V	
output voltage range	R_L = 100Ω	±15	+11.6/-10.5	+8.5/-8.5	+8.5/-8.5	+8.5/-8.5	V	
	R_L = ∞	±15	+13/-12.2	+12/-12	+12/-12	+12/-12	V	
output voltage range	R_L = 100Ω	±5	±2.8				V	
	R_L = ∞	±5	±3.4				V	
output resistance, closed loop			0.01	0.05	0.07	0.1	Ω	
output current sourcing		±15, ±5	120,90	100	95	90	mA	
output current sinking		±15, ±5	80,40	75	70	65	mA	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

supply voltage	±18.0V
maximum junction temperature	+150°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+260°C

Notes

A) J-level: spec is 100% tested at +25°C, sample tested at +85°C.
B) J-level: spec is sample tested at +25°C.

Ordering Information

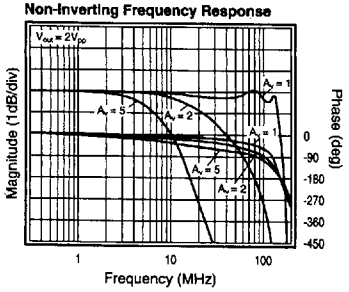
Model	Temperature Range	Description
CLC436AJP	-40°C to +85°C	8-pin PDIP
CLC436AJE	-40°C to +85°C	8-pin SOIC

Package Thermal Resistance

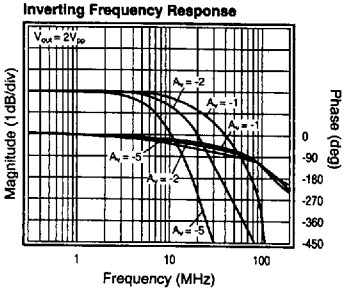
Package	θ_{JC}	θ_{JA}
Plastic (AJP)	90°C/W	105°C/W
Surface Mount (AJE)	120°C/W	140°C/W

CLC436 Typical Performance Characteristics (V_{cc} = ±15V, A_V = +2, R_f = 499Ω, R_L = 1kΩ; unless specified)

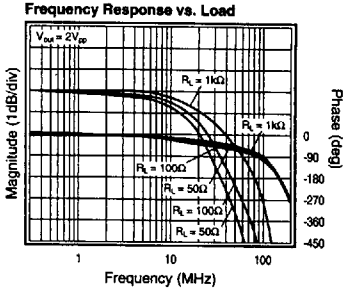
Non-Inverting Frequency Response



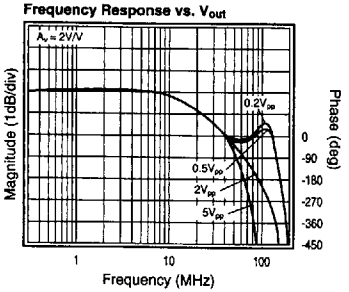
Inverting Frequency Response



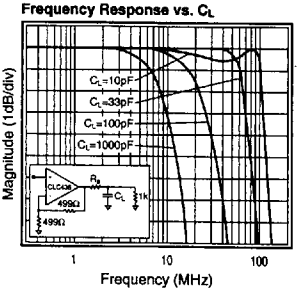
Frequency Response vs. Load



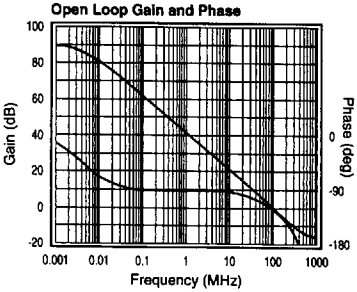
Frequency Response vs. V_{out}



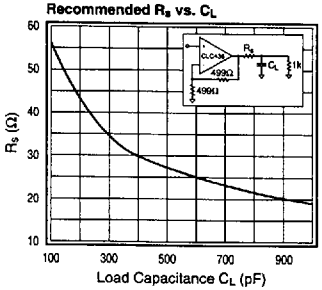
Frequency Response vs. C_L



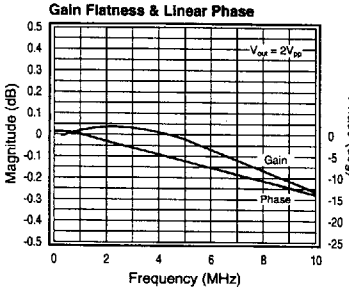
Open Loop Gain and Phase



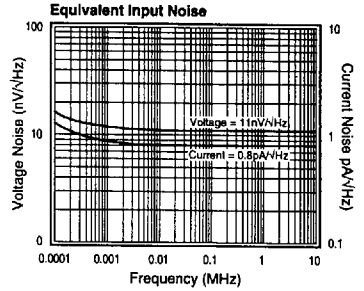
Recommended R_s vs. C_L



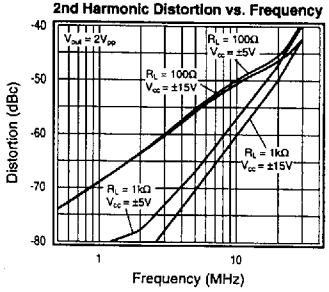
Gain Flatness & Linear Phase



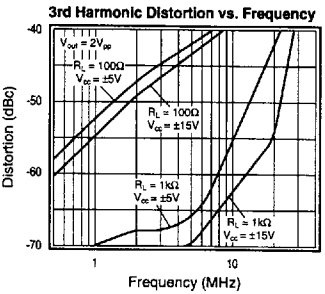
Equivalent Input Noise



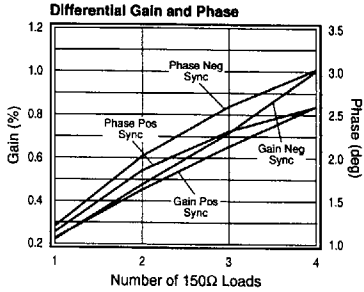
2nd Harmonic Distortion vs. Frequency



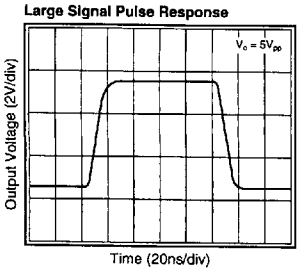
3rd Harmonic Distortion vs. Frequency



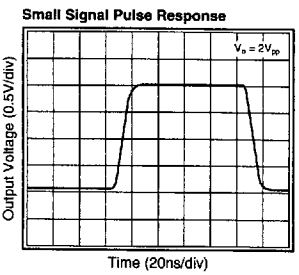
Differential Gain and Phase



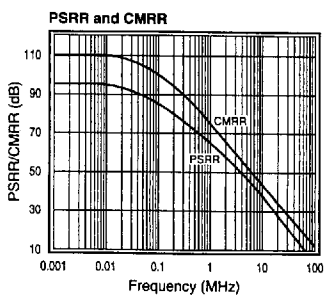
Large Signal Pulse Response



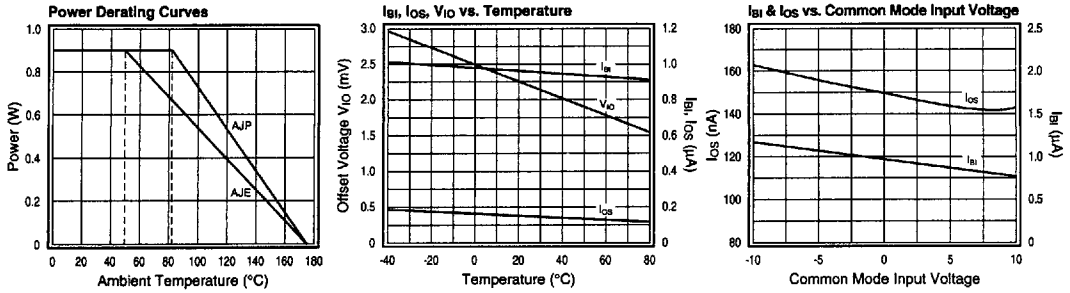
Small Signal Pulse Response



PSRR and CMRR



CLC436 Typical Performance Characteristics (V_{cc} = ±15V, A_v = +2, R_f = 499Ω, R_L = 1kΩ; unless specified)



CLC436 OPERATION

Description

The CLC436 is a unity gain stable voltage feedback amplifier. The voltage feedback topology allows for capacitors and nonlinear devices in the feedback path. The matched input bias currents track well over temperature. This allows the DC offset to be minimized by matching the impedance seen by both inputs.

The low cost, low power, conventional topology, and high output current make the CLC436 an excellent choice for applications such as:

- Low Power Cable Drivers
- Active Filters
- Buffers
- NTSC and PAL Video Systems

Gain

The non-inverting and inverting gain equations for the CLC436 are as follows:

Non-inverting Gain: $1+\frac{R_f}{R_g}$

Inverting Gain: $-\frac{R_f}{R_g}$

Where R_f is the feedback resistor and R_g is the gain setting resistor. Figure 1 shows the general non-inverting gain configuration including the recommended bypass capacitors.

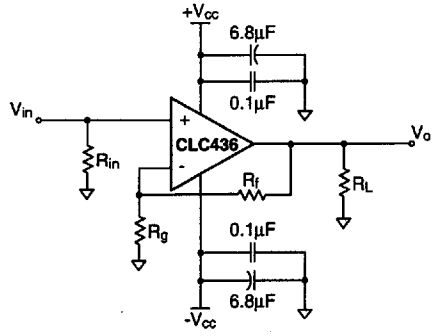


Figure 1: Recommended Non-Inverting Gain Circuit

Output Drive Performance

The CLC436 can source over 120mA of output current. It can easily drive $9V_{pp}$ into a 50Ω load. The circuit shown in Figure 1 demonstrates the output current capability of the CLC436. The circuit values listed below, a $3V_{pp}$ input signal and ±15V supplies, were used to obtain the result shown in Figure 2.

- R_f = 499Ω
- R_L = 50Ω
- R_g = 249.5Ω
- R_{in} = 50Ω

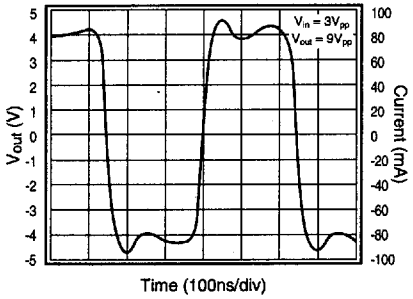


Figure 2: Large Signal Pulse Response into 50Ω

The high output drive capability of the CLC436 is suitable for driving capacitive loads. When driving a capacitive load or coaxial cable, include a series resistance R_s to improve stability. Refer to the ***R_s vs Capacitive Load*** plot in the typical performance section to determine the recommended resistance for various capacitive loads.

Single Supply Operation

The CLC436 can be operated from a single supply using the topology shown in Figure 3. R_1 and R_2 form a voltage divider that sets the non-inverting input DC voltage. The coupling capacitor C1 isolates the DC bias point from the previous stage. The DC gain of this circuit is 1 and the high frequency gain is set by R_f and R_g.

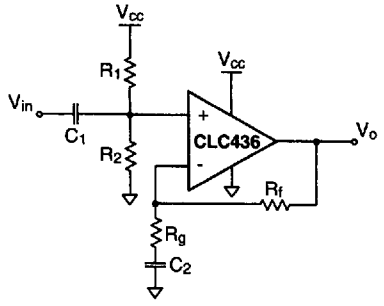


Figure 3: Single Supply Circuit

Power Dissipation

The power dissipation of an amplifier can be described in two conditions:

- Quiescent Power Dissipation - P_Q (No Load Condition)
- Total Power Dissipation - P_T (with Load Condition)

The following steps can be taken to determine the power consumption of the CLC436:

1. Determine the quiescent power
   $P_Q = I_{cc} (V_{cc} - V_{ee})$
2. Determine the RMS power at the output stage
   $P_O = (V_{cc} - V_{load}) (I_{load})$
3. Determine the total RMS power
   $P_T = P_Q + P_O$

The maximum power that the package can dissipate at a given temperature is illustrated in the ***Power Derating*** plot in the ***Typical Performance Characteristics*** section. The power derating curve for any package can be derived by utilizing the following equation:

$$P = \frac{(175° - T_{amb})}{\theta_{JA}}$$

where: T_{amb} = Ambient temperature in °C
θ_{JA} = Thermal resistance, from junction to ambient, for a given package in °C/W

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. Comlinear provides evaluation boards for the CLC436 (730013 - DIP, 730027-SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

Supply bypassing is required for optimum performance. The bypass capacitors provide a low impedance current return path at the supply pins. They also provide high frequency filtering on the power supply traces. Other layout factors also play a major role in high frequency performance. The following steps are recommended as a basis for high frequency layout:

1. Include 6.8µF tantalum and 0.01µF ceramic bypass capacitors on both supplies.
2. Place the 6.8µF capacitors within 0.75 inches of the power pins.
3. Place the 0.01µF capacitors within 0.1 inches of the power pins.
4. Remove the ground plane near the input and output pins to reduce parasitic capacitance.
5. Minimize all trace lengths to reduce series inductances.

Applications Circuit

State Variable Filter

The filter shown on the front page offers both a band-pass and a low pass output. The design equations are shown below.

$$Q = \frac{R_1}{R_3}$$

$$A_V = \frac{R_1}{R_4}, \text{ desired mid-band gain}$$

$$f_r = \frac{Q}{2\pi R_1 C}, \text{ desired resonant frequency}$$

$$R_2 = R_3$$

The state variable filter can be modified to obtain a tunable band pass filter. This technique is shown in the CLC522, Wideband Variable Gain Amplifier, data sheet.

Transimpedance Application

The low 1.1pA/√Hz input current noise and unity gain stability make the CLC436 useful as a photo diode pre-amplifier. Figure 4 illustrates a transimpedance amplifier. R_f sets the transimpedance gain. The photodiode current is multiplied by R_f to determine the output voltage.

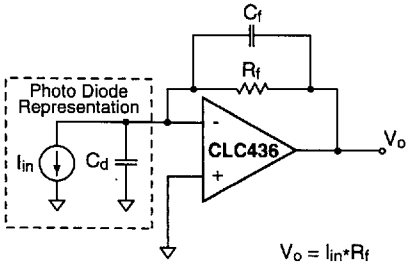


Figure 4: Transimpedance Amplifier

The feedback capacitor (C_f) is required to compensate for the added input capacitance of the photodiode (C_d). The feedback capacitance reduces peaking in the frequency response. As the value of the feedback capacitance increases from zero, the rolloff of the response will increase.

Instrumentation Amplifier

An instrumentation circuit is shown in Figure 5. The high CMRR of the CLC436 benefits this application. The resistors are kept equal to improve the overall CMRR.

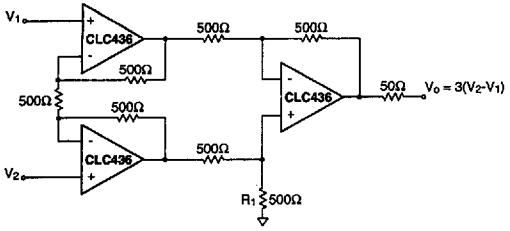


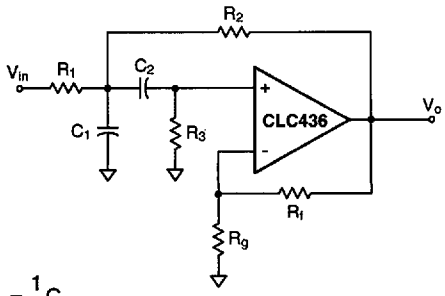
Figure 5: Instrumentation Amplifier

2nd Order Sallen-Key Band-Pass Filter

The CLC436 is well suited for Sallen-Key type active filters. Figure 6 illustrates the band pass topology and design equations. For optimum high frequency performance:

- Keep the resistor values between 10Ω and 1kΩ
- Keep the capacitor values between 10pF and 500pF

Begin design by choosing reasonable values for C_1 and C_2 and then setting the desired mid-band gain.



$$C_2 = \frac{1}{5}C_1$$

$$G = 1 + \frac{R_f}{R_g}, \text{ desired mid-band gain}$$

$$R_1 = 2\frac{Q}{GC_1(2\pi f)}, \text{ where } f = \text{desired center frequency}$$

$$R_2 = \frac{GR_1\left(\sqrt{1+4.8Q^2-2G+G^2}+1\right)}{4.8Q^2-2G+G^2}$$

$$R_3 = \frac{5GR_1\left(\sqrt{1+4.8Q^2-2G+G^2}+G-1\right)}{4Q^2}$$

Figure 6: Sallen-Key Active Filter