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Kind regards,

Team Nexperia

# 74LV165A

## 8-bit parallel-in/serial-out shift register

Rev. 4 — 28 March 2014

Product data sheet

### 1. General description

The 74LV165A is an 8-bit parallel-load or serial-in shift register with complementary serial outputs ( $Q_7$  and  $\overline{Q_7}$ ) available from the last stage. When the parallel-load input ( $\overline{PL}$ ) is LOW, parallel data from the inputs D0 to D7 are loaded into the register asynchronously. When input  $\overline{PL}$  is HIGH, data enters the register serially at the input DS. It shifts one place to the right ( $Q_0 \rightarrow Q_1 \rightarrow Q_2$ , etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the output  $Q_7$  to the input DS of the succeeding stage.

The clock input is a gate-OR structure which allows one input to be used as an active LOW clock enable input ( $\overline{CE}$ ) input. The pin assignment for the inputs CP and  $\overline{CE}$  is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of the input  $\overline{CE}$  should only take place while CP HIGH for predictable operation.

Schmitt-trigger action at all inputs, makes the circuit tolerant for slower input rise and fall times. It is fully specified for partial-power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging current backflow through the device when it is powered down.

### 2. Features and benefits

- Wide supply voltage range from 2.0 V to 5.5 V
- Synchronous parallel-to-serial applications
- Synchronous serial input for easy expansion
- Latch-up performance exceeds 250 mA
- CMOS LOW power consumption
- 5.5 V tolerant inputs/outputs
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Complies with JEDEC standards:
  - ◆ JESD8-5 (2.3 V to 2.7 V)
  - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
  - ◆ JESD8-1A (4.5 V to 5.5 V)
- ESD protection:
  - ◆ HBM JESD22-A114-A exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$



### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LV165AD	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV165APW	-40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

### 4. Functional diagram

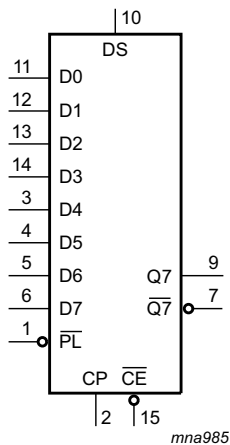


Fig 1. Logic symbol

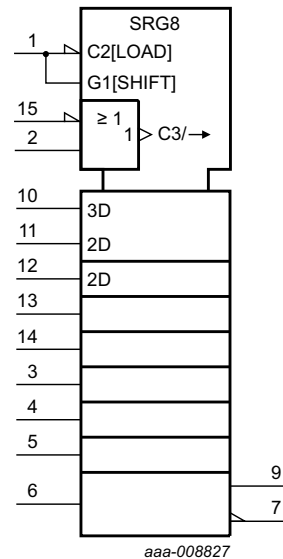


Fig 2. IEC logic symbol

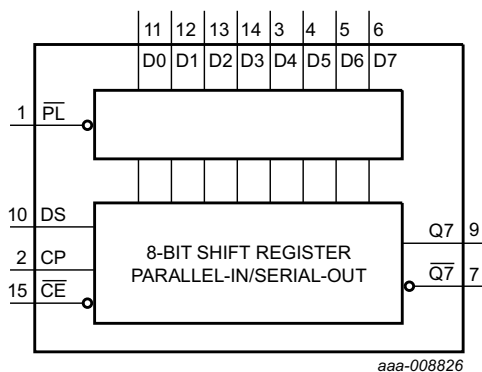


Fig 3. Functional diagram

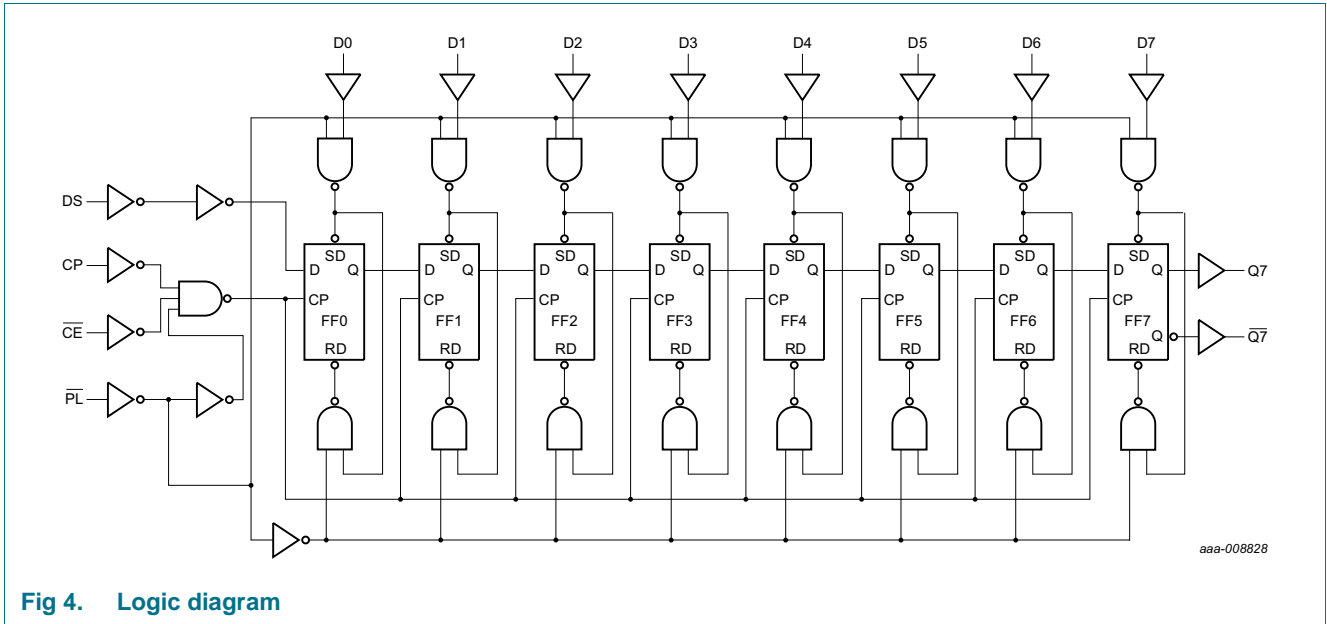


Fig 4. Logic diagram

## 5. Pinning information

### 5.1 Pinning

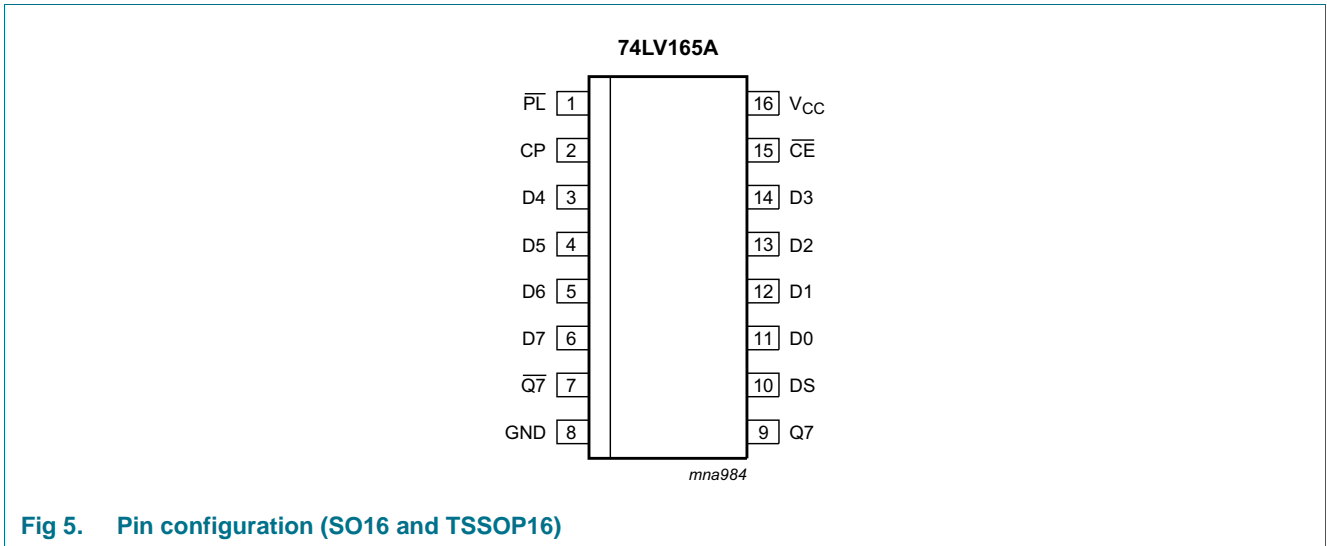


Fig 5. Pin configuration (SO16 and TSSOP16)

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{PL}$	1	parallel enable input (active LOW)
CP	2	clock input (LOW-to-HIGH edge-triggered)
$\overline{Q7}$	7	complementary serial output from the last stage
GND	8	ground (0 V)
Q7	9	serial output from the last stage
DS	10	serial data input
D0 to D7	11, 12, 13, 14, 3, 4, 5, 6	parallel data inputs
$\overline{CE}$	15	clock enable input (active LOW)
V <sub>CC</sub>	16	positive supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating modes	Inputs					Qn registers		Output	
	$\overline{\text{PL}}$	$\overline{\text{CE}}$	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	$\overline{\text{Q7}}$
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{\text{q6}}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{\text{q6}}$
	H	↑	L	l	X	L	q0 to q5	q6	$\overline{\text{q6}}$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{\text{q6}}$
hold "do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{\text{q7}}$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{\text{q7}}$

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
 q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;  
 X = don't care;  
 ↑ = LOW-to-HIGH clock transition.

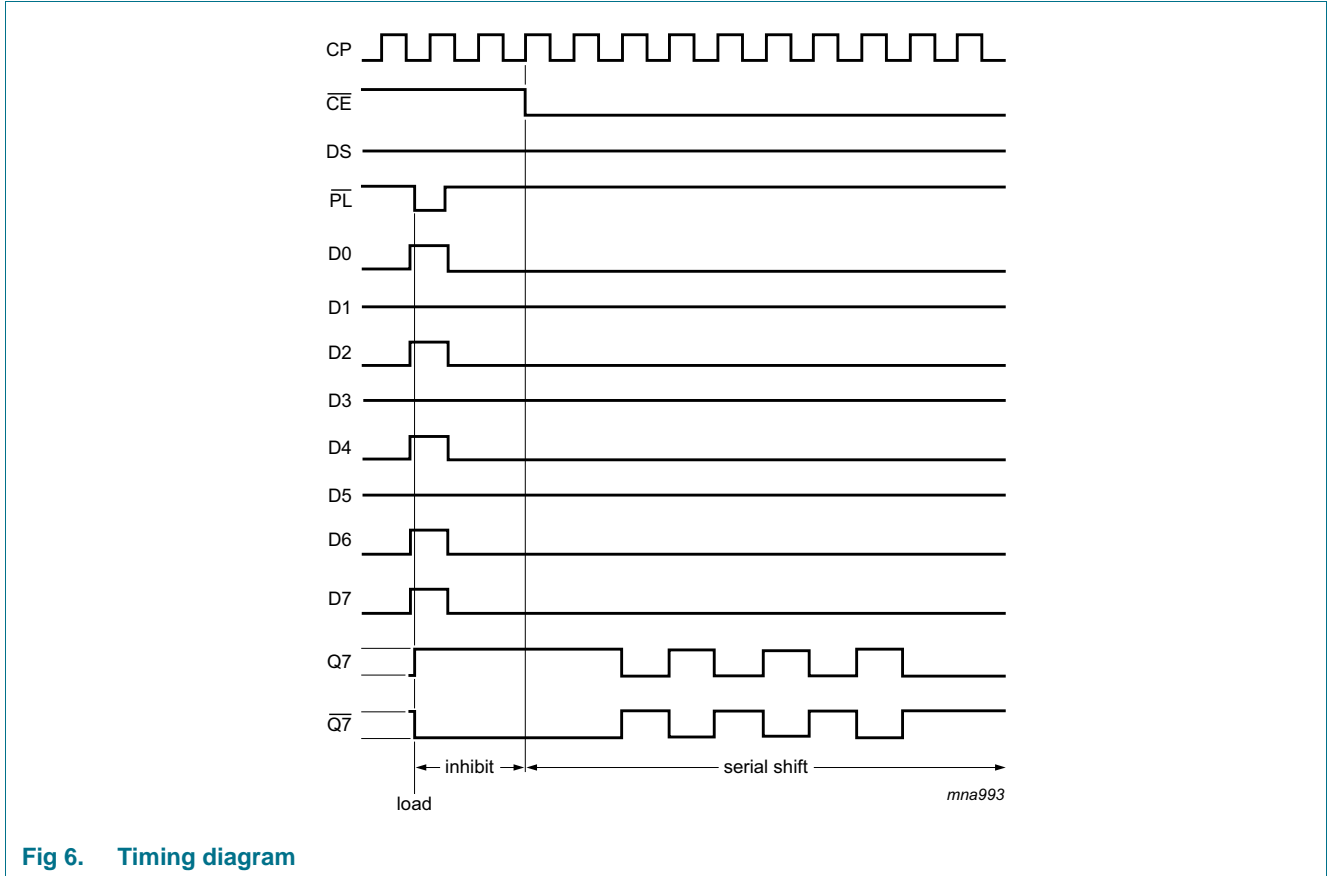


Fig 6. Timing diagram

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-	-20	mA
V <sub>I</sub>	input voltage		-0.5	+7	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	-	±50	mA
V <sub>O</sub>	output voltage		-0.5	V <sub>CC</sub> + 0.5	V
		power-down mode	-0.5	+7	V
I <sub>O</sub>	output current	0 V < V <sub>O</sub> < V <sub>CC</sub>	-	±25	mA
I <sub>CC</sub>	supply current		-	+50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C			
		SO16 package <sup>[2]</sup>	-	500	mW
		TSSOP16 package <sup>[3]</sup>	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

[3] P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		2.0	-	5.5	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V	0	-	200	ns/V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0	-	100	ns/V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.7V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7V <sub>CC</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.3V <sub>CC</sub>	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.3V <sub>CC</sub>	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V to 5.5 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -2.0 mA; V <sub>CC</sub> = 2.3 V	2.0	-	-	V
		I <sub>O</sub> = -6.0 mA; V <sub>CC</sub> = 3.0 V	2.48	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 4.5 V	3.8	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V to 5.5 V	-	-	0.10	V
		I <sub>O</sub> = 2.0 mA; V <sub>CC</sub> = 2.3 V	-	-	0.40	V
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.44	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 4.5 V	-	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	±0.01	±1	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0.0 V	-	±0.05	±5	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	0.2	20	μA
C <sub>I</sub>	input capacitance		-	3.0	-	pF



## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**
*GND (ground = 0 V); for test circuit, see [Figure 12](#)*

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit	
			Min	Typ <sup>[1]</sup>	Max		
t <sub>pd</sub>	propagation delay	CE, CP to Q7, Q7; C <sub>L</sub> = 15 pF; see <a href="#">Figure 7</a> and <a href="#">Figure 8</a>					
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	1.0	11.0	22.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	1.0	7.5	18.0	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	[5]	1.0	5.5	11.5	ns
		PL to Q7, Q7; C <sub>L</sub> = 15 pF; see <a href="#">Figure 8</a>					
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	1.0	11.5	23.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	1.0	8.0	18.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	[5]	1.0	5.5	11.5	ns
		D7 to Q7, Q7; C <sub>L</sub> = 15 pF; see <a href="#">Figure 9</a>					
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	1.0	12.0	24.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	1.0	8.5	16.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	[5]	1.0	6.0	10.5	ns
		CE, CP to Q7, Q7; see <a href="#">Figure 7</a> and <a href="#">Figure 8</a>					
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	1.0	13.0	26.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	1.0	9.0	21.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	[5]	1.0	6.1	13.5	ns
		PL to Q7, Q7; see <a href="#">Figure 8</a>					
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	1.0	14.0	28.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	1.0	10.0	22.0	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	[5]	1.0	6.5	13.5	ns
D7 to Q7, Q7; see <a href="#">Figure 9</a>							
V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	1.0	14.0	28.0	ns		
V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	1.0	10.0	20	ns		
V <sub>CC</sub> = 4.5 V to 5.5 V	[5]	1.0	6.5	12.5	ns		
t <sub>w</sub>	pulse width	CP input HIGH to LOW; see <a href="#">Figure 7</a>					
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	9.0	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	7.0	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	[5]	4.0	-	-	ns
		PL input LOW; see <a href="#">Figure 8</a>					
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	13.0	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	9.0	-	-	ns
V <sub>CC</sub> = 4.5 V to 5.5 V	[5]	6.0	-	-	ns		
t <sub>rec</sub>	recovery time	PL to CP, CE; see <a href="#">Figure 8</a>					
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	8.5	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	6.0	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	[5]	4.0	-	-	ns

**Table 7. Dynamic characteristics ...continued**  
 GND (ground = 0 V); for test circuit, see [Figure 12](#)

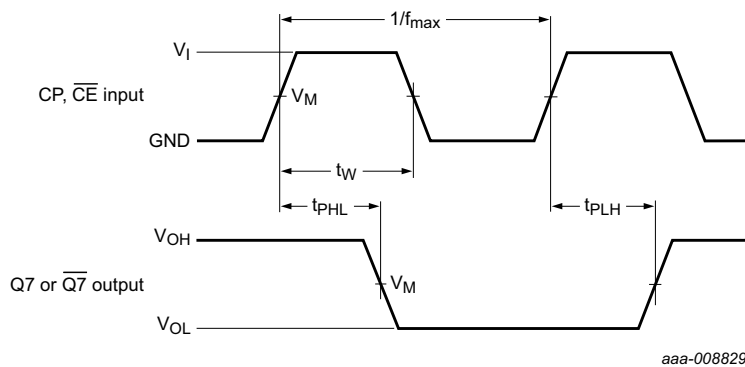
Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
t <sub>su</sub>	set-up time	DS to CP, $\overline{CE}$ ; see <a href="#">Figure 10</a>				
		V <sub>CC</sub> = 2.3 V to 2.7 V <sup>[3]</sup>	6.0	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[4]</sup>	4.0	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[5]</sup>	7.0	-	-	ns
		$\overline{CE}$ to CP, CP to $\overline{CE}$ ; see <a href="#">Figure 10</a>				
		V <sub>CC</sub> = 2.3 V to 2.7 V <sup>[3]</sup>	7.0	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[4]</sup>	5.0	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[5]</sup>	3.5	-	-	ns
		D7 to $\overline{PL}$ ; see <a href="#">Figure 11</a>				
		V <sub>CC</sub> = 2.3 V to 2.7 V <sup>[3]</sup>	12	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[4]</sup>	8.5	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[5]</sup>	5.0	-	-	ns
t <sub>h</sub>	hold time	DS to CP, $\overline{CE}$ ; $\overline{PL}$ to CP, $\overline{CE}$ ; see <a href="#">Figure 10</a>				
		V <sub>CC</sub> = 2.3 V to 2.7 V <sup>[3]</sup>	0	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[4]</sup>	0	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[5]</sup>	0.5	-	-	ns
		Dn to $\overline{PL}$ ; see <a href="#">Figure 11</a>				
		V <sub>CC</sub> = 2.3 V to 2.7 V <sup>[3]</sup>	0.5	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[4]</sup>	0.5	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[5]</sup>	1.0	-	-	ns
f <sub>max</sub>	maximum frequency	CP input; C <sub>L</sub> = 15 pF; see <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 2.3 V to 2.7 V <sup>[3]</sup>	45	80	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[4]</sup>	50	115	-	MHz
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[5]</sup>	90	165	-	MHz
		CP input; see <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 2.3 V to 2.7 V <sup>[3]</sup>	35	65	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[4]</sup>	50	90	-	MHz
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[5]</sup>	85	125	-	MHz

**Table 7. Dynamic characteristics ...continued**  
 GND (ground = 0 V); for test circuit, see [Figure 12](#)

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V <sup>[6]</sup>	-	24	-	pF

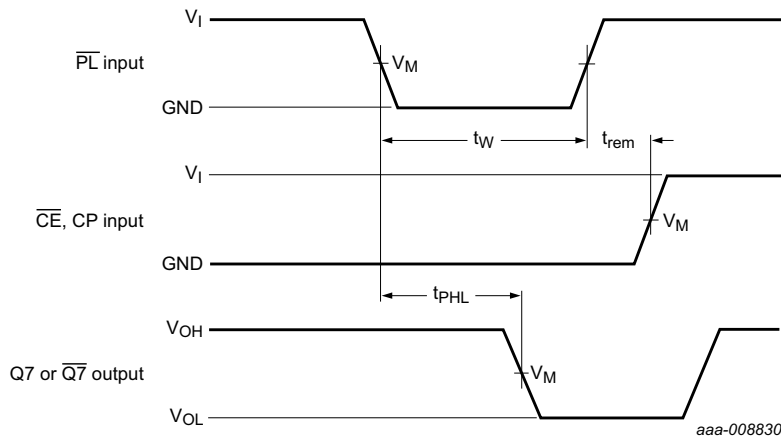
- [1] Typical values are measured at T<sub>amb</sub> = 25 °C and nominal V<sub>CC</sub>.
- [2] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.
- [3] Typical values are measured at V<sub>CC</sub> = 2.5 V.
- [4] Typical values are measured at V<sub>CC</sub> = 3.3 V.
- [5] Typical values are measured at V<sub>CC</sub> = 5.0 V.
- [6] C<sub>PD</sub> is used to determine the dynamic power dissipation P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> + Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) (P<sub>D</sub> in μW), where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V.

## 11. Waveforms



Measurement points are given in [Table 8](#).  
 The changing to output assumes that internal Q6 is opposite state from Q7.

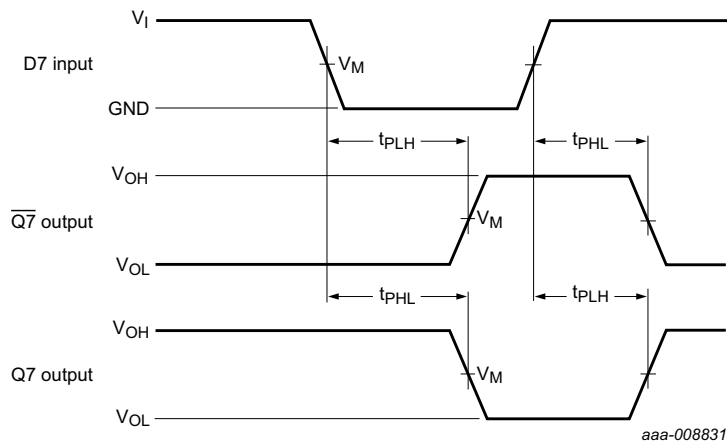
**Fig 7. Clock pulse (CP) and clock enable (CE) to output (Q7 or Q7) propagation delays, clock pulse width and maximum clock frequency**



Measurement points are given in [Table 8](#).

The changing to output assumes that internal Q6 is opposite state from Q7.

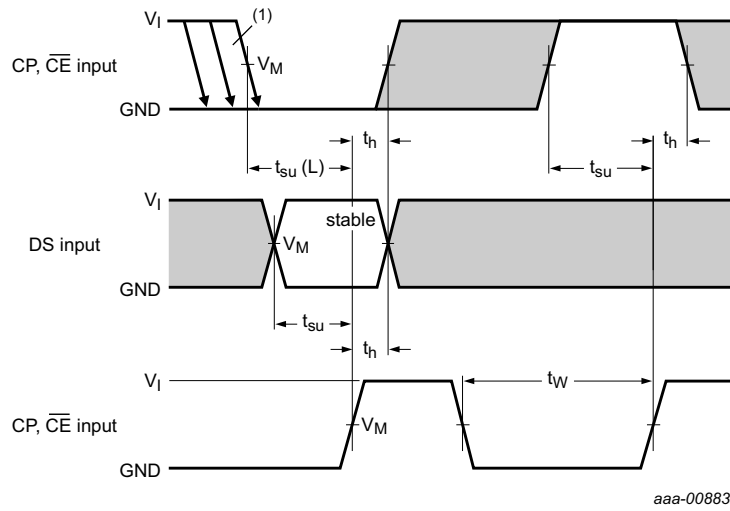
**Fig 8. Parallel load ( $\overline{PL}$ ) pulse width, parallel load to output (Q7 or  $\overline{Q7}$ ) propagation delays, parallel load to clock (CP) and clock enable ( $\overline{CE}$ ) recovery time**



Measurement points are given in [Table 8](#).

The changing to output assumes that internal Q6 is opposite state from Q7.

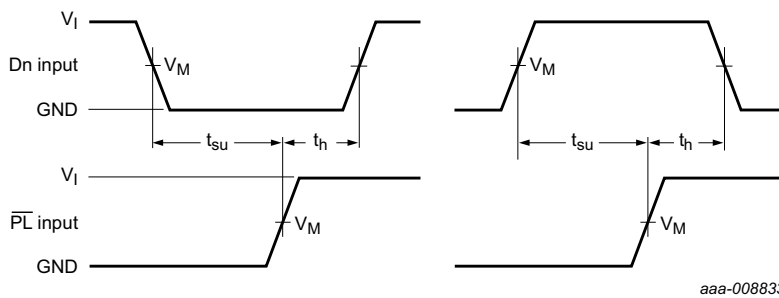
**Fig 9. Data input (D7) to output (Q7 or  $\overline{Q7}$ ) propagation delays when  $\overline{PL}$  is LOW**



Measurement points are given in [Table 8](#).

- (1) CE may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 10. Set-up and hold times**

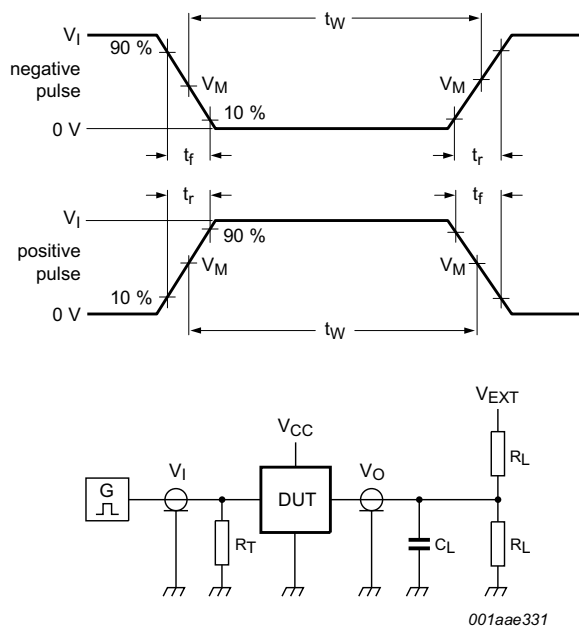


Measurement points are given in [Table 8](#).

**Fig 11. Set-up and hold times from the data inputs (Dn) to the parallel load input (PL)**

**Table 8. Measurement points**

Supply voltage	Input	Output
V <sub>CC</sub>	V <sub>M</sub>	V <sub>M</sub>
2.0 V to 5.5 V	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 12. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$
2.0 V to 5.5 V	$V_{CC}$	3.0 ns	50 pF, 15 pF	1 k $\Omega$	open

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

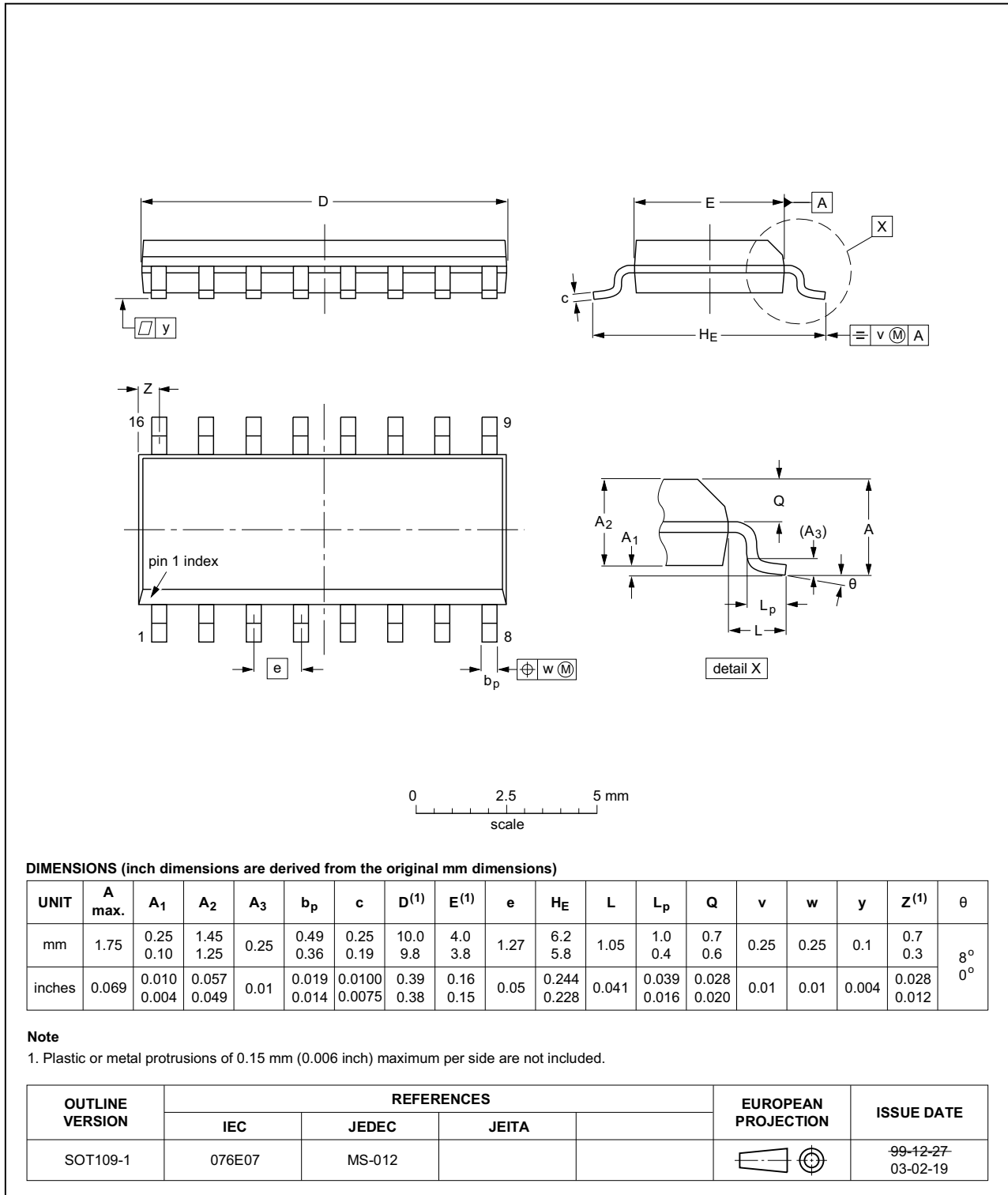


Fig 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

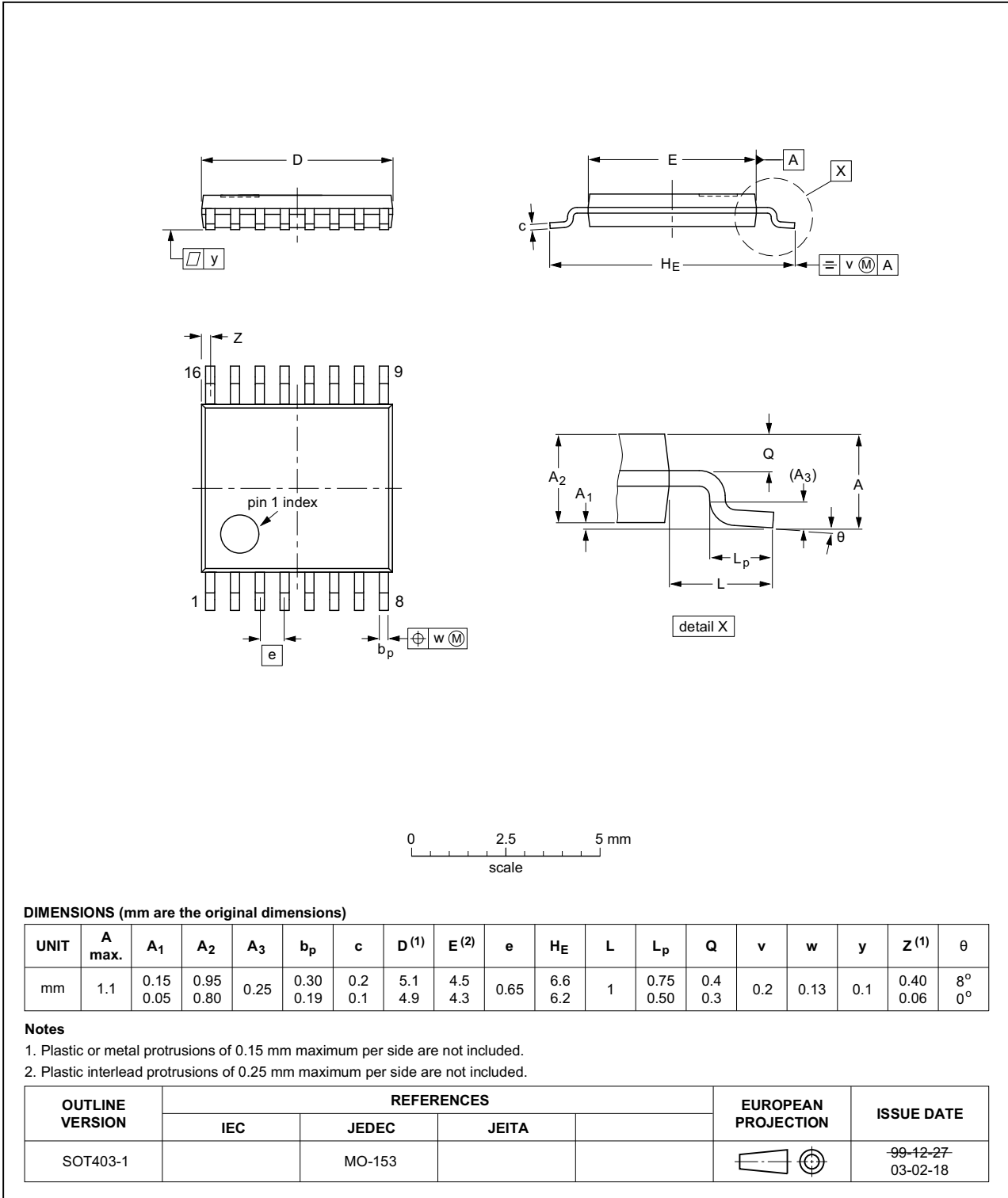


Fig 14. Package outline SOT403-1 (TSSOP16)



## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV165A v.4	20140328	Product data sheet	-	74LV165A v.3
Modifications:	<ul style="list-style-type: none"> <li>Minimum limit <math>V_{OH}</math> for <math>V_{CC} = 4.5</math> V corrected from 3.0 V to 3.8 V (errata) in <a href="#">Table 6 "Static characteristics"</a></li> </ul>			
74LV165A v.3	20140220	Product data sheet	-	74LV165A v.2
Modifications:	<ul style="list-style-type: none"> <li>Typo corrected in <a href="#">Table 2 "Pin description"</a></li> </ul>			
74LV165A v.2	20130904	Product data sheet	-	74LV165A_CNV_1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Family data added, see <a href="#">Section 9 "Static characteristics"</a></li> </ul>			
74LV165A_CNV_1	December 1990	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 28 March 2014

Document identifier: 74LV165A