PN7120

Full NFC Forum-compliant controller with integrated firmware and NCI interface

Rev. 2 — 15 June 2015
312420

Preliminary data sheet
COMPANY PUBLIC

1. Introduction

This document describes the functionality and electrical specification of the NFC Controller PN7120.

Additional documents describing the product functionality further are available for design-in support. Refer to the references listed in this document to get access to the full for full documentation provided by NXP.

2. General description

PN7120 is a full NFC controller solution with integrated firmware and NCI interface designed for contactless communication at 13.56 MHz.

PN7120 is the ideal solution for rapidly integrating NFC technology in any application, especially those running O/S environment like Linux and Android, reducing Bill of Material (BOM) size and cost, thanks to:

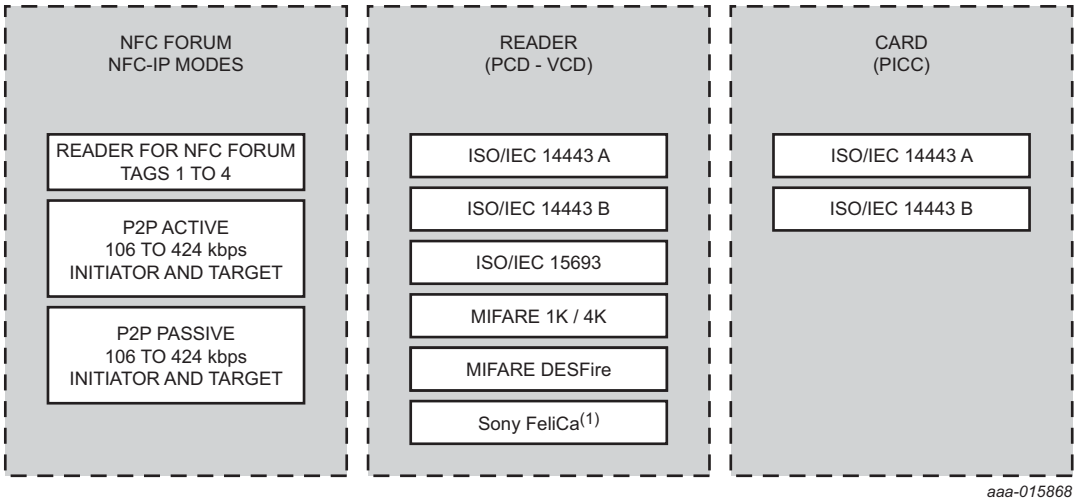
- full NFC forum compliancy (see Ref. 11) with small form factor antenna
- embedded NFC firmware providing all NFC protocols as pre-integrated feature
- direct connection to the main host or microcontroller, by I^2C-bus physical and NCI protocol
- ultra-low power consumption in polling loop mode
- Highly efficient integrated power management unit (PMU) allowing direct supply from a battery

PN7120 embeds a new generation RF contactless front-end supporting various transmission modes according to NFCIP-1 and NFCIP-2, ISO/IEC14443, ISO/IEC 15693, ISO/IEC 18000-3, MIFARE and FeliCa specifications. It embeds an ARM Cortex-M0 microcontroller core loaded with the integrated firmware supporting the NCI 1.0 host communication.

The contactless front-end design brings a major performance step-up with on one hand a higher sensitivity and on the other hand the capability to work in active load modulation communication enabling the support of small antenna form factor

Supported transmission modes are listed in Figure 1. For contactless card functionality, the PN7120 can act autonomously if previously configured by the host in such a manner.

PN7120 integrated firmware provides an easy integration and validation cycle as all the NFC real-time constraints, protocols and device discovery (polling loop) are being taken care internally. In few NCI commands, host SW can configure the PN7120 to notify for card or peer detection and start communicating with them.



(1) According to ISO/IEC 18092 (Ecma 340) standard.

Fig 1. PN7120 transmission modes

3. Features and benefits

- ARM Cortex-M0 microcontroller core
- Highly integrated demodulator and decoder
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated Polling Loop for automatic device discovery
- RF protocols supported
  - NFCIP-1, NFCIP-2 protocol (see Ref. 7 and Ref. 10)
  - ISO/IEC 14443A, ISO/IEC 14443B PICC mode via host interface (see Ref. 2)
  - ISO/IEC 14443A, ISO/IEC 14443B PCD designed according to NFC Forum digital protocol T4T platform and ISO-DEP (see Ref. 11)
  - FeliCa PCD mode
  - MIFARE PCD encryption mechanism (MIFARE 1K/4K)
  - NFC Forum tag 1 to 4 (MIFARE Ultralight, Jewel, Open FeliCa tag, DESFire) (see Ref. 11)
  - ISO/IEC 15693/ICODE VCD mode (see Ref. 8)
- Supported host interfaces
  - NCI protocol interface according to NFC Forum standardization (see Ref. 1)
  - I^2C-bus High-speed mode (see Ref. 3)
- Integrated power management unit
  - Direct connection to a battery (2.3 V to 5.5 V voltage supply range)

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- Support different Hard Power-Down/Standby states activated by firmware
- Autonomous mode when host is shut down

- Automatic wake-up via RF field, internal timer and I^2C-bus interface
- Integrated non-volatile memory to store data and executable code for customization

4. Applications

- All devices requiring NFC functionality especially those running in an Android or Linux environment
- TVs, set-top boxes, Blu-ray decoders, audio devices
- Home automation, gateways, wireless routers
- Home appliances
- Wearables, remote controls, healthcare, fitness
- Printers, IP phones, gaming consoles, accessories

5. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	Card Emulation and Passive Target; V_{SS} = 0 V [1] [2]	2.3	-	5.5	V
		Reader, Active Initiator and Active Target; V_{SS} = 0 V [1] [2]	2.7	-	5.5	V
V_{DD}	supply voltage	internal supply voltage	1.65	1.8	1.95	V
$V_{DD(PAD)}$	$V_{DD(PAD)}$ supply voltage	supply voltage for host interface				
		1.8 V host supply; V_{SS} = 0 V [1]	1.65	1.8	1.95	V
		3.3 V host supply; V_{SS} = 0 V [1]	3.0	-	3.6	V
I_{BAT}	battery supply current	in Hard Power Down state; V_{BAT} = 3.6 V; T = 25 °C	-	10	12	µA
		in Standby state; V_{BAT} = 3.6 V; T = 25 °C	-	-	20	µA
		in Monitor state; V_{BAT} = 2.75 V; T = 25 °C	-	-	12	µA
		in low-power polling loop; V_{BAT} = 3.6 V; T = 25 °C; loop time = 500 ms	-	150	-	µA
		PCD mode at typical 3 V [3]	-	-	170	mA
$I_{O(VDDPAD)}$	output current on pin $V_{DD(PAD)}$	total current which can be pulled on $V_{DD(PAD)}$ referenced outputs	-	-	15	mA

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Table 1. Quick reference data *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{th(Ilim)}$	current limit threshold current	current limiter on $V_{DD(TX)}$ pin; $V_{DD(TX)}$ = 3.1 V [3] [4]	-	180	-	mA
P_{tot}	total power dissipation	Reader; $I_{VDD(TX)}$ = 100 mA; V_{BAT} = 5.5 V	-	-	0.5	W
T_{amb}	ambient temperature	JEDEC PCB-0.5	−30	+25	+85	°C

[1] V_{SS} represents V_{SS}, V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}, $V_{SS(PAD)}$ and $V_{SS(TX)}$.

[2] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account).

[3] The antenna shall be tuned not to exceed the maximum of I_{VBAT}.

[4] This is the threshold of a built-in protection done to limit the current out of $V_{DD(TX)}$ in case of any issue at antenna pins to avoid burning the device. It is not allowed in operational mode to have $I_{VDD(TX)}$ such that I_{VBAT} maximum value is exceeded.

6. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN7120A0EV/C1xxxx	VFBGA49	plastic very thin fine-pitch ball grid array package; 49 balls	SOT1320-1

7. Marking

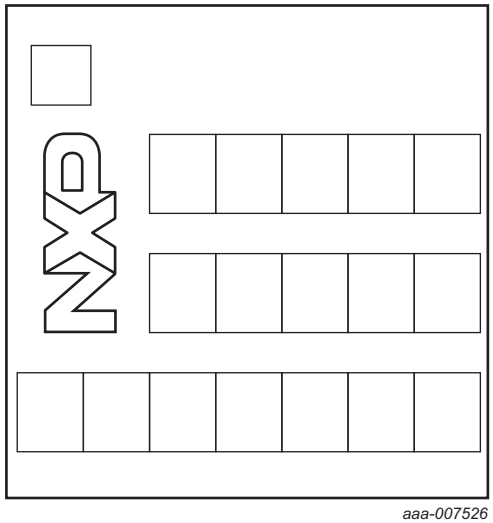

Fig 2. PN7120 package marking (top view)

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Table 3. Marking code

Line number	Marking code
Line 1	product version identification
Line 2	diffusion batch sequence number
Line 3	manufacturing code including: • diffusion center code: – N: TSMC – s: Global Foundry • assembly center code: – S: APK – X: ASEN • RoHS compliancy indicator: – D: Dark Green; fully compliant RoHS and no halogen and antimony • manufacturing year and week, 3 digits: – Y: year – WW: week code • product life cycle status code: – X: means not qualified product – nothing means released product

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8. Block diagram

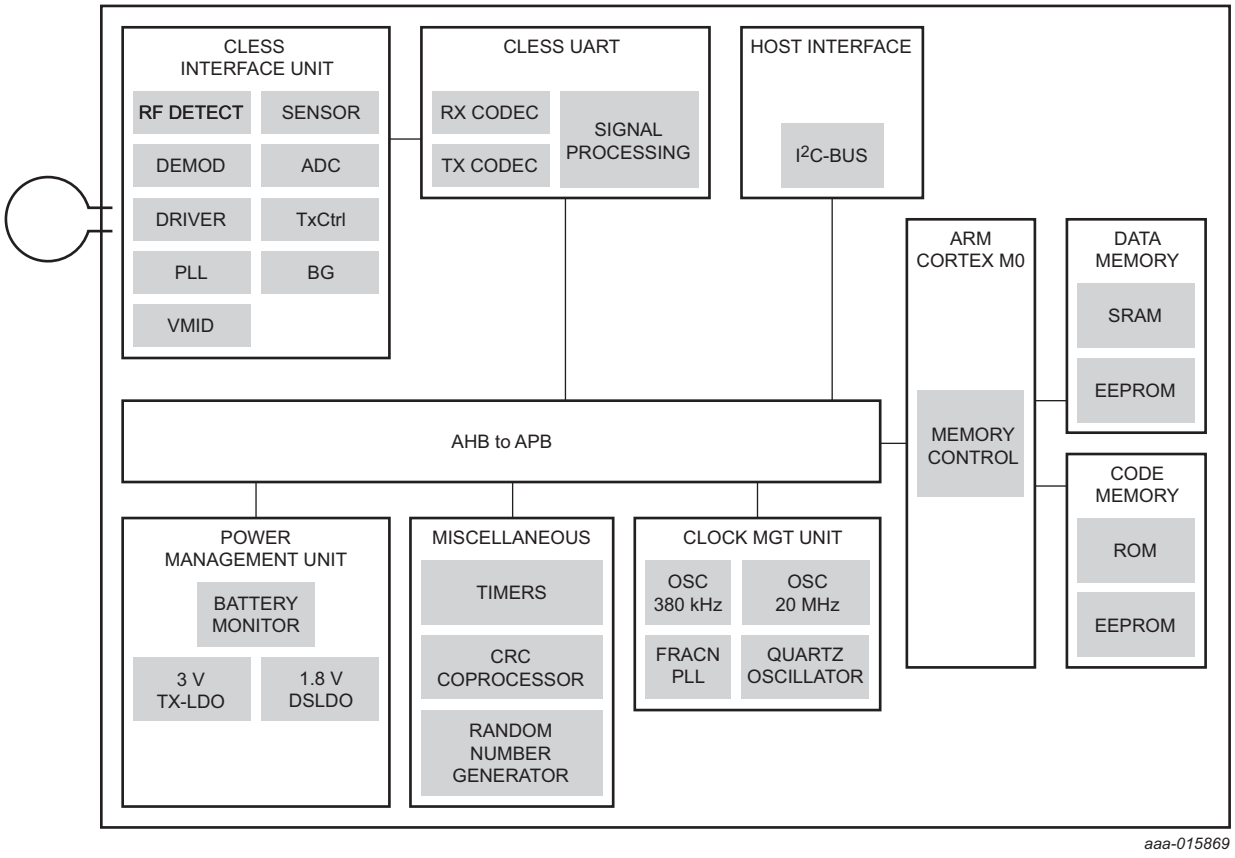

Fig 3. PN7120 block diagram

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9. Pinning information

9.1 Pinning

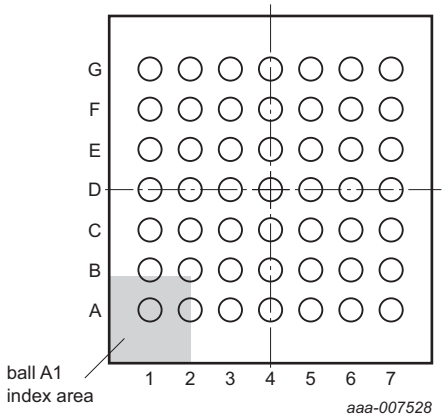

Fig 4. PN7120 pinning (bottom view)

Table 4. PN7120 pin description

Symbol	Pin	Type[1]	Refer	Description
i.c.	A1	-	-	internally connected; leave open
CLK_REQ	A2	O	$V_{DD(PAD)}$	clock request pin
XTAL1	A3	I	V_{DD}	PLL clock input. Oscillator input
i.c.	A4	-	-	internally connected; leave open
i.c.	A5	-	-	internally connected; must be connected to ground
i.c.	A6	-	-	internally connected; leave open
i.c.	A7	-	-	internally connected; leave open
I2CSCL	B1	I	$V_{DD(PAD)}$	I^2C-bus serial clock input
I2CADR0	B2	I	$V_{DD(PAD)}$	I^2C-bus address bit 0 input
i.c.	B3	-	-	internally connected; leave open
i.c.	B4	-	-	internally connected; leave open
i.c.	B5	-	-	internally connected; must be connected to ground
V_{SS1}	B6	G	n/a	ground
i.c.	B7	-	-	internally connected; leave open
I2CSDA	C1	I/O	$V_{DD(PAD)}$	I^2C-bus serial data
$V_{SS(PAD)}$	C2	G	n/a	pad ground
XTAL2	C3	O	V_{DD}	oscillator output
V_{SS}	C4	G	n/a	ground
n.c.	C5	-	-	not connected
V_{DD}	C6	P	n/a	LDO output supply voltage
V_{BAT}	C7	P	n/a	battery supply voltage
IRQ	D1	O	$V_{DD(PAD)}$	interrupt request output

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Table 4. PN7120 pin description *…continued*

Symbol	Pin	Type[1]	Refer	Description
BOOST_CTRL	D2	O	$V_{DD(PAD)}$	booster control, see Ref. 5
$V_{DD(PAD)}$	D3	P	n/a	pad supply voltage
V_{SS2}	D4	G	n/a	ground
i.c.	D5	-	-	internally connected; leave open
V_{SS3}	D6	G	n/a	ground
i.c.	D7	-	-	internally connected; leave open
VEN	E1	I	V_{BAT}	reset pin. Set the device in Hard Power Down
$V_{SS(DC_DC)}$	E2	G	n/a	ground
n.c.	E3	-	-	not connected
n.c.	E4	-	-	not connected
n.c.	E5	-	-	not connected
n.c.	E6	-	-	not connected
$V_{DD(TX)}$	E7	P	n/a	contactless transmitter output supply voltage for decoupling
i.c.	F1	-	-	internally connected; leave open
i.c.	F2	-	-	internally connected; leave open
V_{SS4}	F3	G	n/a	ground
i.c.	F4	-	-	internally connected; leave open
RXN	F5	I	V_{DD}	negative receiver input
RXP	F6	I	V_{DD}	positive receiver input
$V_{DD(MID)}$	F7	P	n/a	receiver reference input supply voltage
V_{BAT2}	G1	P	n/a	battery supply voltage; must be connected to V_{BAT}
V_{BAT1}	G2	P	n/a	battery supply voltage; must be connected to V_{BAT}
TX1	G3	O	$V_{DD(TX)}$	antenna driver output
$V_{SS(TX)}$	G4	G	n/a	contactless transmitter ground
TX2	G5	O	$V_{DD(TX)}$	antenna driver output
ANT2	G6	P	n/a	antenna connection for Listen mode
ANT1	G7	P	n/a	antenna connection for Listen mode

[1] P = power supply; G = ground; I = input, O = output; I/O = input/output.

10. Functional description

PN7120 can be connected on a host controller through I^2C-bus. The logical interface towards the host baseband is NCI-compliant Ref. 1 with additional command set for NXP-specific product features. This IC is fully user controllable by the firmware interface described in Ref. 4.

Moreover, PN7120 provides flexible and integrated power management unit in order to preserve energy supporting Power Off mode.

In the following chapters you will find also more details about PN7120 with references to very useful application note such as:

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- PN7120 User Manual (Ref. 4):

  User Manual describes the software interfaces (API) based on the NFC forum NCI standard. It does give full description of all the NXP NCI extensions coming in addition to NCI standard (Ref. 1).

- PN7120 Hardware Design Guide (Ref. 5):

  Hardware Design Guide provides an overview on the different hardware design options offered by the IC and provides guidelines on how to select the most appropriate ones for a given implementation. In particular, this document highlights the different chip power states and how to operate them in order to minimize the average NFC-related power consumption so to enhance the battery lifetime.

- PN7120 Antenna and Tuning Design Guide (Ref. 6):

  Antenna and Tuning Design Guide provides some guidelines regarding the way to design an NFC antenna for the PN7120 chip.

  It also explains how to determine the tuning/matching network to place between this antenna and the PN7120.

  Standalone antenna performances evaluation and final RF system validation (PN7120 + tuning/matching network + NFC antenna within its final environment) are also covered by this document.

- PN7120 Low-Power Mode Configuration (Ref. 9):

  Low-Power Mode Configuration documentation provides guidance on how PN7120 can be configured in order to reduce current consumption by using Low-power polling mode.

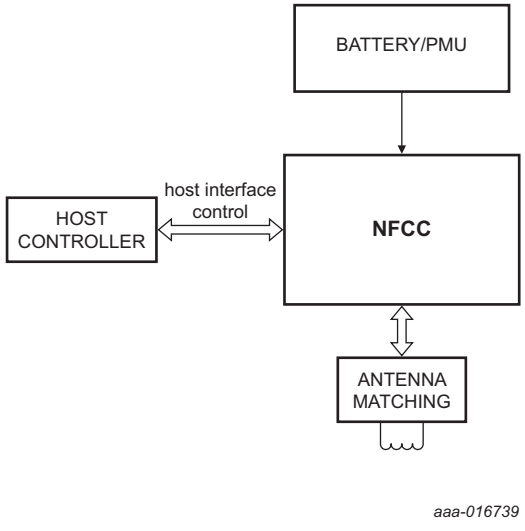

Fig 5. PN7120 connection

10.1 System modes

10.1.1 System power modes

PN7120 is designed in order to enable the different power modes from the system.

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2 power modes are specified: Full power mode and Power Off mode.

Table 5. System power modes description

System power mode	Description
Full power mode	the main supply (V_{BAT}) as well as the host interface supply ($V_{DD(PAD)}$) is available, all use cases can be executed
Power Off mode	the system is kept Hard Power Down (HPD)

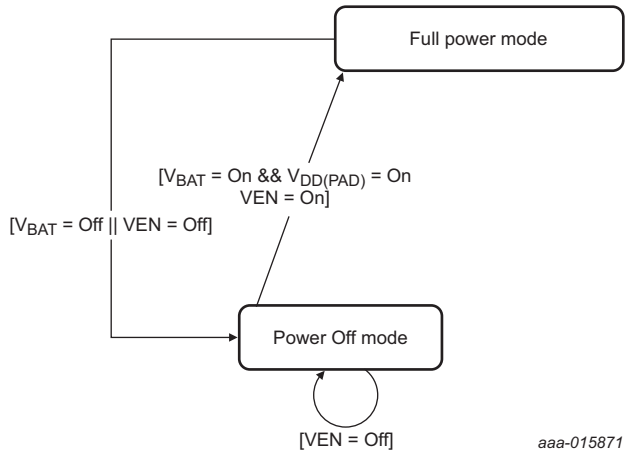

Fig 6. System power mode diagram

Table 6 summarizes the system power mode of the PN7120 depending on the status of the external supplies available in the system:

Table 6. System power modes configuration

V_{BAT}	VEN	Power mode
Off	X	Power Off mode
On	Off	Power Off mode
On	On	Full power mode

Depending on power modes, some application states are limited:

Table 7. System power modes description

System power mode	Allowed communication modes
Power Off mode	no communication mode available
Full power mode	Reader/Writer, Card Emulation, P2P modes

10.1.2 PN7120 power states

Next to system power modes defined by the status of the power supplies, the power states include the logical status of the system thus extend the power modes.

4 power states are specified: Monitor, Hard Power Down (HPD), Standby, Active.

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Table 8. PN7120 power states

Power state name	Description
Monitor	The PN7120 is supplied by V_{BAT} which voltage is below its programmable critical level, VEN voltage > 1.1 V and the Monitor state is enabled. The system power mode is Power Off mode.
Hard Power Down	The PN7120 is supplied by V_{BAT} which voltage is above its programmable critical level when Monitor state is enabled and PN7120 is kept in Hard Power Down (VEN voltage is kept low by host or SW programming) to have the minimum power consumption. The system power mode is in Power Off.
Standby	The PN7120 is supplied by V_{BAT} which voltage is above its programmable critical level when the Monitor state is enabled, VEN voltage is high (by host or SW programming) and minimum part of PN7120 is kept supplied to enable configured wake-up sources which allow to switch to Active state; RF field, Host interface. The system power mode is Full power mode.
Active	The PN7120 is supplied by V_{BAT} which voltage is above its programmable critical level when Monitor state is enabled, VEN voltage is high (by host or SW programming) and the PN7120 internal blocks are supplied. 3 functional modes are defined: Idle, Target and Initiator. The system power mode is Full power mode.

At application level, the PN7120 will continuously switch between different states to optimize the current consumption (polling loop mode). Refer to Table 1 for targeted current consumption in here described states.

The PN7120 is designed to allow the host controller to have full control over its functional states, thus of the power consumption of the PN7120 based NFC solution and possibility to restrict parts of the PN7120 functionality.

10.1.2.1 Monitor state

In Monitor state, the PN7120 will exit it only if the battery voltage recovers over the critical level. Battery voltage monitor thresholds show hysteresis behavior as defined in Table 26.

10.1.2.2 Hard Power Down (HPD) state

The Hard Power Down state is entered when $V_{DD(PAD)}$ and V_{BAT} are high by setting VEN voltage < 0.4 V. As these signals are under host control, the PN7120 has no influence on entering or exiting this state.

10.1.2.3 Standby state

Active state is PN7120's default state after boot sequence in order to allow a quick configuration of PN7120. It is recommended to change the default state to Standby state after first boot in order to save power. PN7120 can switch to Standby state autonomously (if configured by host).

In this state PN7120 most blocks including CPU are no more supplied. Number of wake-up sources exist to put PN7120 into Active state:

- I^2C-bus interface wake-up event
- Antenna RF level detector
- Internal timer event when using polling loop (380 kHz Low-power oscillator is enabled)

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If wake-up event occurs, PN7120 will switch to Active state. Any further operation depends on software configuration and/or wake-up source.

10.1.2.4 Active state

Within the Active state, the system is acting as an NFC device. The device can be in 3 different functional modes: Idle, Poller and Target.

Table 9. Functional modes in active state

Functional modes	Description
Idle	the PN7120 is active and allows host interface communication. The RF interface is not activated.
Listener	the PN7120 is active and is configured for listening to external device.
Poller	the PN7120 is active and is configured in Poller mode. It polls external device

Poller mode: In this mode, PN7120 is acting as Reader/Writer or NFC Initiator, searching for or communicating with passive tags or NFC target. Once RF communication has ended, PN7120 will switch to active battery mode (that is, switch off RF transmitter) to save energy. Poller mode shall be used with 2.7 V < V_{BAT} < 5.5 V and VEN voltage > 1.1 V. Poller mode shall not be used with V_{BAT} < 2.7 V. $V_{DD(PAD)}$ is within its operational range (see Table 1).

Listener mode: In this mode, PN7120 is acting as a card or as an NFC Target. Listener mode shall be used with 2.3 V < V_{BAT} < 5.5 V and VEN voltage > 1.1 V.

10.1.2.5 Polling loop

The polling loop will sequentially set PN7120 in different power states (Active or Standby). All RF technologies supported by PN7120 can be independently enabled within this polling loop.

There are 2 main phases in the polling loop:

- Listening phase. The PN7120 can be in Standby power state or Listener mode
- Polling phase. The PN7120 is in Poller mode

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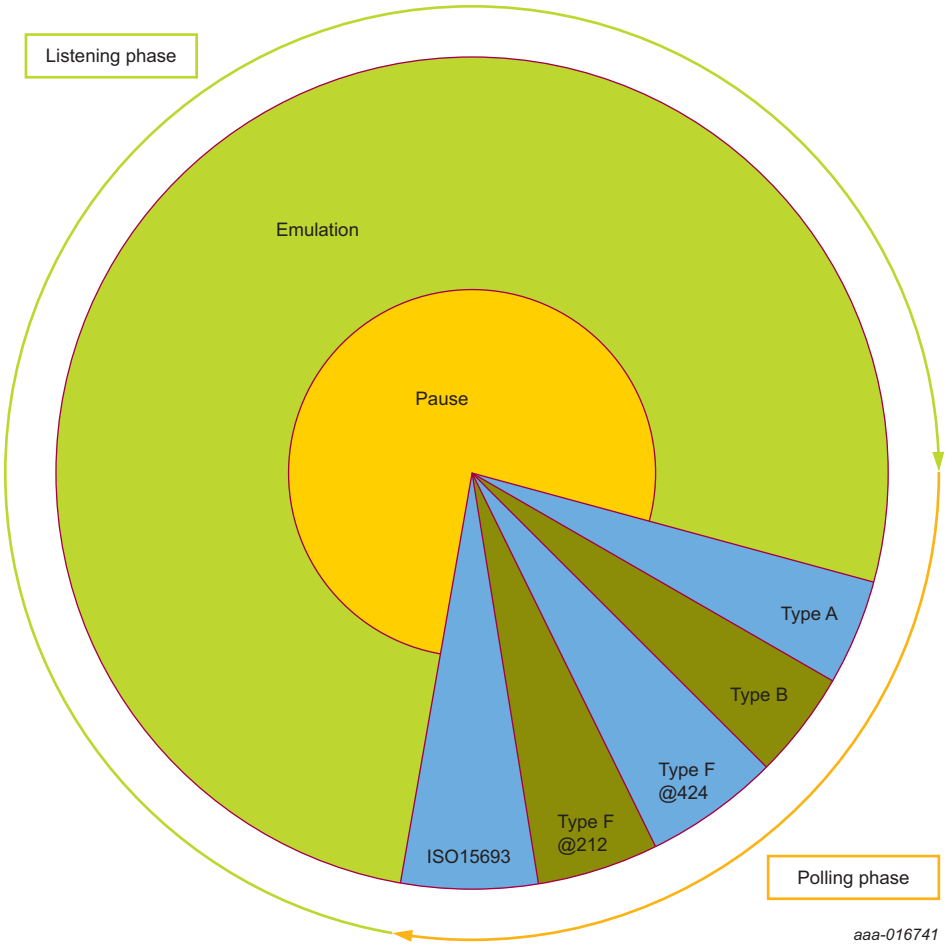

Fig 7. Polling loop: all phases enabled

Listening phase uses Standby power state (when no RF field) and PN7120 goes to Listener mode when RF field is detected. When in Polling phase, PN7120 goes to Poller mode.

To further decrease the power consumption when running the polling loop, PN7120 features a low-power RF polling. When PN7120 is in Polling phase instead of sending regularly RF command PN7120 senses with a short RF field duration if there is any NFC Target or card/tag present. If yes, then it goes back to standard polling loop. With 500 ms (configurable duration, see Ref. 4) listening phase duration, the average power consumption is around 150 μA.

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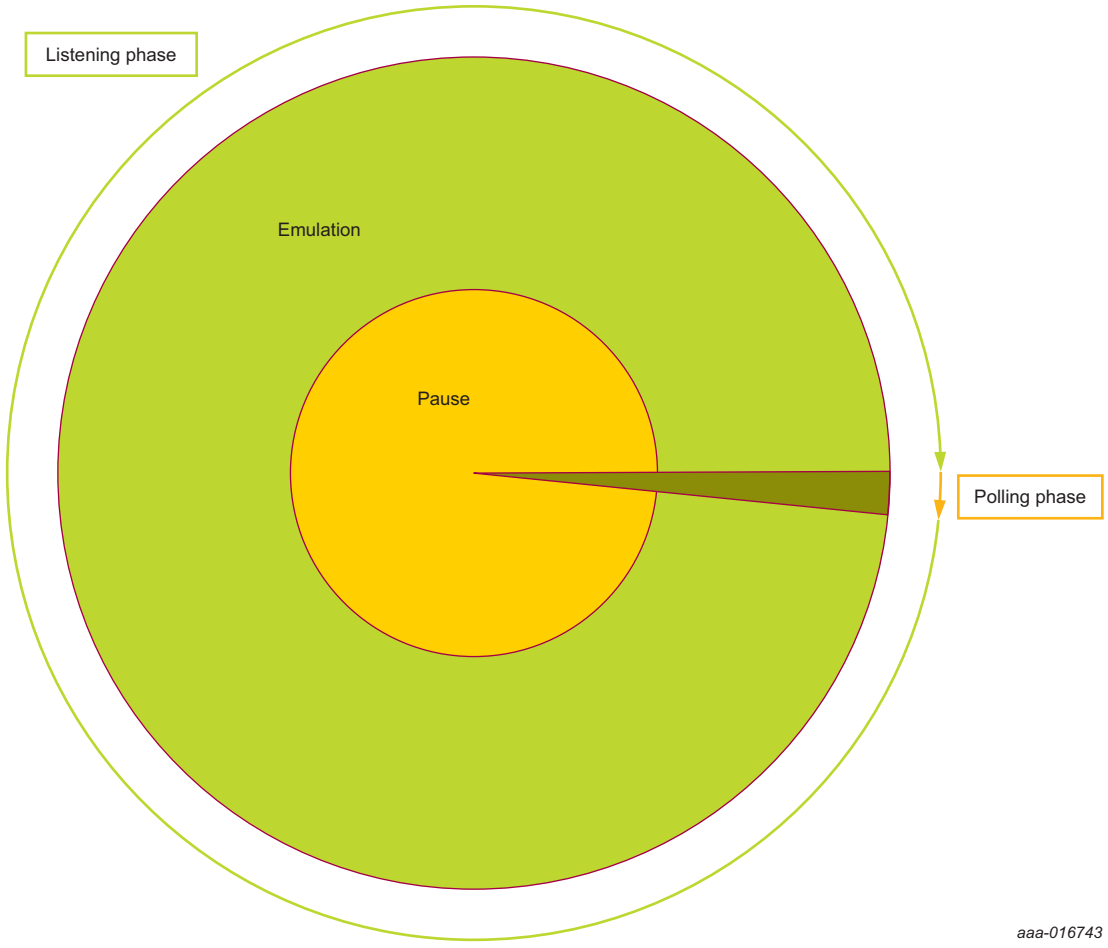

Fig 8. Polling loop: low-power RF polling

Detailed description of polling loop configuration options is given in Ref. 4.

10.2 Microcontroller

PN7120 is controlled via an embedded ARM Cortex-M0 microcontroller core.

PN7120 features integrated in firmware are referenced in Ref. 4

10.3 Host interfaces

PN7120 provides the support of an I^2C-bus Slave Interface, up to 3.4 MBaud.

The host interface is waken-up on I^2C-bus address.

To enable and ensure data flow control between PN7120 and host controller, additionally a dedicated interrupt line IRQ is provided which Active state is programmable. See Ref. 4 for more information.

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10.3.1 I²C-bus interface

The I²C-bus interface implements a slave I²C-bus interface with integrated shift register, shift timing generation and slave address recognition.

I²C-bus Standard mode (100 kHz SCL), Fast mode (400 kHz SCL) and High-speed mode (3.4 MHz SCL) are supported.

The mains hardware characteristics of the I²C-bus module are:

- Support slave I²C-bus
- Standard, Fast and High-speed modes supported
- Wake-up of PN7120 on its address only
- Serial clock synchronization can be used by PN7120 as a handshake mechanism to suspend and resume serial transfer (clock stretching)

The I²C-bus interface module meets the I²C-bus specification Ref. 3 except General call, 10-bit addressing and Fast mode Plus (Fm+).

10.3.1.1 I²C-bus configuration

The I²C-bus interface shares four pins with I²C-bus interface also supported by PN7120. When I²C-bus is configured in EEPROM settings, functionality of interface pins changes to one described in Table 10.

Table 10. Functionality for I²C-bus interface

Pin name	Functionality
I2CADR0	I²C-bus address 0
I2CSDA	I²C-bus data line
I2CSCL	I²C-bus clock line

PN7120 supports 7-bit addressing mode. Selection of the I²C-bus address is done by 2-pin configurations on top of a fixed binary header: 0, 1, 0, 1, 0, 0, I2CADR0, R/W.

Table 11. I²C-bus interface addressing

I2CADR0	I²C-bus address (R/W = 0, write)	I²C-bus address (R/W = 1, read)
0	0x50	0x51
1	0x52	0x53

10.4 PN7120 clock concept

There are 4 different clock sources in PN7120:

- 27.12 MHz clock coming either/or from:
  - Internal oscillator for 27.12 MHz crystal connection
  - Integrated PLL unit which includes a 1 GHz VCO
- 13.56 MHz RF clock recovered from RF field
- Low-power oscillator 20 MHz
- Low-power oscillator 380 kHz

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10.4.1 27.12 MHz quartz oscillator

When enabled, the 27.12 MHz quartz oscillator applied to PN7120 is the time reference for the RF front end when PN7120 is behaving in Reader mode or NFCIP-1 initiator.

Therefore stability of the clock frequency is an important factor for reliable operation. It is recommended to adopt the circuit shown in Figure 9.

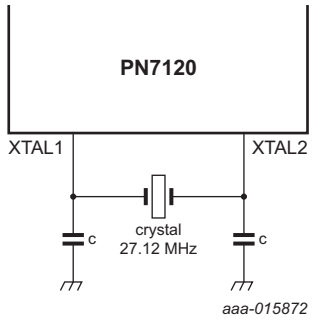

Fig 9. 27.12 MHz crystal oscillator connection

Table 12 describes the levels of accuracy and stability required on the crystal.

Table 12. Crystal requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{xtal}	crystal frequency	ISO/IEC and FCC compliancy	-	27.12	-	MHz
Δf_{xtal}	crystal frequency accuracy	full operating range [1]	−100	-	+100	ppm
		all V_{BAT} range; T = 20 °C [1]	−50	-	+50	ppm
		all temperature range; V_{BAT} = 3.6 V [1]	−50	-	+50	ppm
ESR	equivalent series resistance		-	50	100	Ω
C_L	load capacitance		-	10	-	pF
$P_{o(xtal)}$	crystal output power		-	-	100	μW

[1] This requirement is according to FCC regulations requirements. To meet only ISO/IEC 14443 and ISO/IEC 18092, then ± 14 kHz apply.

10.4.2 Integrated PLL to make use of external clock

When enabled, the PLL is designed to generate a low noise 27.12 MHz for an input clock 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz and 52 MHz.

The 27.12 MHz of the PLL is used as the time reference for the RF front end when PN7120 is behaving in Reader mode or NFC Initiator as well as in NFC Target when configured in Active communication mode.

The input clock on XTAL1 shall comply with the.following phase noise requirements for the following input frequency: 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz and 52 MHz:

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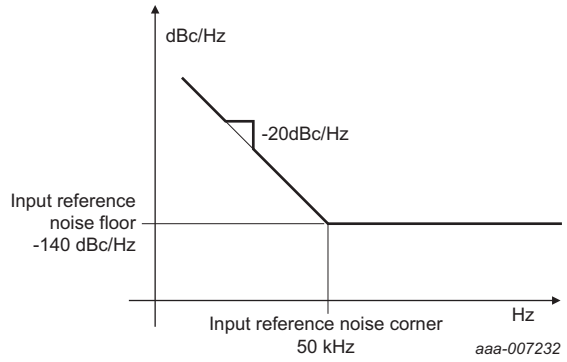

Fig 10. Input reference phase noise characteristics

This phase noise is equivalent to an RMS jitter of 6.23 ps from 10 Hz to 1 MHz. For configuration of input frequency, refer to Ref. 8. There are 6 pre programmed and validated frequencies for the PLL: 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz and 52 MHz.

Table 13. PLL input requirements

Coupling: single-ended, AC coupling;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	ISO/IEC and FCC compliancy	-	13	-	MHz
			-	19.2	-	MHz
			-	24	-	MHz
			-	26	-	MHz
			-	38.4	-	MHz
			-	52	-	MHz
$f_{i(ref)acc}$	reference input frequency accuracy	full operating range; frequencies typical values: 13 MHz, 26 MHz and 52 MHz [1]	−25	-	+25	ppm
		full operating range; frequencies typical values: 19.2 MHz, 24 MHz and 38.4 MHz [1]	−50	-	+50	ppm
φ_n	phase noise	input noise floor at 50 kHz	−140	-	-	dB/Hz
Sinusoidal shape						
$V_{i(p-p)}$	peak-to-peak input voltage		0.2	-	1.8	V
$V_{i(clk)}$	clock input voltage		0	-	1.8	V
Square shape						
$V_{i(clk)}$	clock input voltage		0	-	1.8 ± 10 %	V

[1] This requirement is according to FCC regulations requirements. To meet only ISO/IEC 14443 and ISO/IEC 18092, then ± 400 ppm limits apply.

For detailed description of clock request mechanisms, refer to Ref. 4 and Ref. 5.

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10.4.3 Low-power 20 MHz oscillator

Low-power 20 MHz oscillator is used as system clock of the system.

10.4.4 Low-power 380 kHz oscillator

A Low Frequency Oscillator (LFO) is implemented to drive a counter (WUC) waking-up PN7120 from Standby state. This allows implementation of low-power reader polling loop at application level. Moreover, this 380 kHz is used as the reference clock for write access to EEPROM memory.

10.5 Power concept

10.5.1 PMU functional description

The Power Management Unit of PN7120 generates internal supplies required by PN7120 out of V_{BAT} input supply voltage:

- V_{DD}: internal supply voltage
- $V_{DD(TX)}$: output supply voltage for the RF transmitter

The Figure 11 describes the main blocks available in PMU:

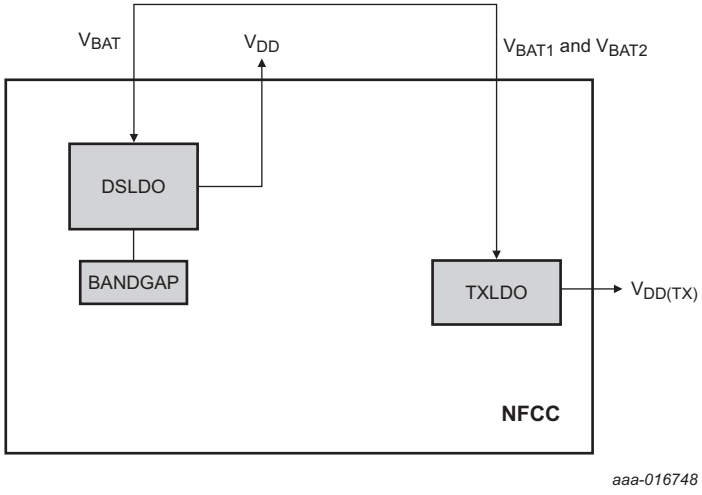

Fig 11. PMU functional diagram

10.5.2 DSLDO: Dual Supply LDO

The input pin of the DSLDO is V_{BAT}.

The Low drop-out regulator provides V_{DD} required in PN7120.

10.5.3 TXLDO

This is the LDO which generates the transmitter voltage.

The value of $V_{DD(TX)}$ is configured at 3.1 V ± 0.2 V.

$V_{DD(TX)}$ value is given according to the minimum targeted V_{BAT} value for which Reader mode shall work.

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For V_{BAT} above 3.1 V, $V_{DD(TX)}$ = 3.1 V:

$$V_{BAT} \geq 3.1V \Rightarrow V_{DD(TX)} = 3.1V$$

$$3.1V > V_{BAT} \geq 2.3V \Rightarrow V_{DD(TX)} = V_{BAT}$$

In Standby state, $V_{DD(TX)}$ is around 2.5 V with some ripples; it toggles between 2.35 V to 2.65 V with a period which depends on the capacitance and load on $V_{DD(TX)}$.

Figure 12 shows $V_{DD(TX)}$ behavior for 3.1 V:

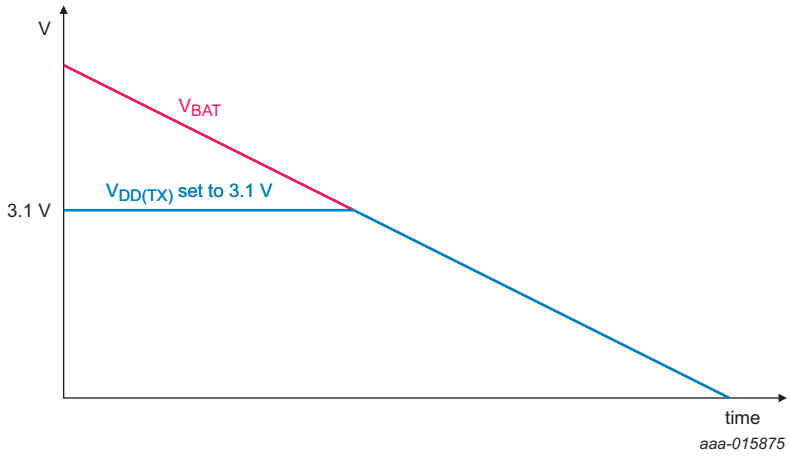

Fig 12. $V_{DD(TX)}$ offset disabled behavior

Figure 13 shows the case where the PN7120 is in Standby state:

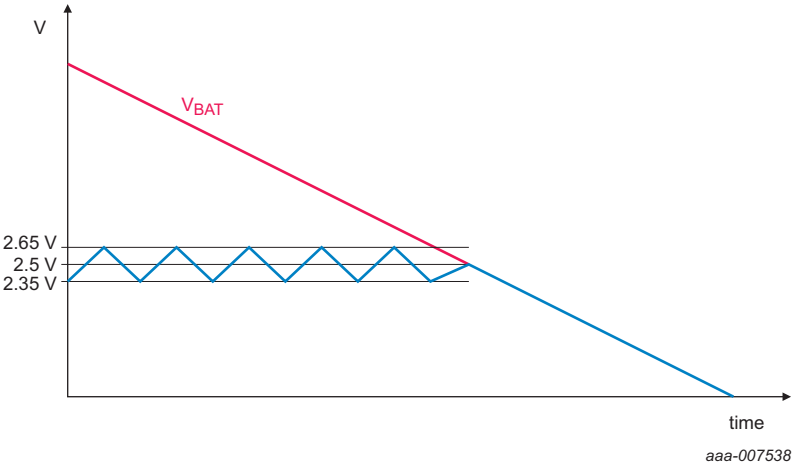

Fig 13. $V_{DD(TX)}$ behavior when PN7120 is in Standby state

10.5.3.1 TXLDO limiter

The TXLDO includes a current limiter to avoid too high current within TX1, TX2 when in reader or initiator modes.

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The current limiter block compares an image of the TXLDO output current to a reference. Once the reference is reached, the output current gets limited which is equivalent to a typical output current of 220 mA whatever V_{BAT} = 2.7 V and 180 mA for V_{BAT} = 3.1 V.

10.5.4 Battery voltage monitor

The PN7120 features low-power V_{BAT} voltage monitor which protects the host device battery from being discharged below critical levels. When V_{BAT} voltage goes below $V_{BATcritical}$ threshold, then the PN7120 goes in Monitor state. Refer to Figure 14 for principle schematic of the battery monitor.

The battery voltage monitor is enabled via an EEPROM setting.

The $V_{BATcritical}$ threshold can be configured to 2.3 V or 2.75 V by an EEPROM setting.

At the first start-up, V_{BAT} voltage monitor functionality is OFF and then enabled if properly configured in EEPROM. The PN7120 monitors battery voltage continuously.

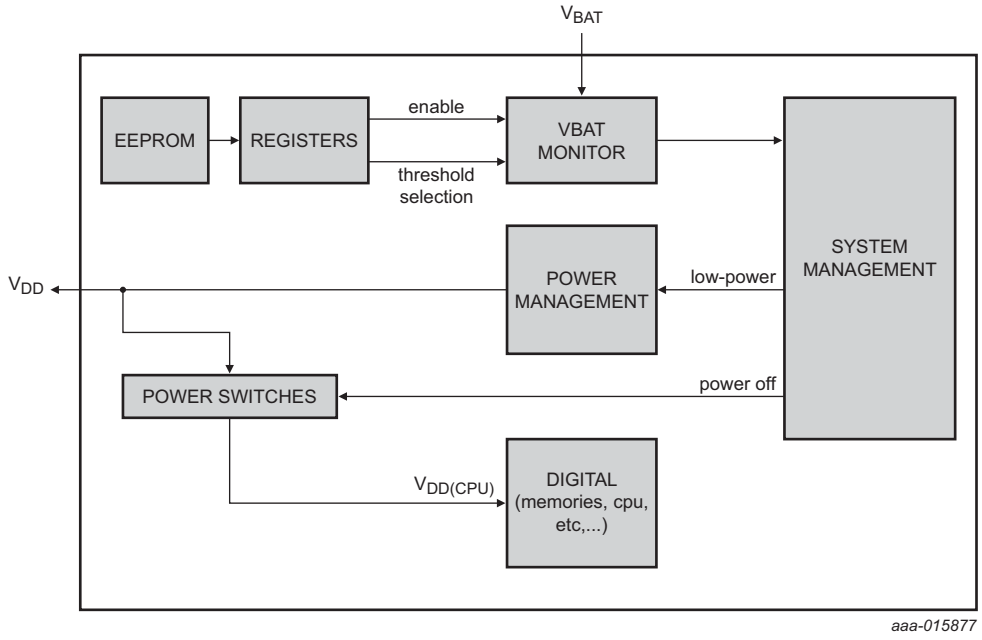

Fig 14. Battery voltage monitor principle

The value of the critical level can be configured to 2.3 V or 2.75 V by an EEPROM setting. This value has a typical hysteresis around 150 mV.

10.6 Reset concept

10.6.1 Resetting PN7120

To enter reset there are 2 ways:

- Pulling VEN voltage low (Hard Power Down state)
- if V_{BAT} monitor is enabled: lowering V_{BAT} below the monitor threshold (Monitor state, if VEN voltage is kept above 1.1 V)

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Reset means resetting the embedded FW execution and the registers values to their default values. Part of these default values is defined from EEPROM data loaded values, others are hardware defined. See Ref. 4 to know which ones are accessible to tune PN7120 to the application environment.

To get out of reset:

- Pulling VEN voltage high with V_{BAT} above V_{BAT} monitor threshold if enabled

Figure 15 shows reset done via VEN pin.

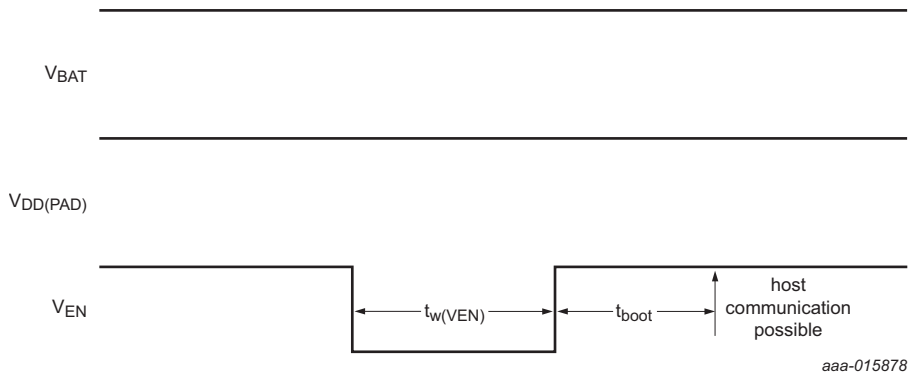

Fig 15. Resetting PN7120 via VEN pin

See Section 15.2.2 for the timings values.

10.6.2 Power-up sequences

There are 2 different supplies for PN7120. PN7120 allows these supplies to be set up independently, therefore different power-up sequences have to be considered.

10.6.2.1 V_{BAT} is set up before $V_{DD(PAD)}$

This is at least the case when V_{BAT} pin is directly connected to the battery and when PN7120 V_{BAT} is always supplied as soon the system is supplied.

As VEN pin is referred to V_{BAT} pin, VEN voltage shall go high after V_{BAT} has been set.

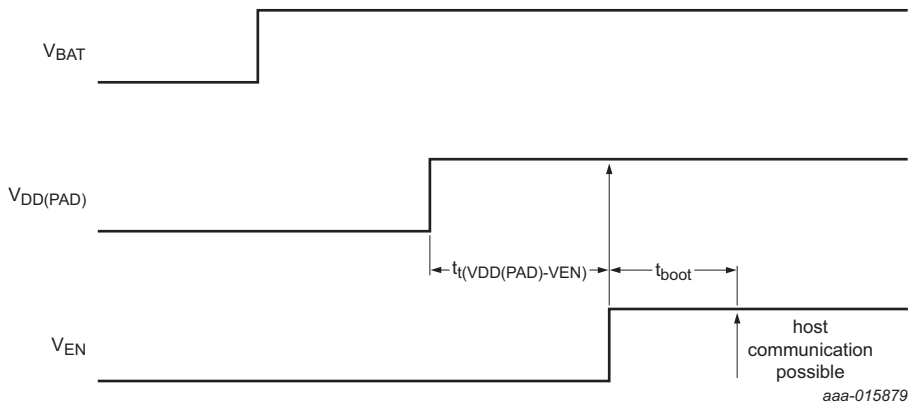

Fig 16. V_{BAT} is set up before $V_{DD(PAD)}$

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See Section 15.2.3 for the timings values.

10.6.2.2 $V_{DD(PAD)}$ and V_{BAT} are set up in the same time

It is at least the case when V_{BAT} pin is connected to a PMU/regulator which also supply $V_{DD(PAD)}$.

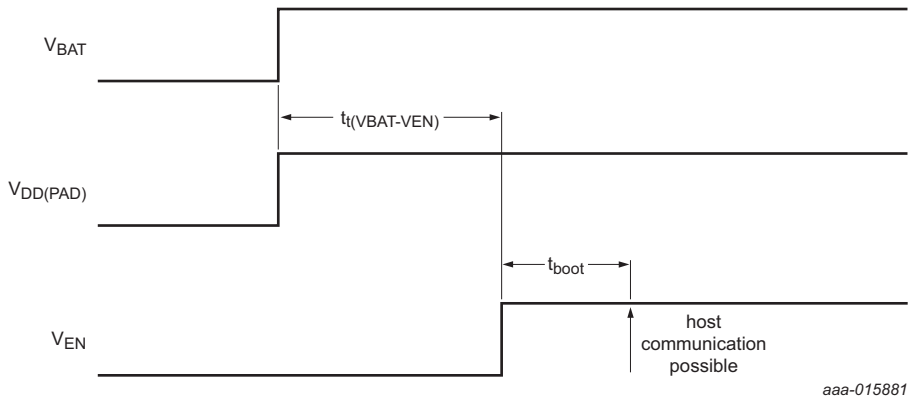

Fig 17. $V_{DD(PAD)}$ and V_{BAT} are set up in the same time

See Section 15.2.3 for the timings values.

10.6.2.3 PN7120 has been enabled before $V_{DD(PAD)}$ is set up or before $V_{DD(PAD)}$ has been cut off

This can be the case when V_{BAT} pin is directly connected to the battery and when $V_{DD(PAD)}$ is generated from a PMU. When the battery voltage is too low, then the PMU might no more be able to generate $V_{DD(PAD)}$. When the device gets charged again, then $V_{DD(PAD)}$ is set up again.

As the pins to select the interface are biased from $V_{DD(PAD)}$, when $V_{DD(PAD)}$ disappears the pins might not be correctly biased internally and the information might be lost. Therefore it is required to make the IC boot after $V_{DD(PAD)}$ is set up again.

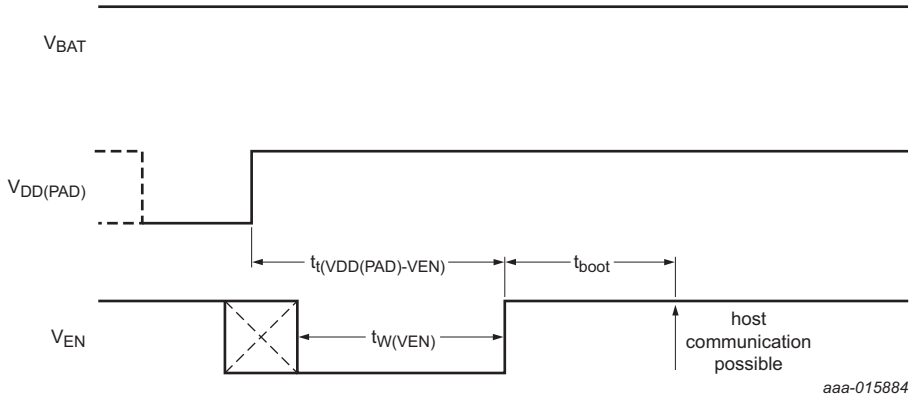

Fig 18. $V_{DD(PAD)}$ is set up or cut-off after PN7120 has been enabled

See Section 15.2.3 for the timings values.

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10.6.3 Power-down sequence

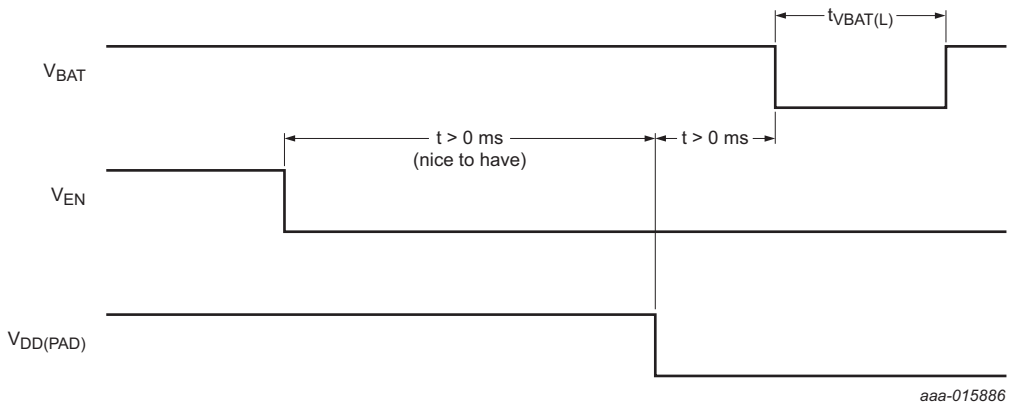

Fig 19. PN7120 power-down sequence

10.7 Contactless Interface Unit

PN7120 supports various communication modes at different transfer speeds and modulation schemes. The following chapters give more detailed overview of selected communication modes.

Remark: all indicated modulation index and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimum performance.

10.7.1 Reader/Writer communication modes

Generally 5 Reader/Writer communication modes are supported:

- PCD Reader/Writer for ISO/IEC 14443A/MIFARE
- PCD Reader/Writer for Jewel/Topaz tags
- PCD Reader/Writer for FeliCa cards
- PCD Reader/Writer for ISO/IEC 14443B
- VCD Reader/Writer for ISO/IEC 15693/ICODE

10.7.1.1 ISO/IEC 14443A/MIFARE and Jewel/Topaz PCD communication mode

The ISO/IEC 14443A/MIFARE PCD communication mode is the general reader to card communication scheme according to the ISO/IEC 14443A specification. This modulation scheme is as well used for communications with Jewel/Topaz cards.

Figure 20 describes the communication on a physical level, the communication table describes the physical parameters (the numbers take the antenna effect on modulation depth for higher data rates).

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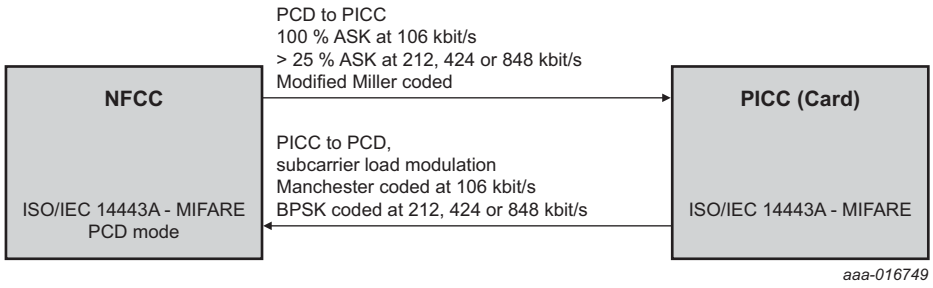

Fig 20. ISO/IEC 14443A/MIFARE Reader/Writer communication mode diagram

Table 14. Overview for ISO/IEC 14443A/MIFARE Reader/Writer communication mode

Communication direction		ISO/IEC 14443A/ MIFARE/ Jewel/ Topaz	ISO/IEC 14443A higher transfer speeds		
	Transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**	**848 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**	**(16/13.56) µs**
PN7120 → PICC					
(data sent by PN7120 to a card)	modulation on PN7120 side	100 % ASK	> 25 % ASK	> 25 % ASK	> 25 % ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller	Modified Miller
PICC → PN7120					
(data received by PN7120 from a card)	modulation on PICC side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester	BPSK	BPSK	BPSK

The contactless coprocessor and the on-chip CPU of PN7120 handle the complete ISO/IEC 14443A/MIFARE RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

10.7.1.2 FeliCa PCD communication mode

The FeliCa communication mode is the general Reader/Writer to card communication scheme according to the FeliCa specification. Figure 21 describes the communication on a physical level, the communication overview describes the physical parameters.

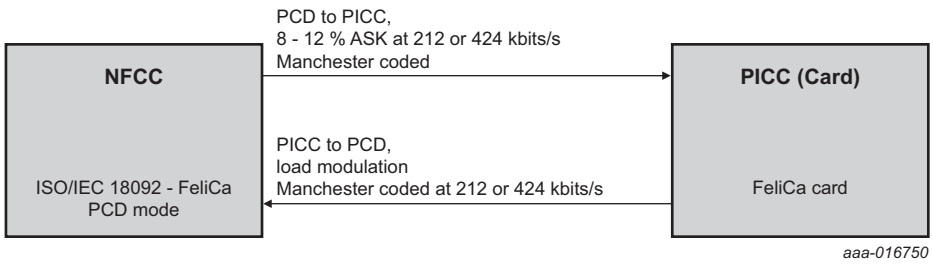

Fig 21. FeliCa Reader/Writer communication mode diagram

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Table 15. Overview for FeliCa Reader/Writer communication mode

Communication direction		FeliCa	FeliCa higher transfer speeds
	Transfer speed	**212 kbit/s**	**424 kbit/s**
	Bit length	**(64/13.56) µs**	**(32/13.56) µs**
PN7120 → PICC			
(data sent by PN7120 to a card)	modulation on PN7120 side	8 % – 12 % ASK	8 % – 12 % ASK
	bit coding	Manchester	Manchester
PICC → PN7120			
(data received by PN7120 from a card)	modulation on PICC side	load modulation	load modulation
	subcarrier frequency	no subcarrier	no subcarrier
	bit coding	Manchester	Manchester

The contactless coprocessor of PN7120 and the on-chip CPU handle the FeliCa protocol. Nevertheless a dedicated external host has to handle the application layer communication.

10.7.1.3 ISO/IEC 14443B PCD communication mode

The ISO/IEC 14443B PCD communication mode is the general reader to card communication scheme according to the ISO/IEC 14443B specification.Figure 22 describes the communication on a physical level, the communication table describes the physical parameters.

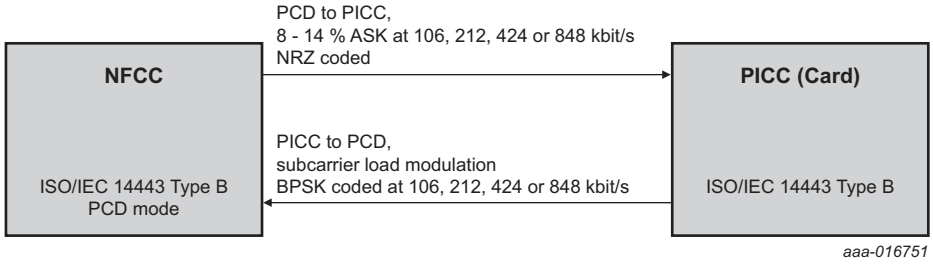

Fig 22. ISO/IEC 14443B Reader/Writer communication mode diagram

Table 16. Overview for ISO/IEC 14443B Reader/Writer communication mode

Communication direction		ISO/IEC 14443B	ISO/IEC 14443B higher transfer speeds		
	Transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**	**848 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**	**(16/13.56) µs**
PN7120 → PICC					
(data sent by PN7120 to a card)	modulation on PN7120 side	8 % – 14 % ASK	8 % – 14 % ASK	8 % – 14 % ASK	8 % – 14 % ASK
	bit coding	NRZ	NRZ	NRZ	NRZ
PICC → PN7120					

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Table 16. Overview for ISO/IEC 14443B Reader/Writer communication mode *...continued*

Communication direction		ISO/IEC 14443B	ISO/IEC 14443B higher transfer speeds		
	Transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**	**848 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**	**(16/13.56) µs**
(data received by PN7120 from a card)	modulation on PICC side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	BPSK	BPSK	BPSK	BPSK

The contactless coprocessor and the on-chip CPU of PN7120 handles the complete ISO/IEC 14443B RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

10.7.1.4 ISO/IEC 15693 VCD communication mode

The ISO/IEC 15693 VCD Reader/Writer communication mode is the general reader to card communication scheme according to the ISO/IEC 15693 specification. PN7120 will communicate with VICC using only the higher data rates of the VICC (26.48 kbit/s with single subcarrier and 26.69 kbit/s with dual subcarrier).

PN7120 supports the commands as defined by the ETSI HCI (see Ref. 1) and on top offers the inventory of the tags (anticollision sequence) on its own.

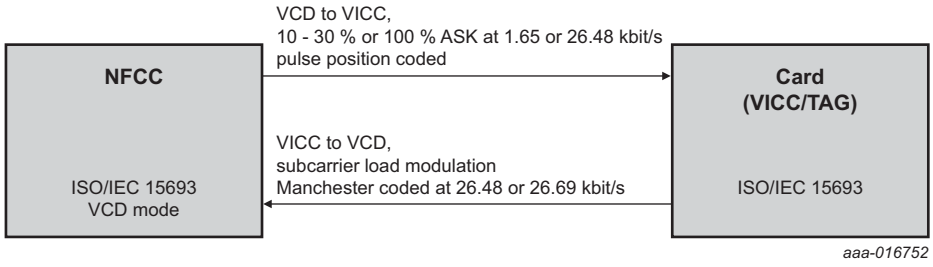

Fig 23. ISO/IEC 15693 VCD communication mode diagram

Figure 23 shows the communication schemes used.

2 communication schemes can be used from card to PN7120 and 2 communication schemes can be used from PN7120 to card.

Thus, 4 communication schemes are possible.

Table 17. Overview for ISO/IEC 15693 VCD communication mode

Communication direction			
PN7120 → VICC			
(data sent by PN7120 to a tag)	transfer speed	1.65 kbit/s	26.48 kbit/s
	bit length	(8192/13.56) µs	(512/13.56) µs
	modulation on PN7120 side	10 % – 30 % or 100 % ASK	10 % – 30 % or 100 % ASK
	bit coding	pulse position modulation 1 out of 256 mode	pulse position modulation 1 out of 4 mode

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Table 17. Overview for ISO/IEC 15693 VCD communication mode *…continued*

Communication direction			
VICC → PN7120			
(data received by PN7120 from a tag)	transfer speed	26.48 kbit/s	26.69 kbit/s
	bit length	(512/13.56) μs	(508/13.56) μs
	modulation on VICC side	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	single subcarrier	dual subcarrier
	bit coding	Manchester	Manchester

10.7.2 ISO/IEC 18092, Ecma 340 NFCIP-1 communication modes

An NFCIP-1 communication takes place between 2 devices:

- NFC Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
- NFC Target: responds to NFC Initiator command either in a load modulation scheme in Passive communication mode or using a self-generated and self-modulated RF field for Active communication mode.

The NFCIP-1 communication differentiates between Active and Passive communication modes.

- Active communication mode means both the NFC Initiator and the NFC Target are using their own RF field to transmit data
- Passive communication mode means that the NFC Target answers to an NFC Initiator command in a load modulation scheme. The NFC Initiator is active in terms of generating the RF field.

PN7120 supports the Active Target, Active Initiator, Passive Target and Passive Initiator communication modes at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard.

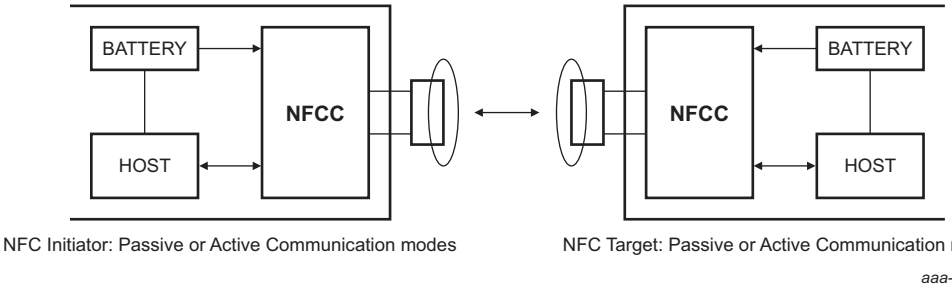

Fig 24. NFCIP-1 communication mode

Nevertheless a dedicated external host has to handle the application layer communication.

10.7.2.1 ACTIVE communication mode

Active communication mode means both the NFC Initiator and the NFC Target are using their own RF field to transmit data.

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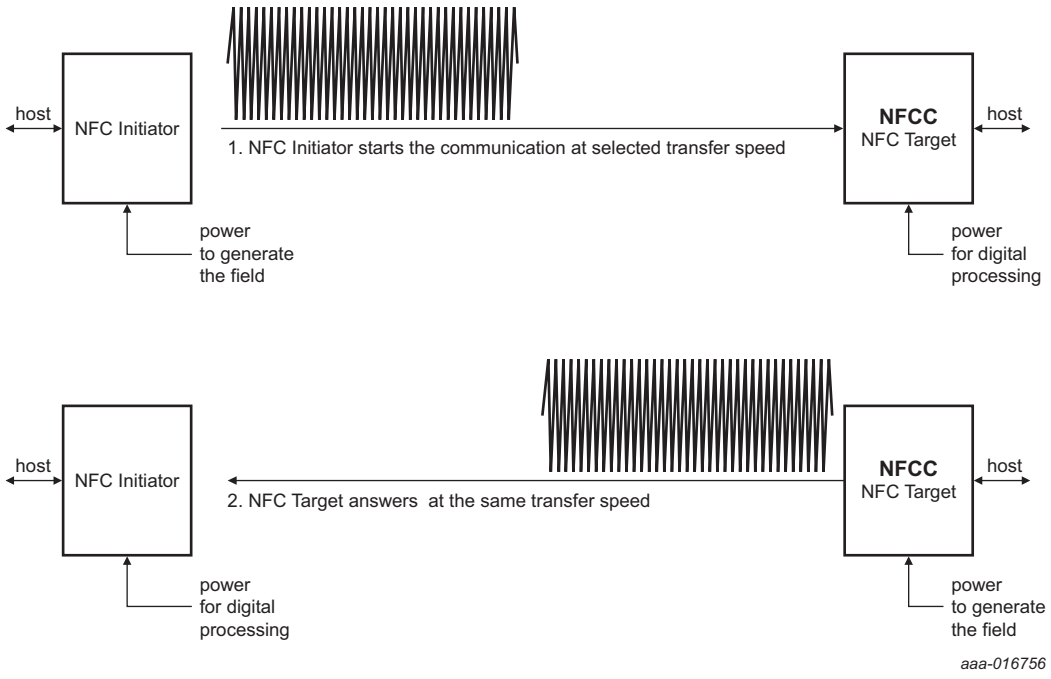

Fig 25. Active communication mode

The following table gives an overview of the Active communication modes:

Table 18. Overview for Active communication mode

Communication direction		ISO/IEC 18092, Ecma 340, NFCIP-1		
	Baud rate	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**
NFC Initiator to NFC Target				
	modulation	100 % ASK	8 % – 30 % ASK[1]	8 % – 30 % ASK[1]
	bit coding	Modified Miller	Manchester	Manchester
NFC Target to NFC Initiator				
	modulation	100 % ASK	8 % – 30 % ASK[1]	8 % – 30 % ASK[1]
	bit coding	Miller	Manchester	Manchester

[1] This modulation index range is according to NFCIP-1 standard. It might be that some NFC forum type 3 cards does not withstand the full range as based on FeliCa range which is narrow (8 % to 14 % ASK). To adjust the index, see Ref. 6.

10.7.2.2 Passive communication mode

Passive communication mode means that the NFC Target answers to an NFC Initiator command in a load modulation scheme.

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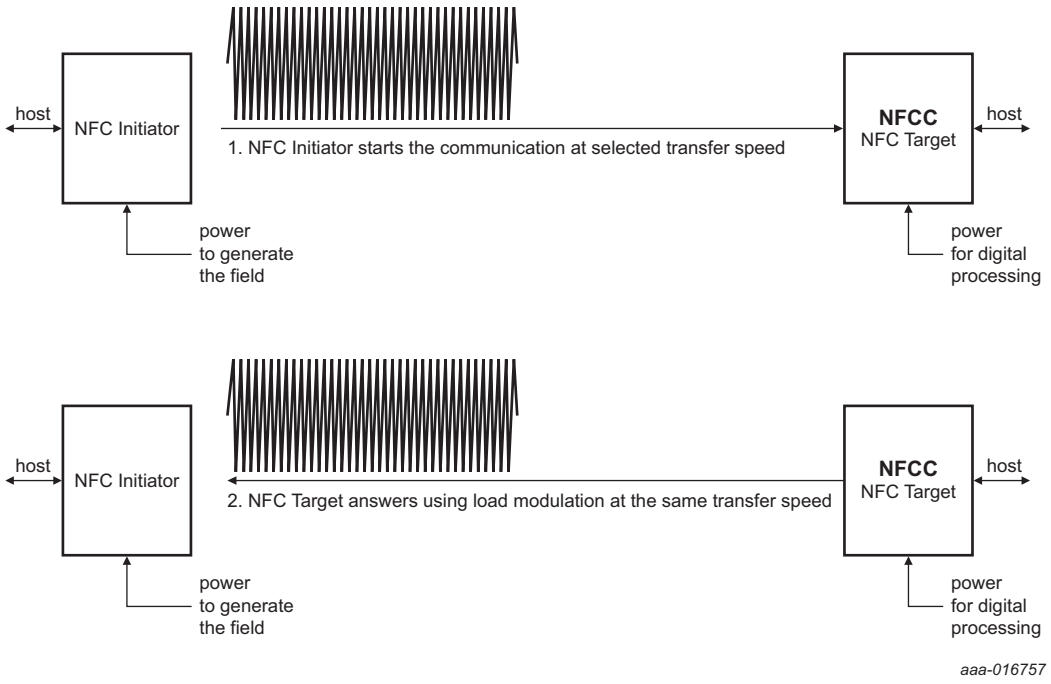

Fig 26. Passive communication mode

Table 19 gives an overview of the Passive communication modes:

Table 19. Overview for Passive communication mode

Communication direction		ISO/IEC 18092, Ecma 340, NFCIP-1		
	Baud rate	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**
NFC Initiator to NFC Target				
	modulation	100 % ASK	8 % – 30 % ASK[1]	8 % – 30 % ASK[1]
	bit coding	Modified Miller	Manchester	Manchester
NFC Target to NFC Initiator				
	modulation	subcarrier load modulation	load modulation	load modulation
	subcarrier frequency	13.56 MHz/16	no subcarrier	no subcarrier
	bit coding	Manchester	Manchester	Manchester

[1] This modulation index range is according to NFCIP-1 standard. It might be that some NFC forum type 3 cards does not withstand the full range as based on FeliCa range which is narrow (8 % to 14 % ASK). To adjust the index, see Ref. 6.

10.7.2.3 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive communication modes are defined in the NFCIP-1 standard: ISO/IEC 18092 or Ecma 340.

10.7.2.4 NFCIP-1 protocol support

The NFCIP-1 protocol is not completely described in this document. For detailed explanation of the protocol, refer to the ISO/IEC 18092 or Ecma 340 NFCIP-1 standard. However the datalink layer is according to the following policy:

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- Transaction includes initialization, anticollision methods and data transfer. This sequence must not be interrupted by another transaction
- PSL shall be used to change the speed between the target selection and the data transfer, but the speed should not be changed during a data transfer

10.7.3 Card communication modes

PN7120 can be addressed as a ISO/IEC 14443A or ISO/IEC 14443B cards. This means that PN7120 can generate an answer in a load modulation scheme according to the ISO/IEC 14443A or ISO/IEC 14443B interface description.

Remark: PN7120 does not support a complete card protocol. This has to be handled by the host controller.

Table 20 and Table 21 describe the physical parameters.

10.7.3.1 ISO/IEC 14443A/MIFARE card communication mode

Table 20. Overview for ISO/IEC 14443A/MIFARE card communication mode

Communication direction		ISO/IEC 14443A	ISO/IEC 14443A higher transfer speeds	
	Transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**
PCD → PN7120				
(data received by PN7120 from a card)	modulation on PCD side	100 % ASK	> 25 % ASK	> 25 % ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller
PN7120 → PCD				
(data sent by PN7120 to a card)	modulation on PN7120 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester	BPSK	BPSK

10.7.3.2 ISO/IEC 14443B card communication mode

Table 21. Overview for ISO/IEC 14443B card communication mode

Communication direction		ISO/IEC 14443B	ISO/IEC 14443B higher transfer speeds	
	Transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**
PCD → PN7120				
(data received by PN7120 from a Reader)	modulation on PCD side	8 % – 14 % ASK	8 % – 14 % ASK	8 % – 14 % ASK
	bit coding	NRZ	NRZ	NRZ
PN7120 → PCD				
(data sent by PN7120 to a Reader)	modulation on PN7120 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	BPSK	BPSK	BPSK

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10.7.4 Frequency interoperability

When in communication, PN7120 is generating some RF frequencies. PN7120 is also sensitive to some RF signals as it is looking from data in the field.

In order to avoid interference with others RF communication, it is required to tune the antenna and design the board according to Ref. 5.

Although ISO/IEC 14443 and ISO/IEC 18092/Ecma 340 allows an RF frequency of 13.56 MHz ± 7 kHz, FCC regulation does not allow this wide spread and limits the dispersion to ± 50 ppm, which is in line with PN7120 capability.

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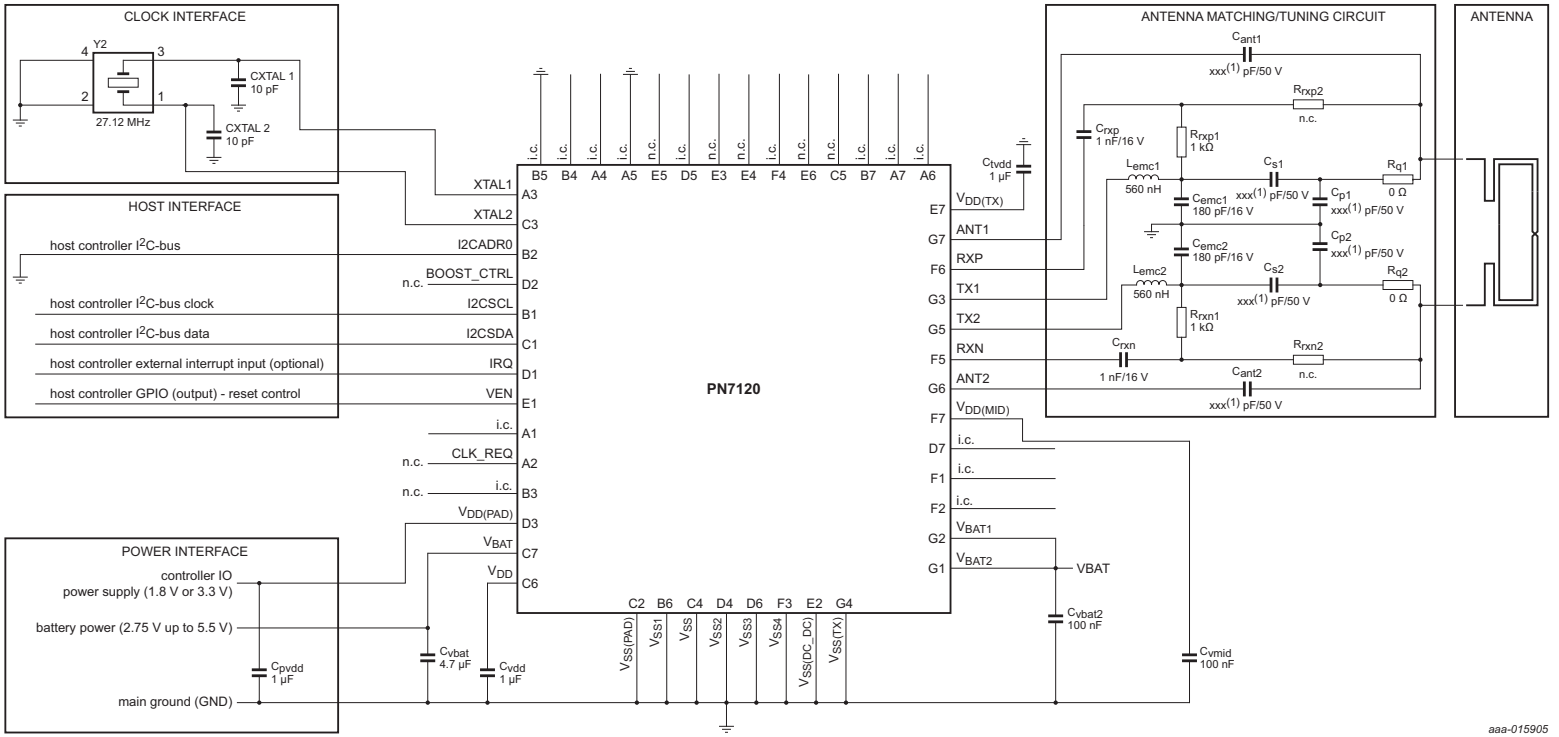
11. Application design-in information



(1) xxx: customer antenna matching tuning.

Fig 27. Application schematic

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12. Limiting values

Table 22. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(PAD)}$	$V_{DD(PAD)}$ supply voltage	supply voltage for host interface	-	4.2	V
V_{BAT}	battery supply voltage		-	6	V
V_{ESD}	electrostatic discharge voltage	HBM; 1500 Ω, 100 pF; EIA/JESD22-A114-D	-	1.5	kV
		CDM; field induced model; EIA/JESC22-C101-C	-	500	V
T_{stg}	storage temperature		−55	+150	°C
P_{tot}	total power dissipation	all modes [1]	-	0.55	W
$V_{RXN(i)}$	RXN input voltage		0	2.5	V
$V_{RXP(i)}$	RXP input voltage		0	2.5	V

[1] The design of the solution shall be done so that for the different use cases targeted the power to be dissipated from the field or generated by PN7120 does not exceed this value.

13. Recommended operating conditions

Table 23. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient temperature	JEDEC PCB-0.5	−30	+25	+85	°C
V_{BAT}	battery supply voltage	battery monitor enabled; V_{SS} = 0 V [1]	2.3	-	5.5	V
		Card Emulation and Passive Target; V_{SS} = 0 V [1] [2]	2.3	-	5.5	V
		Reader, Active Initiator and Active Target; V_{SS} = 0 V [1] [2]	2.7	-	5.5	V
V_{DD}	supply voltage		1.65	1.8	1.95	V
$V_{DD(PAD)}$	$V_{DD(PAD)}$ supply voltage	supply voltage for host interface				
		1.8 V host supply; V_{SS} = 0 V [1]	1.65	1.8	1.95	V
		3 V host supply; V_{SS} = 0 V [1]	3.0	-	3.6	V
P_{tot}	total power dissipation	Reader; $I_{VDD(TX)}$ = 100 mA; V_{BAT} = 5.5 V	-	-	0.5	W
$I_{O(VDDTX)}$	output current on pin $V_{DD(TX)}$	[2]	-	-	100	mA

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Table 23. Operating conditions *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{BAT}	battery supply current	in Hard Power Down state; V_{BAT} = 3.6 V; T = 25 °C	-	10	12	µA
		in Standby state; V_{BAT} = 3.6 V; T = 25 °C	-	-	20	µA
		in Monitor state; V_{BAT} = 2.75 V; T = 25 °C	-	-	12	µA
		in low-power polling loop; V_{BAT} = 3.6 V; T = 25 °C; loop time = 500 ms	-	150	-	µA
$I_{VBAT(tot)}$	total supply current on V_{BAT}	PCD mode at typical 3 V [3]	-	-	170	mA
$I_{th(Ilim)}$	current limit threshold current	current limiter on $V_{DD(TX)}$ pin; $V_{DD(TX)}$ = 3.1 V [3] [4]	-	180	-	mA

[1] V_{SS} represents V_{SS}, V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}, $V_{SS(PAD)}$ and $V_{SS(TX)}$.

[2] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account).

[3] The antenna shall be tuned not to exceed the maximum of I_{VBAT}.

[4] This is the threshold of a built-in protection done to limit the current out of $V_{DD(TX)}$ in case of any issue at antenna pins to avoid burning the device. It is not allowed in operational mode to have $I_{VDD(TX)}$ such that I_{VBAT} maximum value is exceeded.

14. Thermal characteristics

Table 24. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB		-	74	-	K/W

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15. Characteristics

15.1 Current consumption characteristics

Table 25. Current consumption characteristics for operating ambient temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{BAT}	battery supply current	in Hard Power Down state; V_{BAT} = 3.6 V; VEN voltage = 0 V	-	10	18	µA
		in Standby state; [1] V_{BAT} = 3.6 V; including emulation phase of polling loop	-	20	35	µA
		in Idle and Target Active power states; [2] V_{BAT} = 3.6 V	-	6	-	mA
		in Initiator Active power state; [2] V_{BAT} = 3.6 V	-	13	-	mA
		in Monitor state; [3] V_{BAT} = 2.75 V	-	10	18	µA
$I_{O(VDDTX)}$	output current on pin $V_{DD(TX)}$	[4] [5]	-	30	100	mA
$I_{O(VDDPAD)}$	output current on pin $V_{DD(PAD)}$	total current which can be pulled on $V_{DD(PAD)}$ referenced outputs	-	-	15	mA

[1] Refer to Section 10.1.2.4 for the description of the power modes.

[2] Refer to Section 10.1.2.5 for the description of the polling loop.

[3] This is the same value for V_{BAT} = 2.3 V when the monitor threshold is set to 2.3 V.

[4] $I_{VDD(TX)}$ depends on $V_{DD(TX)}$ and on the external circuitry connected to TX1 and TX2.

[5] During operation with a typical circuitry as recommended by NXP in Ref. 6, the overall current is below 100 mA even when loaded by target/card/tag.

15.2 Functional block electrical characteristics

15.2.1 Battery voltage monitor characteristics

Table 26. Battery voltage monitor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	set to 2.3 V	2.2	2.3	2.4	V
		set to 2.75 V	2.65	2.75	2.85	V
V_{hys}	hysteresis voltage		100	150	200	mV

15.2.2 Reset via VEN

Table 27. Reset timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{W(VEN)}$	VEN pulse width	to reset	3	-	-	µs
t_{boot}	boot time		-	-	2.5	ms

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15.2.3 Power-up timings

Table 28. Power-up timings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{t(VBAT-VEN)}$	transition time from pin V_{BAT} to pin VEN	V_{BAT}, VEN voltage = HIGH	0	-	-	ms
$t_{t(VDDPAD-VEN)}$	transition time from pin $V_{DD(PAD)}$ to pin VEN	$V_{DD(PAD)}$, VEN voltage = HIGH	0	-	-	ms
$t_{t(VBAT-VDDPAD)}$	transition time from pin V_{BAT} to pin $V_{DD(PAD)}$	V_{BAT}, $V_{DD(PAD)}$ = HIGH	0	-	-	ms

15.2.4 Power-down timings

Table 29. Power-down timings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{VBAT(L)}$	time V_{BAT} LOW		20	-	-	ms

15.2.5 Thermal protection

Table 30. Thermal threshold

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{th(act)otp}$	overtemperature protection activation threshold temperature		120	125	130	°C

15.2.6 I²C-bus timings

Here below are timings and frequency specifications.

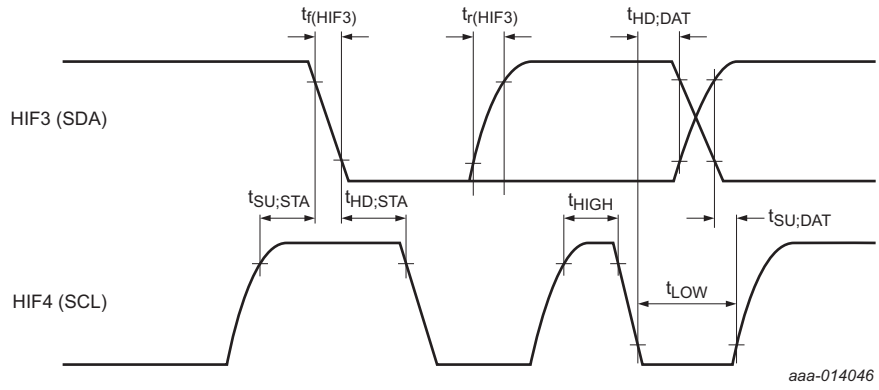

Fig 28. I²C-bus timings

Table 31. High-speed mode I²C-bus timings specification

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{clk(I2CSCL)}$	clock frequency on pin I2CSCL	I²C-bus SCL; C_b < 100 pF	0	3.4	MHz
$t_{SU;STA}$	set-up time for a repeated START condition	C_b < 100 pF	160	-	ns
$t_{HD;STA}$	hold time (repeated) START condition	C_b < 100 pF	160	-	ns

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Table 31. High-speed mode I²C-bus timings specification *…continued*

Symbol	Parameter	Conditions	Min	Max	Unit
t_{LOW}	LOW period of the SCL clock	C_b < 100 pF	160	-	ns
t_{HIGH}	HIGH period of the SCL clock	C_b < 100 pF	60	-	ns
$t_{SU;DAT}$	data set-up time	C_b < 100 pF	10	-	ns
$t_{HD;DAT}$	data hold time	C_b < 100 pF	0	-	ns
$t_{r(I2CSDA)}$	rise time on pin I2CSDA	I²C-bus SDA; C_b < 100 pF	10	80	ns
$t_{f(I2CSDA)}$	fall time on pin I2CSDA	I²C-bus SDA; C_b < 100 pF	10	80	ns
V_{hys}	hysteresis voltage	Schmitt trigger inputs; C_b < 100 pF	$0.1V_{DD(PAD)}$	-	V

Table 32. Fast mode I²C-bus timings specification

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{clk(I2CSCL)}$	clock frequency on pin I2CSCL	I²C-bus SCL; C_b < 400 pF	0	400	kHz
$t_{SU;STA}$	set-up time for a repeated START condition	C_b < 400 pF	600	-	ns
$t_{HD;STA}$	hold time (repeated) START condition	C_b < 400 pF	600	-	ns
t_{LOW}	LOW period of the SCL clock	C_b < 400 pF	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	C_b < 400 pF	600	-	ns
$t_{SU;DAT}$	data set-up time	C_b < 400 pF	100	-	ns
$t_{HD;DAT}$	data hold time	C_b < 400 pF	0	900	ns
V_{hys}	hysteresis voltage	Schmitt trigger inputs; C_b < 400 pF	$0.1V_{DD(PAD)}$	-	V

15.3 Pin characteristics

15.3.1 XTAL1 and XTAL2 pins characteristics

Table 33. Input clock characteristics on XTAL1 when using PLL

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(p-p)}$	peak-to-peak input voltage		0.2	-	1.8	V
δ	duty cycle		35	-	65	%

Table 34. Pin characteristics for XTAL1 when PLL input

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH-level input current	$V_I = V_{DD}$	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0 V	1	-	-	µA
V_i	input voltage		-	-	V_{DD}	V
$V_{i(clk)(p-p)}$	peak-to-peak clock input voltage		200	-	-	mV
C_i	input capacitance	all power modes	-	2	-	pF

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Table 35. Pin characteristics for 27.12 MHz crystal oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{i(XTAL1)}$	XTAL1 input capacitance	V_{DD} = 1.8 V; V_{DC} = 0.65 V; V_{AC} = 0.9 V(p-p)	-	2	-	pF
$C_{i(XTAL2)}$	XTAL2 input capacitance		-	2	-	pF

[1] See the Figure 27 for example of appropriate connected components. The layout should ensure minimum distance between the pins and the components.

Table 36. PLL accuracy

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{o(acc)}$	output frequency accuracy	deviation added to XTAL1 frequency on RF frequency generated; worst case whatever input frequency	–50	-	+50	ppm

15.3.2 VEN input pin characteristics

Table 37. VEN input pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		1.1	-	V_{BAT}	V
V_{IL}	LOW-level input voltage		0	-	0.4	V
I_{IH}	HIGH-level input current	VEN voltage = V_{BAT}	-	-	1	µA
I_{IL}	LOW-level input current	VEN voltage = 0 V	1	-	-	µA
C_i	input capacitance		-	5	-	pF

15.3.3 Pin characteristics for IRQ, CLK_REQ and BOOST_CTRL

Table 38. pin characteristics for IRQ, CLK_REQ and BOOST_CTRL

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} < 3 mA	$V_{DD(PAD)}$ – 0.4	-	$V_{DD(PAD)}$	V
V_{OL}	LOW-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
C_L	load capacitance		-	-	20	pF
t_f	fall time	C_L = 12 pF max				
		high speed	1	-	3.5	ns
		slow speed	2	-	10	ns
t_r	rise time	C_L = 12 pF max				
		high speed	1	-	3.5	ns
		slow speed	2	-	10	ns
R_{pd}	pull-down resistance	[1]	0.4	-	0.75	MΩ

[1] Activated in HPD and Monitor states.

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15.3.4 ANT1 and ANT2 pin characteristics

Table 39. Electrical characteristics of ANT1 and ANT2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Z_{i(ANT1-ANT2)}$	input impedance between ANT1 and ANT2	low impedance	-	10	17	Ω
$V_{th(ANT1)}$	ANT1 threshold voltage	I = 10 mA	-	3.3	-	V
$V_{th(ANT2)}$	ANT2 threshold voltage	I = 10 mA	-	3.3	-	V

15.3.5 Input pin characteristics for RXN and RXP

Table 40. Input pin characteristics for RXN and RXP

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RXN(i)}$	RXN input voltage		0	-	V_{DD}	V
$V_{RXP(i)}$	RXP input voltage		0	-	V_{DD}	V
$C_{i(RXN)}$	RXN input capacitance		-	12	-	pF
$C_{i(RXP)}$	RXP input capacitance		-	12	-	pF
$Z_{i(RXN-VDDMID)}$	input impedance between RXN and $V_{DD(MID)}$	Reader, Card and P2P modes	0	-	15	kΩ
$Z_{i(RXP-VDDMID)}$	input impedance between RXP and $V_{DD(MID)}$	Reader, Card and P2P modes	0	-	15	kΩ
$V_{i(dyn)(RXN)}$	RXN dynamic input voltage	Miller coded				
		106 kbit/s	-	150	200	mV(p-p)
		212 to 424 kbit/s	-	150	200	mV(p-p)
$V_{i(dyn)(RXP)}$	RXP dynamic input voltage	Miller coded				
		106 kbit/s	-	150	200	mV(p-p)
		212 to 424 kbit/s	-	150	200	mV(p-p)
$V_{i(dyn)(RXN)}$	RXN dynamic input voltage	Manchester, NRZ or BPSK coded; 106 to 848 kbit/s	-	150	200	mV(p-p)
$V_{i(dyn)(RXP)}$	RXP dynamic input voltage	Manchester, NRZ or BPSK coded; 106 to 848 kbit/s	-	150	200	mV(p-p)
$V_{i(dyn)(RXN)}$	RXN dynamic input voltage	All data coding; 106 kbit/s to 848 kbit/s	V_{DD}	-	-	V(p-p)
$V_{i(dyn)(RXP)}$	RXP dynamic input voltage	All data coding; 106 kbit/s to 848 kbit/s	V_{DD}	-	-	V(p-p)
$V_{i(RF)}$	RF input voltage	RF input voltage detected; Initiator modes		100	-	mV(p-p)

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15.3.6 Output pin characteristics for TX1 and TX2

Table 41. Output pin characteristics for TX1 and TX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(TX)}$ = 3.1 V and I_{OH} = 30 mA; PMOS driver fully on	$V_{DD(TX)}$ − 150	-	-	mV
V_{OL}	LOW-level output voltage	$V_{DD(TX)}$ = 3.1 V and I_{OL} = 30 mA; NMOS driver fully on	-	-	200	mV

Table 42. Output resistance for TX1 and TX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{OL}	LOW-level output resistance	$V_{DD(TX)}$ − 100 mV; CWGsN = 01h	-	-	80	Ω
R_{OL}	LOW-level output resistance	$V_{DD(TX)}$ − 100 mV; CWGsN = 0Fh	-	-	5	Ω
R_{OH}	HIGH-level output resistance	$V_{DD(TX)}$ − 100 mV	-	-	4	Ω

15.3.7 Input pin characteristics for I2CADR0

Table 43. Input pin characteristics for I2CADR0

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.65V_{DD(PAD)}$	-	$V_{DD(PAD)}$	V
V_{IL}	LOW-level input voltage		0	-	$0.35V_{DD(PAD)}$	V
I_{IH}	HIGH-level input current	$V_I = V_{DD(PAD)}$; T = 125 °C	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0 V; T = 125 °C	−1	-	-	µA
C_i	input capacitance		-	5	-	pF

15.3.8 Pin characteristics for I2CSDA and I2CSCL

Table 44. Pin characteristics for I2CSDA and I2CSCL

Below values are given for $V_{DD(PAD)}$ in the range of 1.8 V; unless specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
C_L	load capacitance		-	-	10	pF

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Table 44. Pin characteristics for I2CSDA and I2CSCL *…continued*

Below values are given for $V_{DD(PAD)}$ in the range of 1.8 V; unless specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	fall time	C_L = 100 pF; Rpull-up = 1.8 kΩ; Standard and Fast mode	30	-	250	ns
		C_L = 100 pF; $V_{DD(PAD)}$ = 3.3 V; Rpull-up = 3.3 kΩ; Standard and Fast mode	30	-	250	ns
		C_L = 100 pF; Rpull-up = 1 kΩ; High-speed mode	80	-	110	ns
t_r	rise time	C_L = 100 pF; Rpull-up = 1.8 kΩ; Standard and Fast mode	30	-	250	ns
		C_L = 100 pF; $V_{DD(PAD)}$ = 3.3 V; Rpull-up = 3.3 kΩ; Standard and Fast mode	30	-	250	ns
		C_L = 100 pF; Rpull-up = 1 kΩ; High-speed mode	10	-	100	ns
V_{IH}	HIGH-level input voltage		$0.7V_{DD(PAD)}$	-	$V_{DD(PAD)}$	V
V_{IL}	LOW-level input voltage		0	-	$0.3V_{DD(PAD)}$	V
I_{IH}	HIGH-level input current	$V_I = V_{DD(PAD)}$; high impedance	-	-	1	μA
I_{IL}	LOW-level input current	V_I = 0 V; high impedance	−1	-	-	μA
C_i	input capacitance		-	5	-	pF

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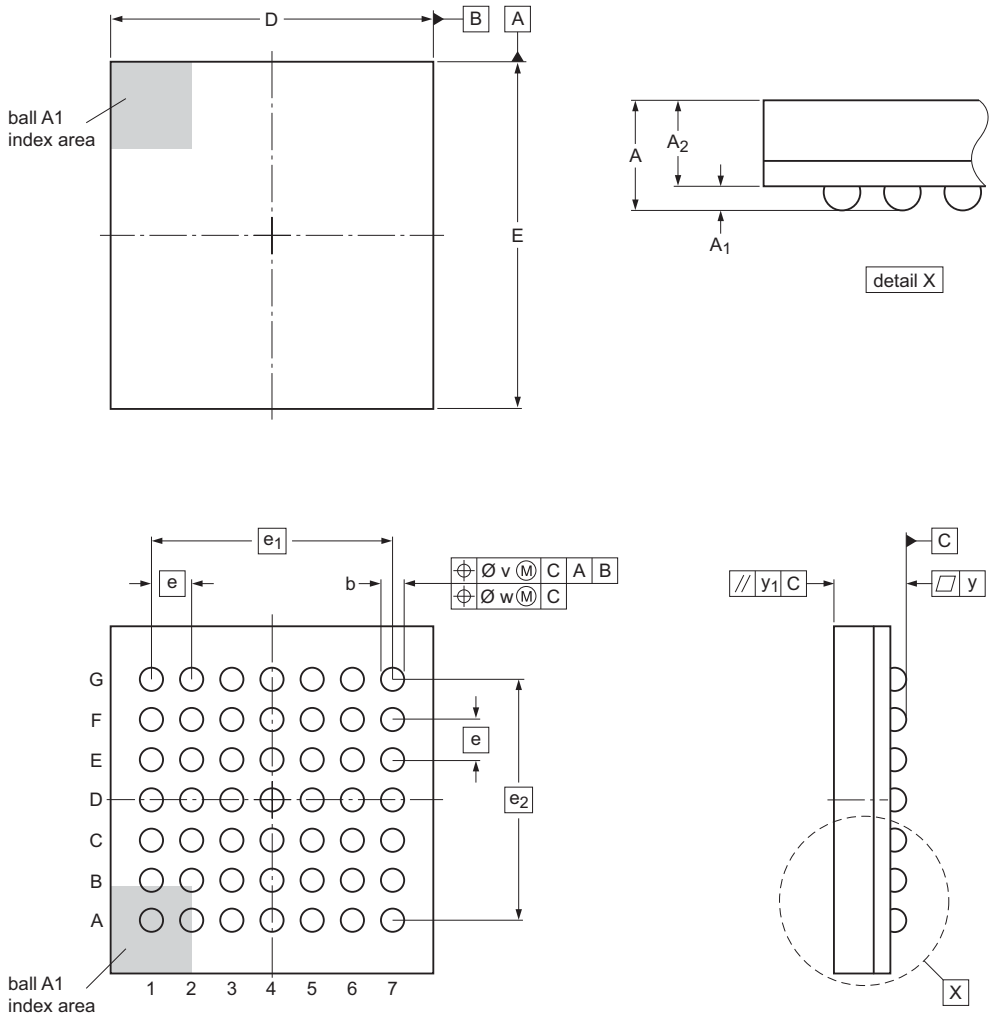
16. Package outline

VFBGA49: plastic very thin fine-pitch ball grid array package; 49 balls **SOT1320-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.00	0.25	0.75	0.35	4.1	4.4							
	nom	0.90	0.20	0.70	0.30	4.0	4.3	0.5	3.0	3.0	0.15	0.05	0.08	0.1
	min	0.80	0.15	0.65	0.25	3.9	4.2							

sot1320-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1320-1						~~11-11-11~~ 11-12-30

Fig 29. Package outline, VFBGA49, SOT1320-1, MSL 1

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17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 30) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 45 and 46

Table 45. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 46. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 30.

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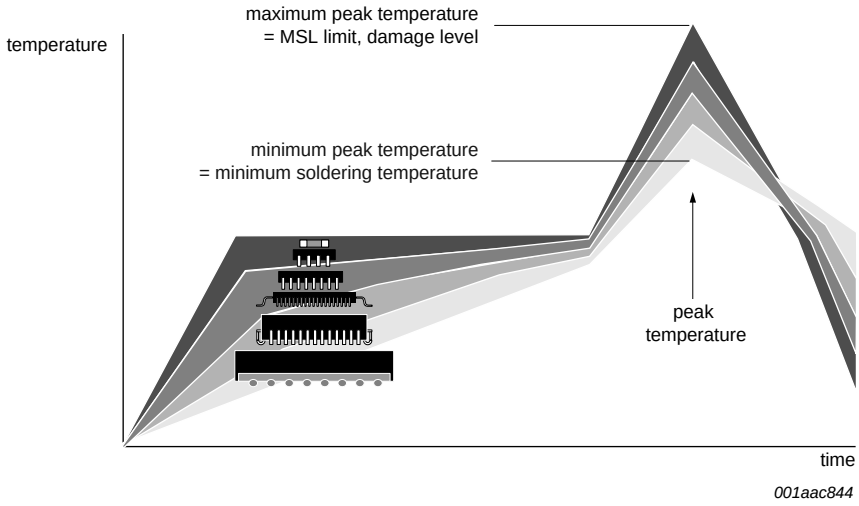

MSL: Moisture Sensitivity Level

Fig 30. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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18. Abbreviations

Table 47. Abbreviations

Acronym	Description
API	Application Programming Interface
ASK	Amplitude Shift keying
ASK modulation index	The ASK modulation index is defined as the voltage ratio (Vmax - Vmin)/ (Vmax + Vmin) × 100 %
Automatic device discovery	Detect and recognize any NFC peer devices (initiator or target) like: NFC initiator or target, ISO/IEC 14443-3, -4 Type A&B PICC, MIFARE Standard and Ultralight PICC, ISO/IEC 15693 VICC
BPSK	Bit Phase Shift Keying
Card Emulation	The IC is capable of handling a PICC emulation on the RF interface including part of the protocol management. The application handling is done by the host controller
DEP	Data Exchange Protocol
DSLDO	Dual Supplied LDO
FW	FirmWare
HPD	Hard Power Down
LDO	Low Drop Out
LFO	Low Frequency Oscillator
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSL	Moisture Sensitivity Level
NCI	NFC Controller Interface
NFC	Near Field Communication
NFCC	NFC Controller, PN7120 in this data sheet
NFC Initiator	Initiator as defined in ISO/IEC 18092 or ECma 340: NFCIP-1 communication
NFCIP	NFC Interface and Protocol
NFC Target	Target as defined in ISO/IEC 18092 or ECma 340: NFCIP-1 communication
NRZ	Non Return to Zero
P2P	Peer to Peer
PCD	Proximity Coupling Device. Definition for a Card reader/writer device according to the ISO/IEC 14443 specification or MIFARE
PCD -> PICC	Communication flow between a PCD and a PICC according to the ISO/IEC 14443 specification or MIFARE
PICC	Proximity Interface Coupling Card. Definition for a contactless Smart Card according to the ISO/IEC 14443 specification or MIFARE
PICC-> PCD	Communication flow between a PICC and a PCD according to the ISO/IEC 14443 specification or MIFARE
PMOS	P-channel MOSFET
PMU	Power Management Unit
PSL	Parameter SeLection
TXLDO	Transmitter LDO
UM	User Manual

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Table 47. Abbreviations *…continued*

Acronym	Description
VCD	Vicinity Coupling Device. Definition for a reader/writer device according to the ISO/IEC 15693 specification
VCO	Voltage Controlled Oscillator
VICC	Vicinity Integrated Circuit Card
WUC	Wake-Up Counter

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19. References

[1] **NFC Controller Interface (NCI) Technical Specification —** V1.0

[2] **ISO/IEC 14443 —** parts 2: 2001 COR 1 2007 (01/11/2007), part 3: 2001 COR 1 2006 (01/09/2006) and part 4: 2nd edition 2008 (15/07/2008)

[3] **I²C Specification —** I²C Specification, UM10204 rev4 (13/02/2012)

[4] **PN7120 User Manual —** UM10819 PN7120 User Manual

[5] **PN7120 Hardware Design Guide —** AN11565 PN7120 Hardware Design Guide

[6] **PN7120 Antenna and Tuning Design Guide —** AN11564 PN7120 Antenna and Tuning Design Guide

[7] **ISO/IEC 18092 (NFCIP-1) —** edition, 15/032013. This is similar to Ecma 340.

[8] **ISO/IEC15693 —** part 2: 2nd edition (15/12/2006), part 3: 1st edition (01/04/2001)

[9] **PN7120 Low-Power Mode Configuration —** AN11562 PN7120 Low-Power Mode Configuration

[10] **ISO/IEC 21481 (NFCIP-2) —** edition, 01/07/2012. This is similar to Ecma 352.

[11] **NFC Forum Device Requirements —** V1.3

[12] **ETSI SWP —** TS 102 613; UICC - Contacless Front-end (CLF) Interface; Part 1: Physical and data link layer characteristics (Release 9)

[13] **ETSI HCI —** TS 102 622; UICC - Contacless Front-end (CLF) Interface; Host Controller Interface (HCI) (Release 9)

[14] **ETSI UICC —** TS 102 221; UICC - Terminal Interface; Physical and logical characteristics (Release 9)

[15] **EMVCo —** EMV Contactless Specifications for Payment Systems - Book D - EMV Contactless Communication Protocol Specification”, version 2.3.1, December 2013

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20. Revision history

Table 48. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PN7120 v.2	20150615	Preliminary data sheet	-	PN7120 v.1
Modifications:	• Table 33: updated.			
PN7120 v.1	20150506	Objective data sheet	-	-

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 15 June 2015
312420