

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4511 BCD to 7-segment latch/decoder/driver

Product specification
File under Integrated Circuits, IC06

December 1990

BCD to 7-segment latch/decoder/driver

74HC/HCT4511

FEATURES

- Latch storage of BCD inputs
- Blanking input
- Lamp test input
- Driving common cathode LED displays
- Guaranteed 10 mA drive capability per output
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4511 are high-speed Si-gate CMOS devices and are pin compatible with "4511" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4511 are BCD to 7-segment latch/decoder/drivers with four address inputs (D₁ to D₄), an active LOW latch enable input (\overline{LE}), an active LOW

ripple blanking input (\overline{BI}), an active LOW lamp test input (\overline{LT}), and seven active HIGH segment outputs (Q_a to Q_g).

When \overline{LE} is LOW, the state of the segment outputs (Q_a to Q_g) is determined by the data on D₁ to D₄.

When \overline{LE} goes HIGH, the last data present on D₁ to D₄ are stored in the latches and the segment outputs remain stable.

When \overline{LT} is LOW, all the segment outputs are HIGH independent of all other input conditions. With \overline{LT} HIGH, a LOW on \overline{BI} forces all segment outputs LOW. The inputs \overline{LT} and \overline{BI} do not affect the latch circuit.

APPLICATIONS

- Driving LED displays
- Driving incandescent displays
- Driving fluorescent displays
- Driving LCD displays
- Driving gas discharge displays

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay	C _L = 15 pF; V _{CC} = 5 V			
	D _n to Q _n		24	24	ns
	\overline{LE} to Q _n		23	24	ns
	\overline{BI} to Q _n		19	20	ns
	\overline{LT} to Q _n		12	13	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	64	64	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}

For HCT the condition is V_I = GND to V_{CC} – 1.5 V

BCD to 7-segment latch/decoder/driver

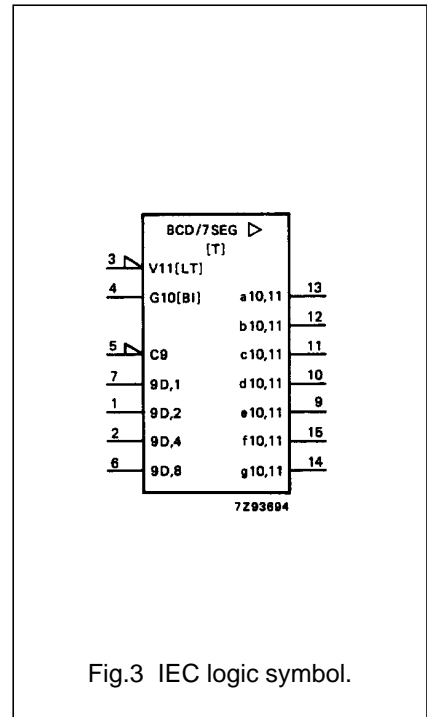
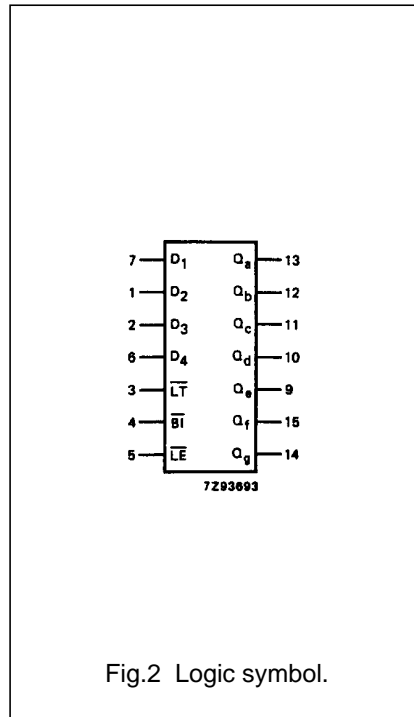
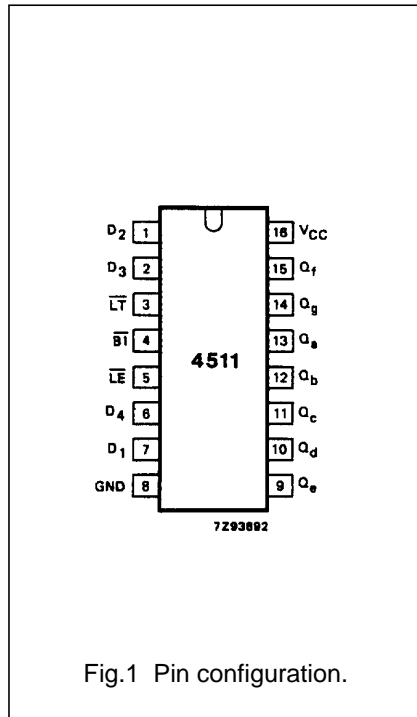
74HC/HCT4511

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

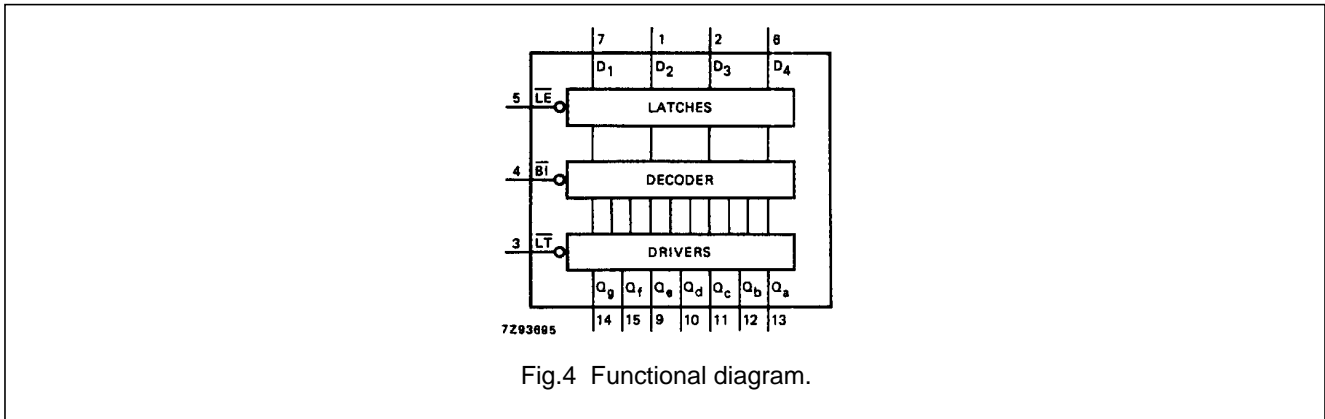
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3	\overline{LT}	lamp test input (active LOW)
4	\overline{BI}	ripple blanking input (active LOW)
5	\overline{LE}	latch enable input (active LOW)
7, 1, 2, 6	D ₁ to D ₄	BCD address inputs
8	GND	ground (0 V)
13, 12, 11, 10, 9, 15, 14	Q _a to Q _g	segments outputs
16	V _{CC}	positive supply voltage



BCD to 7-segment latch/decoder/driver

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FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
\overline{LE}	\overline{BI}	\overline{LT}	D ₄	D ₃	D ₂	D ₁	Q _a	Q _b	Q _c	Q _d	Q _e	Q _f	Q _g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X	(1)							(1)

Note

- Depends upon the BCD-code applied during the LOW-to-HIGH transition of \overline{LE} .
 H = HIGH voltage level
 L = LOW voltage level
 X = don't care

BCD to 7-segment latch/decoder/driver

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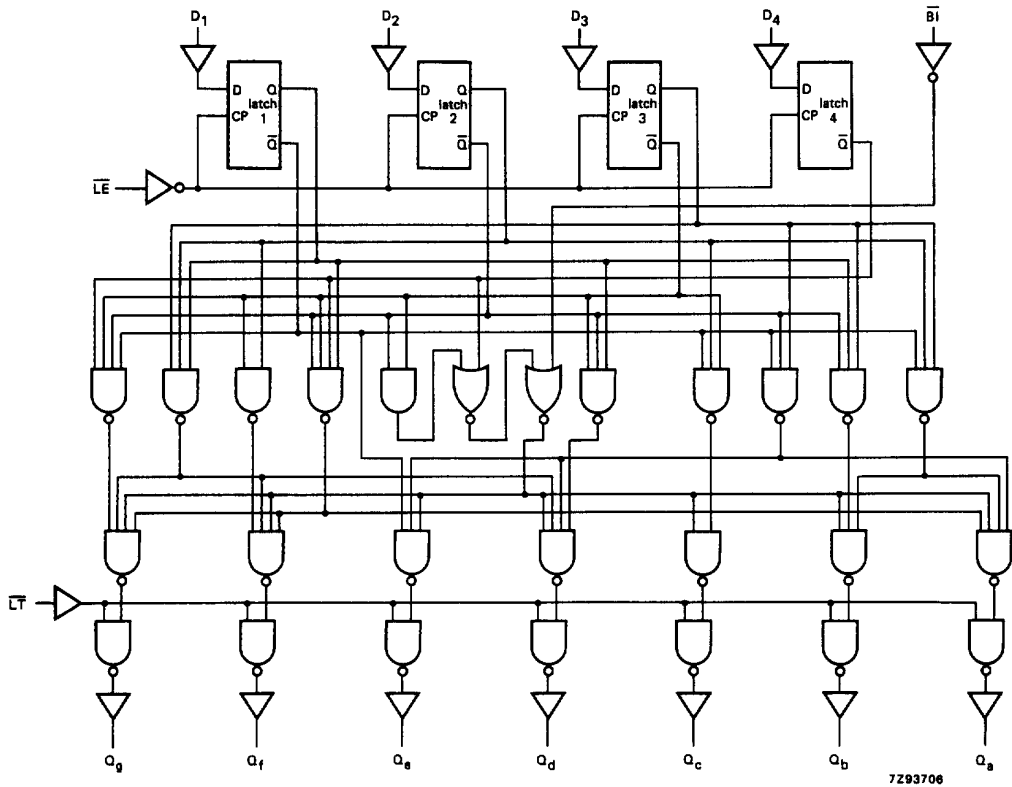


Fig.5 Logic diagram.

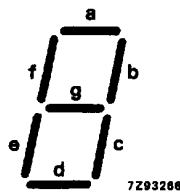


Fig.6 Segment designation.

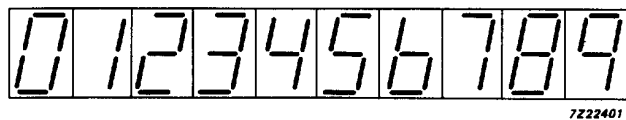


Fig.7 Display.

BCD to 7-segment latch/decoder/driver

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard, excepting V_{OH} which is given below
 I_{CC} category: MSI

Non-standard DC characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	V_I	$-I_o$ (mA)
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{OH}	HIGH level output voltage	3.98			3.84		3.70		V	4.5	V_{IH} or V_{IL}	7.5 10.0
V_{OH}	HIGH level output voltage	5.60			5.45		5.35		V	6.0	V_{IH} or V_{IL}	7.5 10.0 15.0

BCD to 7-segment latch/decoder/driver

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AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V_{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		77 28 22	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig.8
t_{PHL}/t_{PLH}	propagation delay \overline{LE} to Q_n		74 27 22	270 54 46		330 68 58		405 81 69	ns	2.0 4.5 6.0	Fig.9
t_{PHL}/t_{PLH}	propagation delay \overline{BI} to Q_n		61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig.10
t_{PHL}/t_{PLH}	propagation delay \overline{LT} to Q_n		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8, 9 and 10
t_W	latch enable pulse width LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.9
t_{su}	set-up time D_n to LE	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.11
t_h	hold time D_n to \overline{LE}	0 0 0	-11 -4 -3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.11

BCD to 7-segment latch/decoder/driver

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard, excepting V_{OH} which is given below
 I_{CC} category: MSI

Non-standard DC characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	V_I	$-I_o$ (mA)
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{OH}	HIGH level output voltage	3.98 3.60			3.84 3.35		3.70 3.10		V	4.5	V_{IH} or V_{IL}	7.5 10.0

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
 To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
\overline{LT} , \overline{LE}	1.50
\overline{BI} , D_n	0.30

BCD to 7-segment latch/decoder/driver

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AC CHARACTERISTICS FOR 74HCT

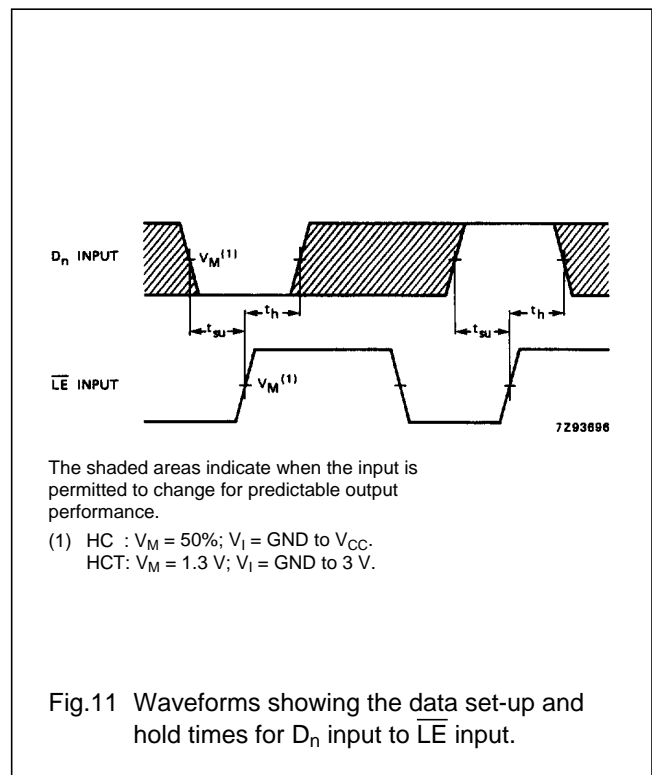
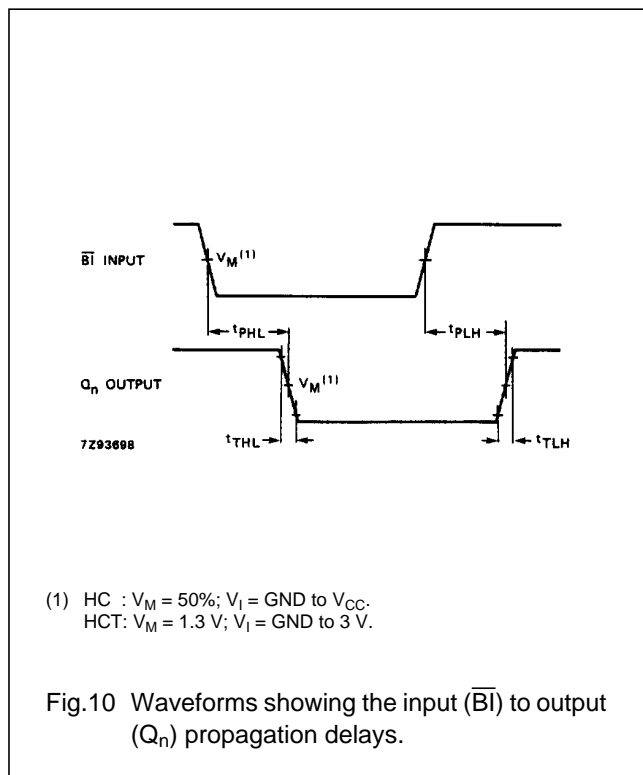
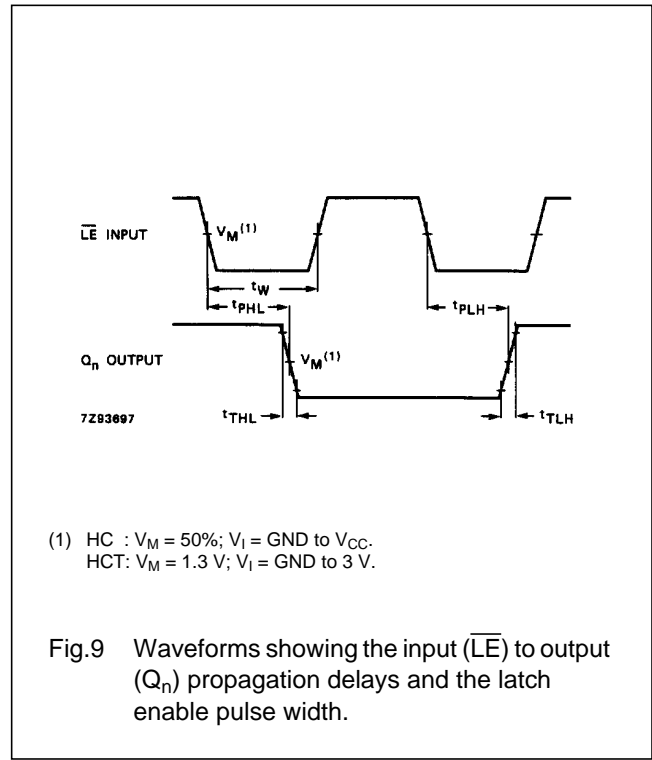
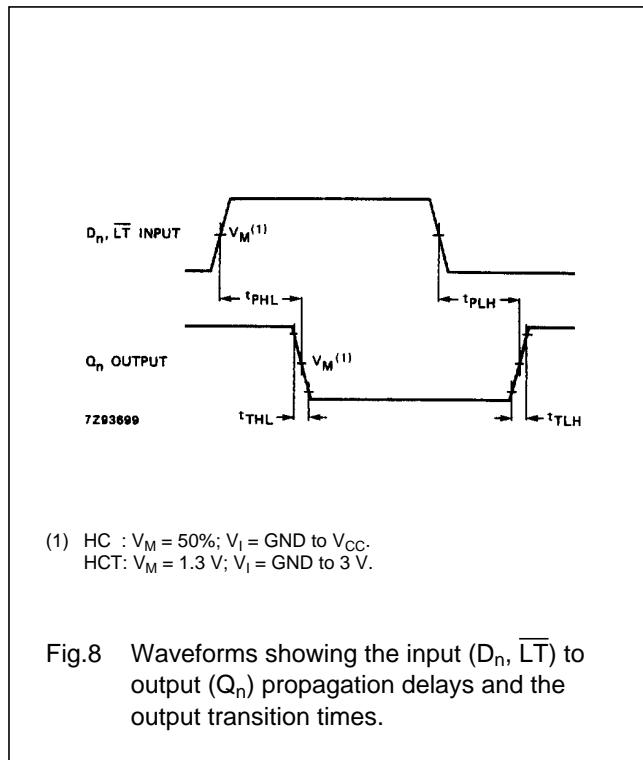
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		28	60		75		90	ns	4.5	Fig.8
t_{PHL}/t_{PLH}	propagation delay \overline{LE} to Q_n		27	54		68		81	ns	4.5	Fig.9
t_{PHL}/t_{PLH}	propagation delay \overline{BI} to Q_n		23	44		55		66	ns	4.5	Fig.10
t_{PHL}/t_{PLH}	propagation delay \overline{LT} to Q_n		16	30		38		45	ns	4.5	Fig.8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 8, 9 and 10
t_W	latch enable pulse width LOW	16	5		20		24		ns	4.5	Fig.9
t_{su}	set-up time D_n to \overline{LE}	12	5		15		18		ns	4.5	Fig.11
t_h	hold time D_n to \overline{LE}	0	-4		0		0		ns	4.5	Fig.11

BCD to 7-segment latch/decoder/driver

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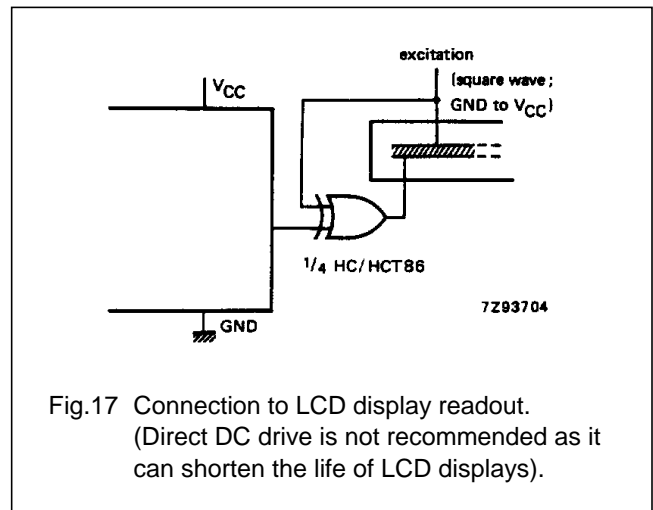
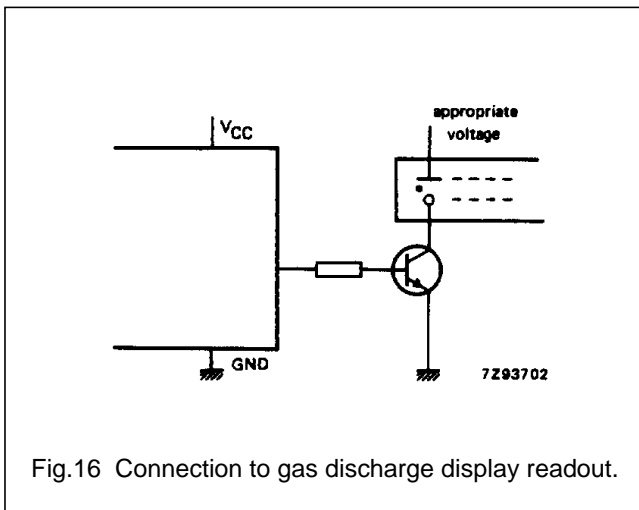
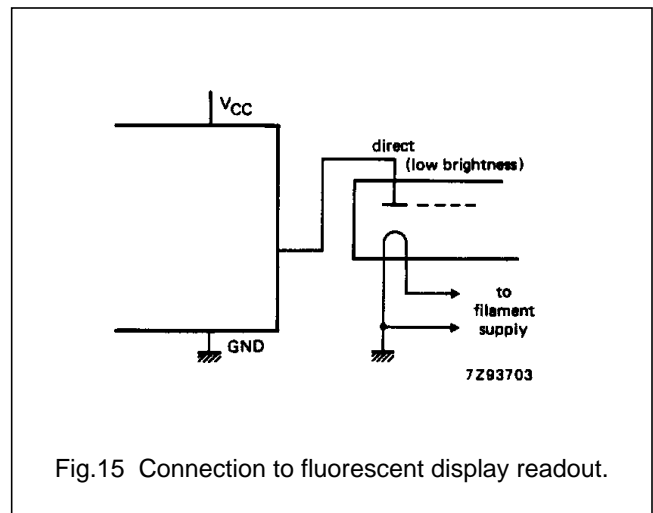
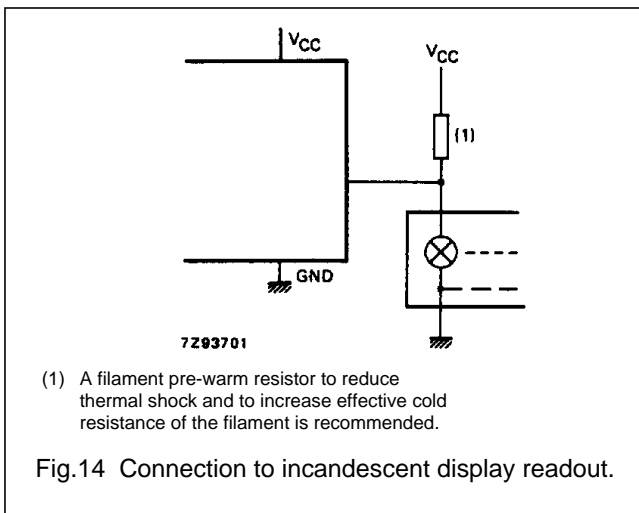
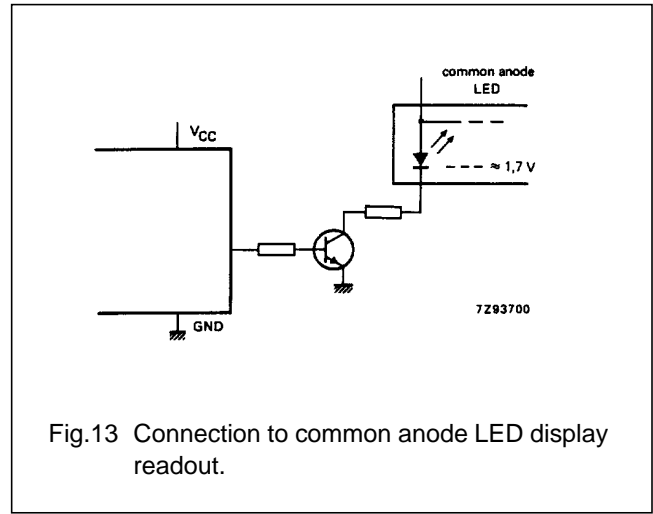
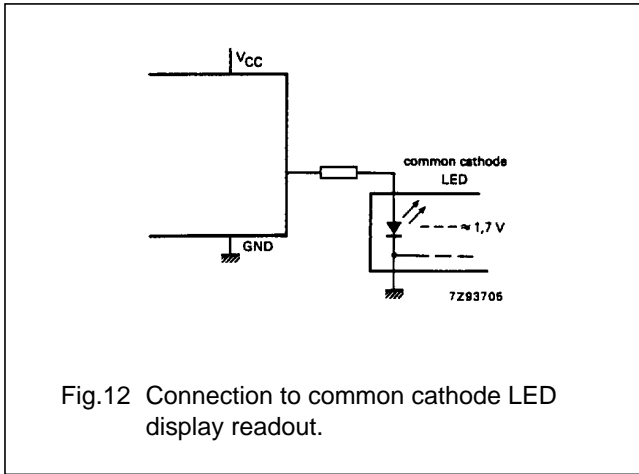
AC WAVEFORMS



BCD to 7-segment latch/decoder/driver

74HC/HCT4511

APPLICATION DIAGRAMS



BCD to 7-segment latch/decoder/driver

74HC/HCT4511

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

74HC/HCT4511; BCD to 7-segment latch/decoder/driver

Information as of 2003-04-22

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Models

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General description

The 74HC/HCT4511 are high-speed Si-gate CMOS devices and are pin compatible with '4511' of the '4000B' series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4511 are BCD to 7-segment latch/decoder/drivers with four address inputs (D_1 to D_4), an active LOW latch enable input (LE), an active LOW ripple blanking input (BI), an active LOW lamp test input (LT), and seven active HIGH segment outputs (Q_a to Q_g).

When LE is LOW, the state of the segment outputs (Q_a to Q_g) is determined by the data on D_1 to D_4 .

When LE goes HIGH, the last data present on D_1 to D_4 are stored in the latches and the segment outputs remain stable.

When LT is LOW, all the segment outputs are HIGH independent of all other input conditions. With LT HIGH, a LOW on BI forces all segment outputs LOW. The inputs LT and BI do not affect the latch circuit.


Features

- Latch storage of BCD inputs
- Blanking input
- Lamp test input
- Driving common cathode LED displays
- Guaranteed 10 mA drive capability per output
- Output capability: non-standard
- I_{CC} category: MSI

Applications




- Driving LED displays
- Driving incandescent displays
- Driving fluorescent displays
- Driving LCD displays
- Driving gas discharge displays

□ Datasheet

<u>Type number</u>	<u>Title</u>	<u>Publication release date</u>	<u>Datasheet status</u>	<u>Page count</u>	<u>File size (kB)</u>	<u>Datasheet</u>
74HC/HCT4511	BCD to 7-segment latch/decoder/driver	12/1/1990	Product specification	12	76	 Download

Additional datasheet info

To complete the device datasheet with package and family information, also download the following PDF files. The "Logic Package Information" document is required to determine in which package(s) this device is available.

<u>Document</u>	<u>Description</u>
1  HCT_FAMILY_SPECIFICATIONS	HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications
2  HCT_PACKAGE_INFO	HC/T Package Info, The IC06 74HC/HCT/HCMOS Logic Package Information
3  HCT_PACKAGE_OUTLINES	HC/T Package Outlines, The IC06 74HC/HCT/HCMOS Logic Package Outlines

□ Parametrics

<u>Type number</u>	<u>Package Description</u>	<u>Propagation Delay(ns)</u>	<u>Voltage</u>	<u>No. of Pins</u>	<u>Power Dissipation Considerations</u>	<u>Logic Switching Levels</u>	<u>Output Drive Capability</u>
74HC4511D	SOT109 (SO16) BCD to 7-Segment Latch/Decoder/Driver with Lamp Test Input	15	5 Volts +	16	Low Power or Battery Applications	CMOS	Low
74HC4511N	SOT38-1 (DIP16) BCD to 7-Segment Latch/Decoder/Driver with Lamp Test Input	15	5 Volts +	16	Low Power or Battery Applications	CMOS	Low
74HCT4511D	SOT109 (SO16) BCD to 7-Segment Latch/Decoder/Driver with Lamp Test Input; TTL Enabled	15	5 Volts +	16	Low Power or Battery Applications	TTL	Low
74HCT4511N	SOT38-1 (DIP16) BCD to 7-Segment Latch/Decoder/Driver with Lamp Test Input; TTL Enabled	15	5 Volts +	16	Low Power or Battery Applications	TTL	Low

□ Products, packages, availability and ordering

<u>Type number</u>	<u>North American type number</u>	<u>Ordering code (12NC)</u>	<u>Marking/Packing</u> Discretes packing info	<u>Package</u>	<u>Device status</u>	<u>Buy online</u>
74HC4511D	74HC4511D	9337 148 80652	Standard Marking * Bulk Pack, CECC	SOT109 (SO16)	Full production	order this <input type="checkbox"/>
	74HC4511D-T	9337 148 80653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT109 (SO16)	Full production	order this <input type="checkbox"/>
74HC4511N	74HC4511N	9336 698 10652	Standard Marking * Bulk Pack, CECC	SOT38-1 (DIP16)	Full production	order this <input type="checkbox"/>
74HCT4511D	74HCT4511D	9337 153 60652	Standard Marking * Bulk Pack, CECC	SOT109 (SO16)	Full production	order this <input type="checkbox"/>
	74HCT4511D-T	9337 153 60653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT109 (SO16)	Full production	order this <input type="checkbox"/>
74HCT4511N	74HCT4511N	9336 704 40652	Standard Marking * Bulk Pack, CECC	SOT38-1 (DIP16)	Full production	order this <input type="checkbox"/>

□ Similar products

[74HC/HCT4511](#) links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

□ Support & tools

[HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications](#)(date 01-Mar-98)

[HC/T User Guide](#)(date 01-Nov-97)

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