32Mx16
Mobile SDRAM
54CSP 1/CS

(VDD/VDDQ 3.0V/3.0V or 3.3V/3.3V)

Revision 1.2

December 2002

8M x 16Bit x 4 Banks Mobile SDRAM

FEATURES

- 3.0V power supply
- LVCMOS compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (1 & 2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (8K cycle)
- 1 /CS Support.
- Commercial Temperature Operation (-25°C ~ 70°C).
  Extended Temperature Operation (-25°C ~ 85°C).
  Industrial Temperature Operation (-40°C ~ 85°C).
- 54balls DDP CSP

GENERAL DESCRIPTION

The K4S511633C is 536,870,912 bits synchronous high data rate Dynamic RAM organized as 4 x 8,388,608 words by 16bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

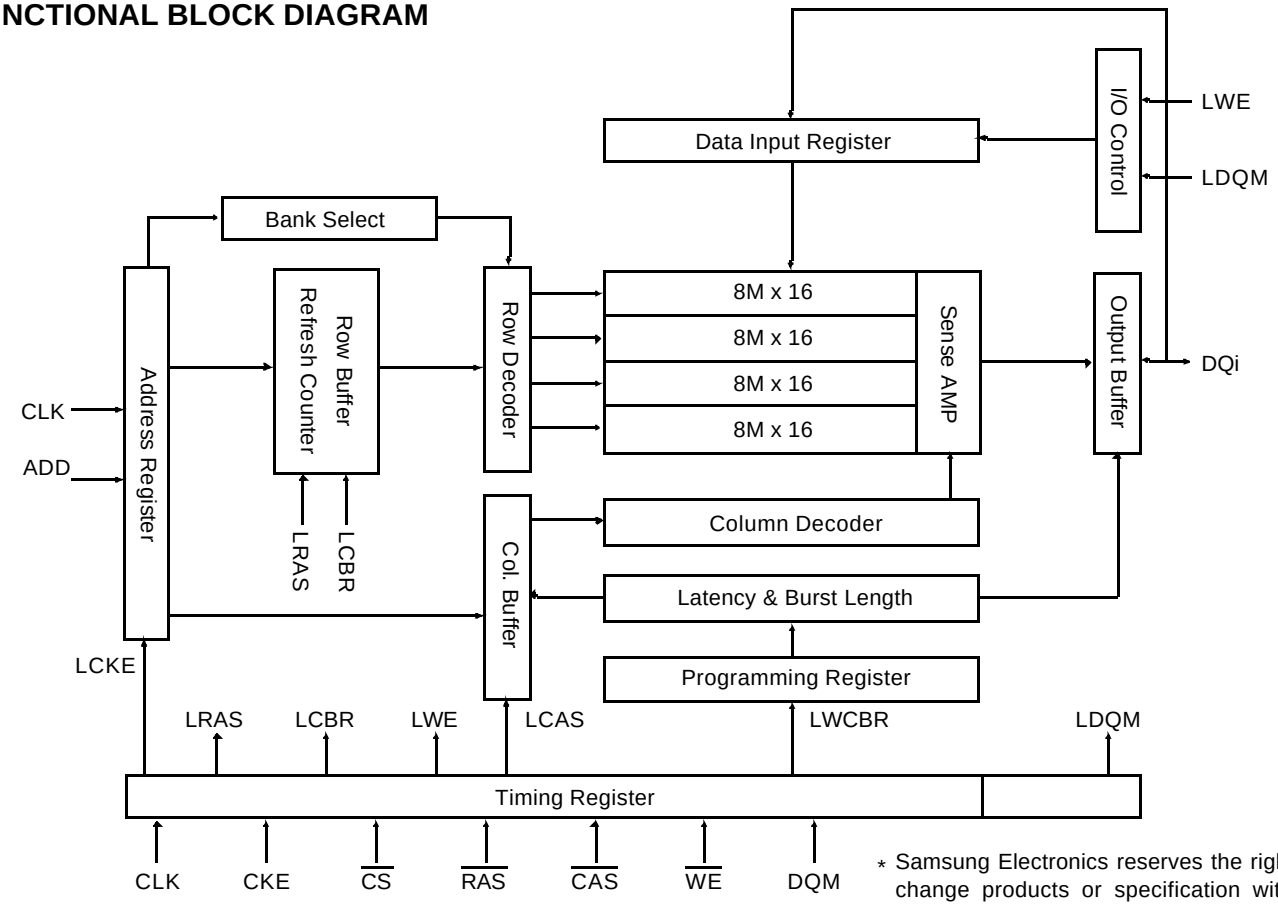
Part No.	Max Freq.	Interface	Package
K4S511633C-YL/N80	125MHz(CL=3) 100MHz(CL=2)	LVCMOS	54 CSP
K4S511633C-YL/N1H	100MHz(CL=2)		
K4S511633C-YL/N1L	100MHz(CL=3)*1		

- YN : Low Power, Operating Temp : -25°C ~ 85°C.
- YL : Low Power, Operating Temp : -25°C ~ 70°C.
- YP : Low Power, Operating Temp : -40°C ~ 85°C.

Note :

1. In case of 33MHz Frequency, CL1 can be supported.

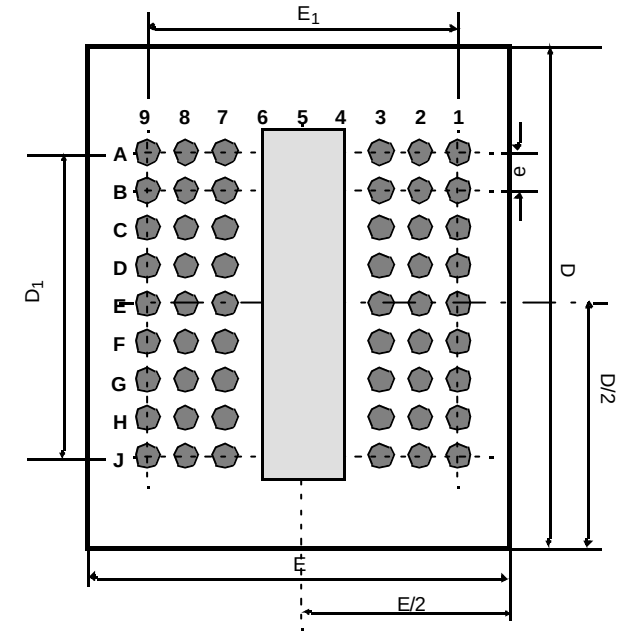
FUNCTIONAL BLOCK DIAGRAM



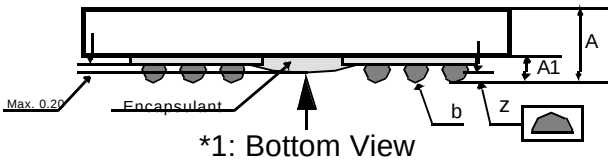
* Samsung Electronics reserves the right to change products or specification without notice.

Package Dimension and Pin Configuration

< Bottom View*1 >

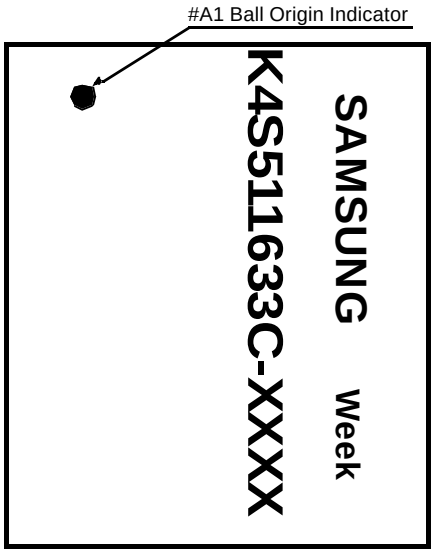


*2: Top View



*1: Bottom View

< Top View*2 >



< Top View*2 >

54Ball(6x9) CSP						
	1	2	3	7	8	9
A	VSS	DQ15	VSSQ	VDDQ	DQ0	VDD
B	DQ14	DQ13	VDDQ	VSSQ	DQ2	DQ1
C	DQ12	DQ11	VSSQ	VDDQ	DQ4	DQ3
D	DQ10	DQ9	VDDQ	VSSQ	DQ6	DQ5
E	DQ8	NC	VSS	VDD	LDQM	DQ7
F	UDQM	CLK	CKE	$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
G	A12	A11	A9	BA0	BA1	$\overline{CS}$
H	A8	A7	A6	A0	A1	A10
J	VSS	A5	A4	A3	A2	VDD

Pin Name	Pin Function
CLK	*System Clock*
$\overline{CS}$	*Chip Select*
CKE	*Clock Enable*
A_0 ~ A_{12}	*Address*
BA_0 ~ BA_1	*Bank Select Address*
$\overline{RAS}$	*Row Address Strobe*
$\overline{CAS}$	*Column Address Strobe*
$\overline{WE}$	*Write Enable*
L(U)DQM	*Data Input/Output Mask*
DQ_0 ~ $_{15}$	*Data Input/Output*
VDD/VSS	*Power Supply/Ground*
VDDQ/VSSQ	*Data Output Power/Ground*

[Unit:mm]

Symbol	Min	Typ	Max
A	1.00	1.10	1.30
A_1	0.27	0.32	0.37
E	-	9.50	-
E_1	-	6.40	-
D	-	15.50	-
D_1	-	6.40	-
e	-	0.80	-
b	0.40	0.45	0.50
z	-	-	0.10

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Notes :
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A =Commercial, Extended and Industrial)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	2.7	3.0	3.6	V	
	V_{DDQ}	2.7	3.0	3.6	V	
Input logic high voltage	V_{IH}	2.2	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.5	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes :
1. V_{IH} (max) = 5.3V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
   Input leakage currents include HI-Z output leakage for all bi-directional buffers with tri-state outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.0V, T_A = 23°C, f = 1MHz, V_{REF} =0.9V ± 50 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	3.0	9.0	pF	
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE	C_{IN}	3.0	9.0	pF	
DQM	C_{IN}	1.5	4.5	pF	
Address	C_{ADD}	3.0	9.0	pF	
DQ_0 ~ DQ_{15}	C_{OUT}	3.0	6.5	pF	

DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A =Commercial, Extended and Industrial)

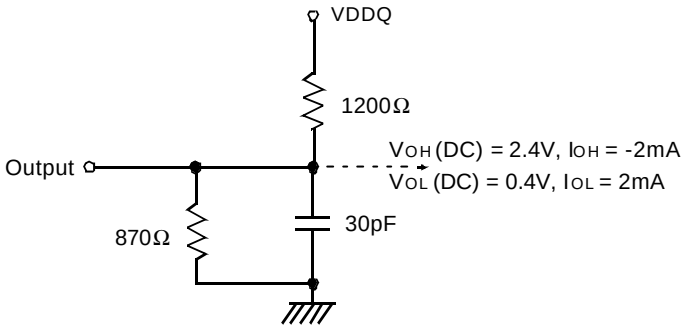
Parameter	Symbol	Test Condition		Version			Unit	Note
				-80	-1H	-1L		
Operating Current (One Bank Active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		160	155	145	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		2			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		2				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		35			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		25				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		15			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		15				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		50			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		45			mA	
Operating Current (Burst Mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs		230	210	210	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		350	335	305	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	-YL	1800			uA	3
			-YN					4
			-YP					5

Notes :

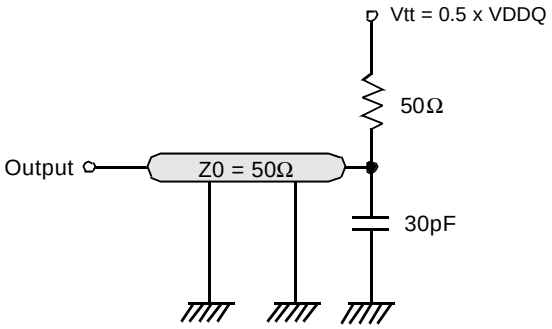
1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S511633C-YL**
4. K4S511633C-YN**
5. K4S511633C-YP**
6. Unless otherwise noted, input swing level is CMOS(V_{IH} /V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS (V_{DD} = 2.7V ~ 3.6V, T_A = Commercial, Extended and Industrial)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	0.5 x VDDQ	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	0.5 x VDDQ	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			- 80	-1H	-1L		
Row active to row active delay		t_{RRD}(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}(min)	20	20	24	ns	1
Row precharge time		t_{RP}(min)	20	20	24	ns	1
Row active time		t_{RAS}(min)	48	50	60	ns	1
		t_{RAS}(max)	100			us	
Row cycle time		t_{RC}(min)	68	70	84	ns	1
Last data in to row precharge		t_{RDL}(min)	2			CLK	2,3
Last data in to Active delay		t_{DAL}(min)	tRDL + tRP			-	3
Last data in to new col. address delay		t_{CDL}(min)	1			CLK	2
Last data in to burst stop		t_{BDL}(min)	1			CLK	2
Col. address to col. address delay		t_{CCD}(min)	1			CLK	4
Number of valid output data	CAS latency=3		2			ea	5
	CAS latency=2		1				
	CAS latency=1		-		0		

Notes :

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. Minimum tRDL=2CLK and tDAL(=tRDL + tRP) is required to complete both of last data wite command(tRDL) and precharge command(tRP). tRDL=1CLK can be supported only in the case under 100MHz with manual precharge mode.
4. All parts allow every cycle column address change.
5. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		12			
	CAS latency=1		-		-		25			
CLK to valid output delay	CAS latency=3	tSAC		6		7		7	ns	1,2
	CAS latency=2			7		7		8		
	CAS latency=1			-		-		20		
Output data hold time	CAS latency=3	tOH	2.5		2.5		2.5		ns	2
	CAS latency=2		2.5		2.5		2.5			
	CAS latency=1		-		-		2.5			
CLK high pulse width		tCH	2.5		3		3		ns	3
CLK low pulse width		tCL	2.5		3		3		ns	3
Input setup time		tSS	2.0		2.5		2.5		ns	3
Input hold time		tSH	1.0		1.5		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		7	ns	
	CAS latency=2			7		7		8		
	CAS latency=1			-		-		20		

Notes :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

Notes :

1. This is to advise Samsung customers that, in accordance with certain terms of an agreement, Samsung is prohibited from selling any DRAM products configured in "Multi-Die Plastic" format for use as components in general and scientific computers, such as mainframes, servers, work stations or desk top personal computers (hereinafter "Prohibited Computer Use"). Applications such as mobile, including cell phones, telecom, including televisions and display monitors, or non-desktop computer systems, including laptops, notebook computers, are, however, permissible. "Multi-Die Plastic" is defined as two or more DRAM die encapsulated within a single plastic leaded package.

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SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_{12}, $A_9 \sim A_0$	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address ($A_0 \sim A_9$)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address ($A_0 \sim A_9$)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Notes :

1. OP Code : Operand Code
   $A_0 \sim A_{12}$ & $BA_0 \sim BA_1$: Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are the same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation it makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).