128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15,17,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40 mA(Max.)
    (CMOS): 10 mA(Max.)
  - Operating KM681002J-15 : 170 mA (Max.)
    KM681002J-17 : 160 mA (Max.)
    KM681002J-20 : 150 mA (Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Tolerance & Compatible with 3.3V Device
- Fully Static Operation
  - -No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM681002J : 32-SOJ-400
  - KM681002T : 32-TSOP2-400F

GENERAL DESCRIPTION

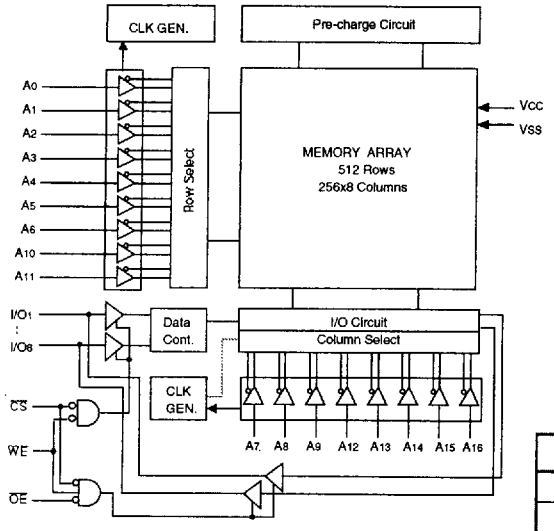
The KM681002 is a 1,048,576-bit high-speed static random access memory organized as 131,072 words by 8 bits.

The KM681002 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

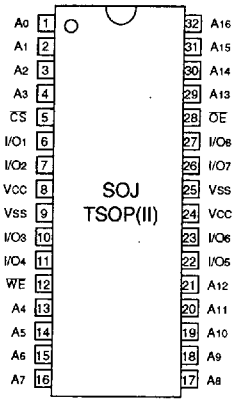
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM681002 is packaged in a 400 mil 32-pin plastic SOJ and TSOP(II) forward.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



Pin Name	Pin Function
A0-A16	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1~I/O8	Data Inputs / Outputs
Vcc	Power (+5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5	V
Input Low Voltage	V_{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -3.0V for ≤ 10 ns Pulse.

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-2	2	µA
Average Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0 mA	15 ns	-	170	mA
			17 ns	-	160	
			20 ns	-	150	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle		-	40	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 MHz V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100µA			3.95	V

*Note : Vcc=5V± 5%, Temp. =25°C

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

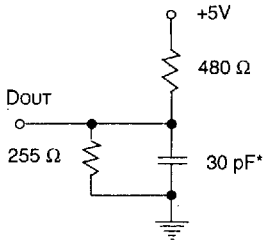
AC CHARACTERISTICS

TEST CONDITIONS

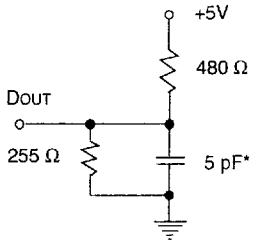
(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681002J-15		KM681002J-17		KM681002J-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	15	-	17	-	20	ns
Output Enable to Valid Output	t_{OE}	-	8	-	9	-	10	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	4	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t_{PD}	-	15	-	17	-	20	ns

WRITE CYCLE

Parameter	Symbol	KM681002J-15		KM681002J-17		KM681002J-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	12	-	13	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	9	-	10	-	11	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

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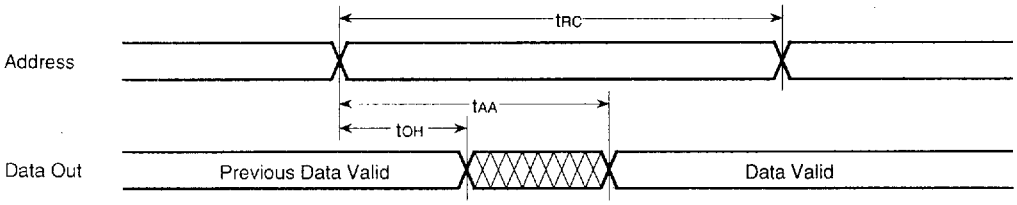
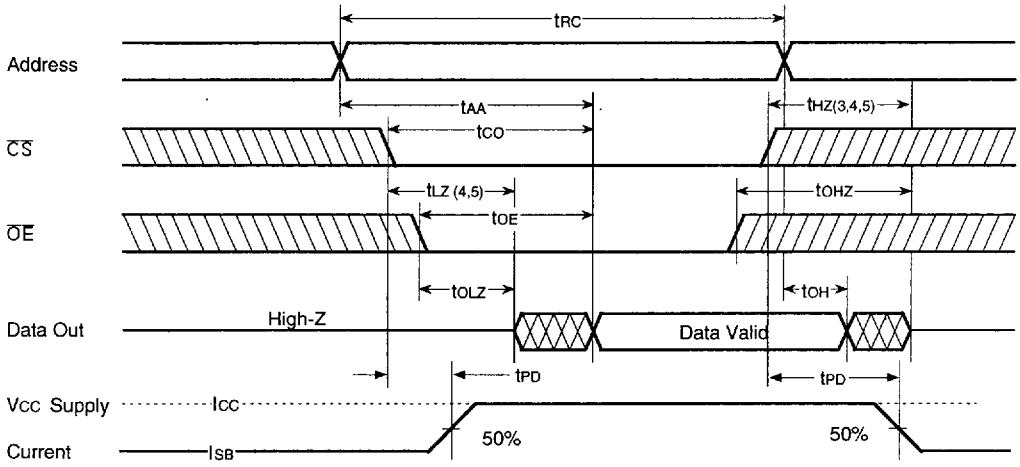
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



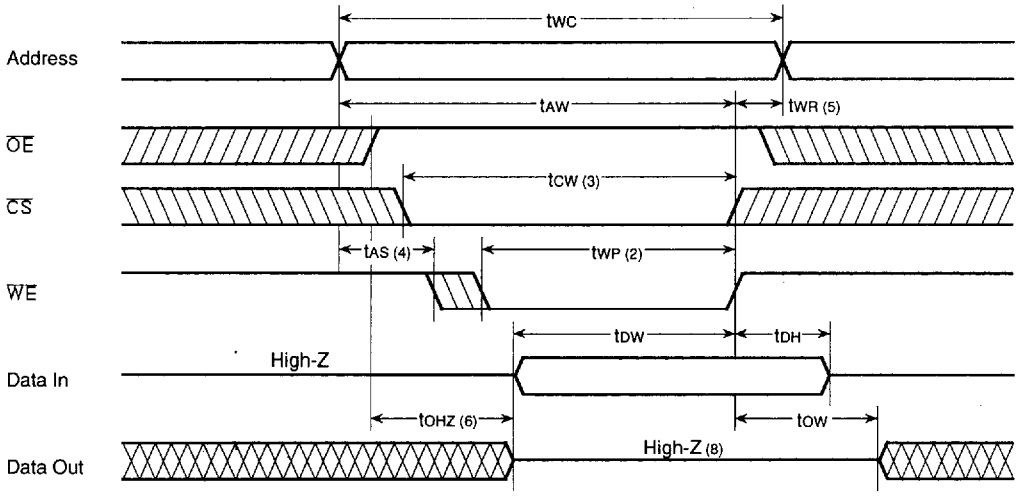
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



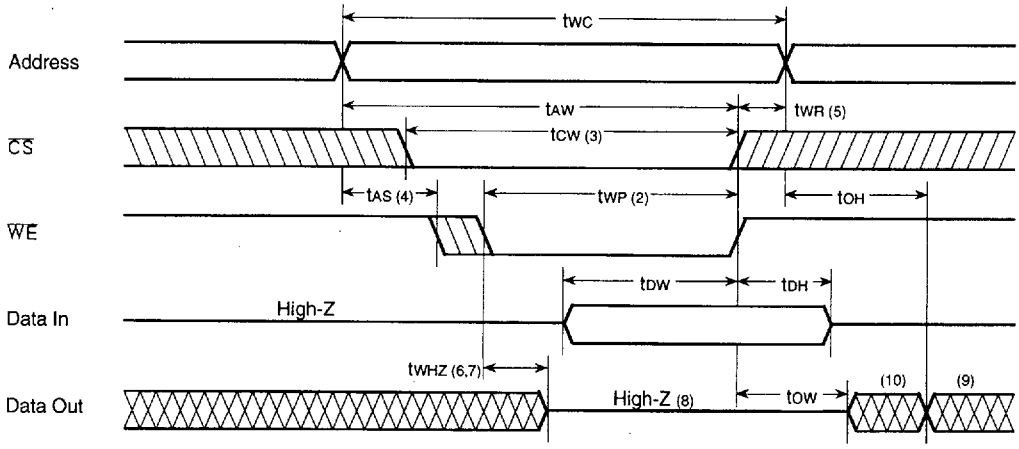
NOTES (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$,$\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.