32K x 32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Single 3.3V-5%/+10% Power Supply.
- 5V Tolerant Inputs except I/O Pins
- Byte Write Enable Control
- Global Write Enable Controls a full bus-width write
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable,1 cycle Disable
- Asynchronous Output Enable Control.
- $\overline{ADSP}$,$\overline{ADSC}$,$\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Outputs.
- 100-Pin QFP /TQFP Package.

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	-17	Unit
Cycle Time	tCYC	75	66	60	MHz
Clock Access Time	tCD	7	8	9	ns
Output Enable Access Time	tOE	6	7	8	ns

GENERAL DESCRIPTION

The KM732V589/L is a 1,048,576-bit Synchronous Static Random Access Memory designed for high performance Second level Cache of i486/Pentium and /Power PC based System.

It is organized as 32,768 words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high perform -ance cache RAM applications; $\overline{GW}$,$\overline{BW}$,$\overline{LBO}$, ZZ.

Write cycles are internally self-timed and synchronous. Full bus-width write is done by $\overline{GW}$,and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is High.

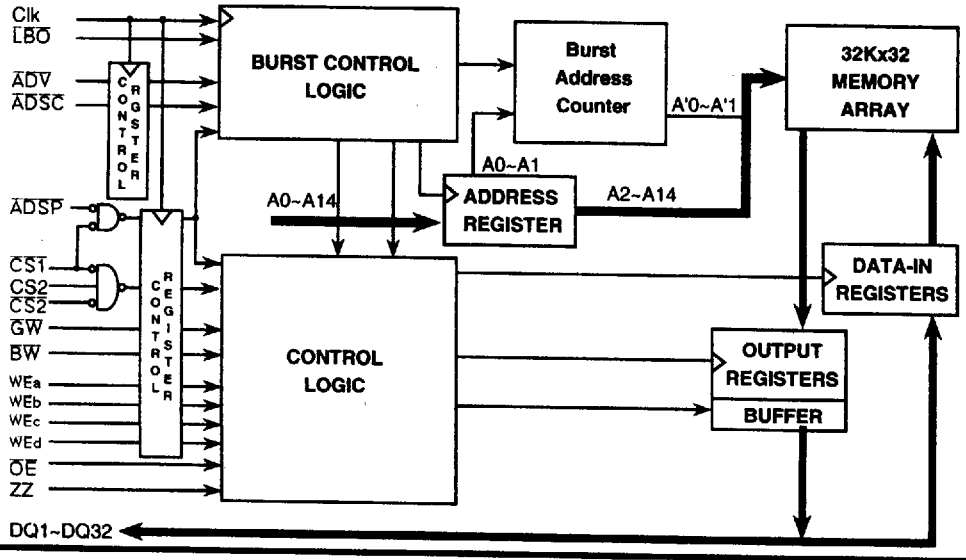
When $\overline{CS1}$ is high, $\overline{ADSP}$ is blocked to control signals. Bursts can be initiate with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

$\overline{LBO}$ Pin is DC operated and determines burst sequence (linear or Interleaved).

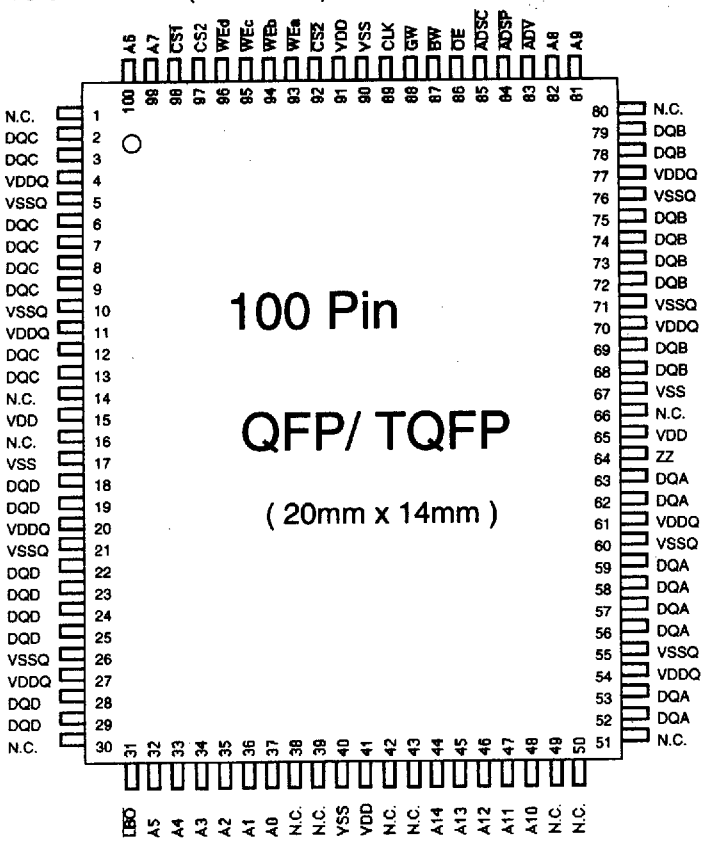
ZZ Pin controls Power Down State and reduces Stand by current regardless of CLK.

The KM732V589/L is fabricated using Samsung's high performance CMOS technology and is available in 100 pin QFP / TQFP package. Multiple power and ground pins are utilized to minimize ground bounce

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	PIN NO.	SYMBOL	PIN NAME	PIN NO.
A0-A14	Address Inputs	32, 33, 34, 35, 36	VDD	Power Supply (+3.3V)	15, 41, 65, 91
		37, 44, 45, 46, 47	VSS	Ground	17, 40, 67, 90
		48, 81, 82, 99, 100	NC	No Connect	1, 14, 16, 30, 38,39,
$\overline{ADV}$	Burst Address Advance	83			42, 43, 49 ,50, 51,
$\overline{ADSP}$	Address Status Processor	84			66, 80
$\overline{ADSC}$	Address Status Controller	85	DQ1~	Data Inputs/Outputs	2, 3, 6, 7, 8, 9, 12
CLK	Clock	89	DQ32		13, 18, 19, 22, 23
$\overline{CS1}$	Chip Select	98			24, 25, 28, 29, 52
CS2	Chip Select	97			53, 56, 57, 58, 59
$\overline{CS2}$	Chip Select	92			62, 63, 68, 69, 72
$\overline{WEx}$	Byte Write Enable	93, 94, 95, 96			73, 74, 75, 78, 79
$\overline{OE}$	Output Enable	86	VDDQ	Output Power Supply	4, 11, 20, 27, 54, 61
$\overline{GW}$	Global Write Enable	88		(+3.3V)	70, 77
$\overline{BW}$	Byte Write Enable	87	VSSQ	Output Ground	5, 10, 21, 26, 55,60
ZZ	Power Down Input	64			71, 76
$\overline{LBO}$	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM732V589/L is a synchronous SRAM designed to support the burst address accessing sequence of the i486/Pentium and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$ / ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$. The accesses are enabled with the chip select signals and output enable signals. Wait states are inserted into the access with $\overline{ADV}$.

During normal operation, ZZ must be pulled LOW. When ZZ is pulled HIGH, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to LOW, the SRAM normally operates after 2 cycles of wake up time.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of Clk, are carried to the Data-out buffer by the next positive edge of Clk. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled HIGH and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$ (regardless of $\overline{BW}$ and $\overline{WE}$x.) ,and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x. when $\overline{GW}$ is High.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled low. The address increases internally to the next address of burst if both $\overline{WE}$x and $\overline{ADV}$ are sampled low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. $\overline{WE}$a controls DQ1~DQ8, $\overline{WE}$b, controls DQ9~DQ16, $\overline{WE}$c controls DQ17~DQ24 and $\overline{WE}$d controls DQ25~DQ32. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$x are sampled on the same clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High , Interleaved burst sequence is selected

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ pin	High	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Lenear Burst)

$\overline{LBO}$ pin	Low	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE :
1. $\overline{LBO}$ pin must be tied to High or Low , and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	K	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE :

1. X means "Don't Care"
2. The rising edge of clock is symbolized by ↑
3. $\overline{WRITE}$ =L means Write operation in WRITE TRUTH TABLE
   $\overline{WRITE}$ =H means Read operation in WRITE TRUTH TABLE
4. Operation finally depends on status of asynchronous input pins (ZZ and $\overline{OE}$)

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE :

1. X means "Don't Care"
2. All inputs in this table must meet setup and hold time around the rising edge of CLK (↑)

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din,High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care"
2. N.C state is Not Allowed.
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WRITE}$	Operation	$\overline{CS1}$	$\overline{WRITE}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An, Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Dn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE

1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.
2. $\overline{CS2}$ =Low and CS2=High .(Not Deselected)
3. $\overline{ADSC}$ =High when $\overline{CS1}$=High (Not Deselected)
4. $\overline{WRITE}$ = Low means that one or more byte write enable inputs ($\overline{WE}$a, $\overline{WE}$b,$\overline{WE}$c,$\overline{WE}$d) and $\overline{BW}$ are Low or $\overline{GW}$ is High.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to +85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

DC ELECTRICAL CHARACTERISTICS (V_{DD}=3.3V-5%/+10%, TA=0°C to +70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iil	V_{IN}=Vss to V_{DD}		-2	+2	μA
Output Leakage Current	Iol	Output Disabled, V_{OUT}=Vss to V_{DD}		-2	+2	μA
Operating Current	Icc	I_{OUT}=0mA , ZZ < VIL	75MHz	-	200	mA
		All Inputs = VIH or VIL	66MHz	-	180	
		Cycle Time ≥ tCYC min	60MHz	-	160	
Standby Current	Isb	Device deselected, I_{OUT}=0mA, ZZ ≤ VIL All Inputs = VIH or VIL, Cycle Time ≥ tCYC min		-	30	mA
	Isb1	Device deselected, ZZ ≤ VIL		-	5	mA
		All Inputs= Fixed(V_{DD}-0.2 or 0.2V)				
		Cycle Time =0 MHz	L-Ver.	-	1	mA
	Isb2	ZZ≥V_{DD}-0.2V		-	5	mA
		All Inputs= V_{DD}-0.2 or 0.2V				
		Cycle Time ≥ tCYC min	L-Ver.	-	200	uA
Output Low Voltage	Vol	Iol=8.0mA		-	0.4	V
Output High Voltage	Voh	Ioh=-4.0mA		2.4	-	V
Input Low Voltage	Vil			-0.5*	0.8	V
Input High Voltage	Vih			2.2	5.5 **	V

* Vil(min)=-3.0 (Pulse Width ≤20ns)

** In Case of I/O Pins, max. Vih is Vdd +0.5V

CAPACITANCE* (T_A=25°C, f=1Mhz)

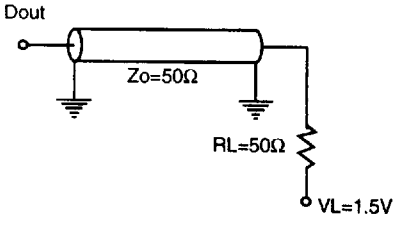
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

*NOTE : Sampled not 100% tested.

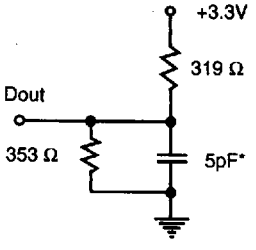
TEST CONDITIONS (T_A=0°C to 70°C, V_{DD}=3.3V-5%/+10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load (A)



Output Load (B)
(for tLZC, tLZOE, tHZOE & tHZC)



* Including Scope and Jig Capacitance

Fig. 1

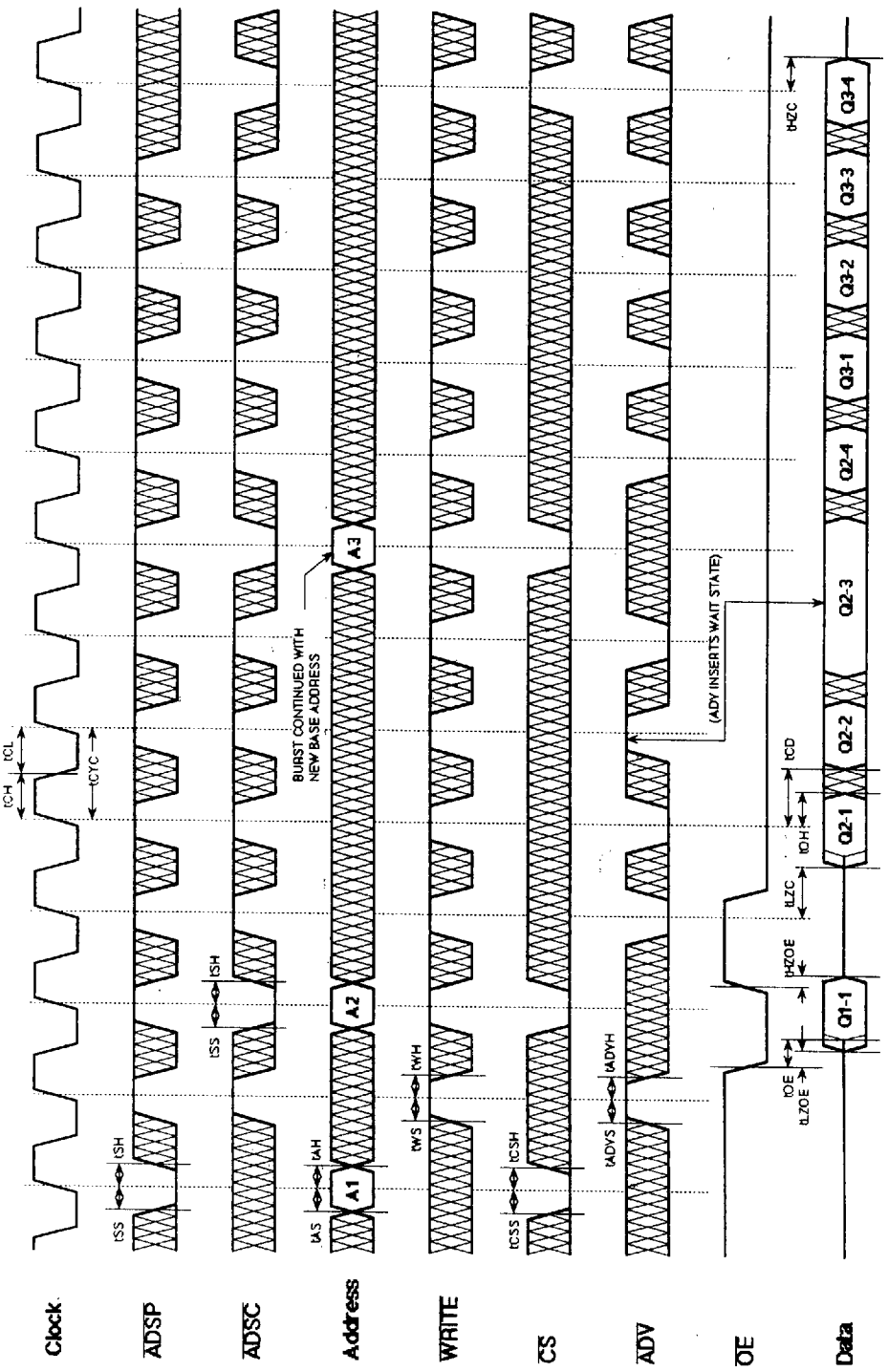
AC TIMING CHARACTERISTICS (V_{DD}=3.3V-5%/+10%, T_A=0°C to +70°C)

Parameter	Symbol	KM732V589-13		KM732V589-15		KM732V589-17		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	13		15		17		ns
Clock Access Time	tCD		7		8		9	ns
Output Enable to Data Valid	tOE		6		7		8	ns
Clock High to Output Low-Z	tLZC	6		6		6		ns
Output Hold from Clock High	tOH	2.5		2.5		2.5		ns
Output Enable Low to Output Low-Z	tLZOE	2		2		2		ns
Output Enable High to Output High-Z	tHZOE	2	5	2	6	2	6	ns
Clock High to Output High-Z	tHZC		7		7		7	ns
Clock High Pulse Width	tCH	4.5		5.5		6		ns
Clock Low Pulse Width	tCL	4.5		5.5		6		ns
Address Setup to Clock High	tAS	2.5		2.5		2.5		ns
Address Status Setup to Clock High	tSS	2.5		2.5		2.5		ns
Data Setup to Clock High	tDS	2.5		2.5		2.5		ns
Write Setup to Clock High($\overline{GW}$,$\overline{BW}$,$\overline{WE}$x)	tWS	2.5		2.5		2.5		ns
Address Advance Setup to Clock High	tADVS	2.5		2.5		2.5		ns
Chip Select Setup to Clock High	tCSS	2.5		2.5		2.5		ns
Address Hold from Clock High	tAH	0.5		0.5		0.5		ns
Address Status Hold from Clock High	tSH	0.5		0.5		0.5		ns
Data Hold from Clock High	tDH	0.5		0.5		0.5		ns
Write Hold from Clock High($\overline{GW}$,$\overline{BW}$,$\overline{WE}$x)	tWH	0.5		0.5		0.5		ns
Address Advance Hold from Clock High	tADVH	0.5		0.5		0.5		ns
Chip Select Hold from Clock High	tCSH	0.5		0.5		0.5		ns
ZZ High to Power Down	tPDS	2		2		2		cycle
ZZ Low to Power Up	tPUS	2		2		2		cycle

NOTE :

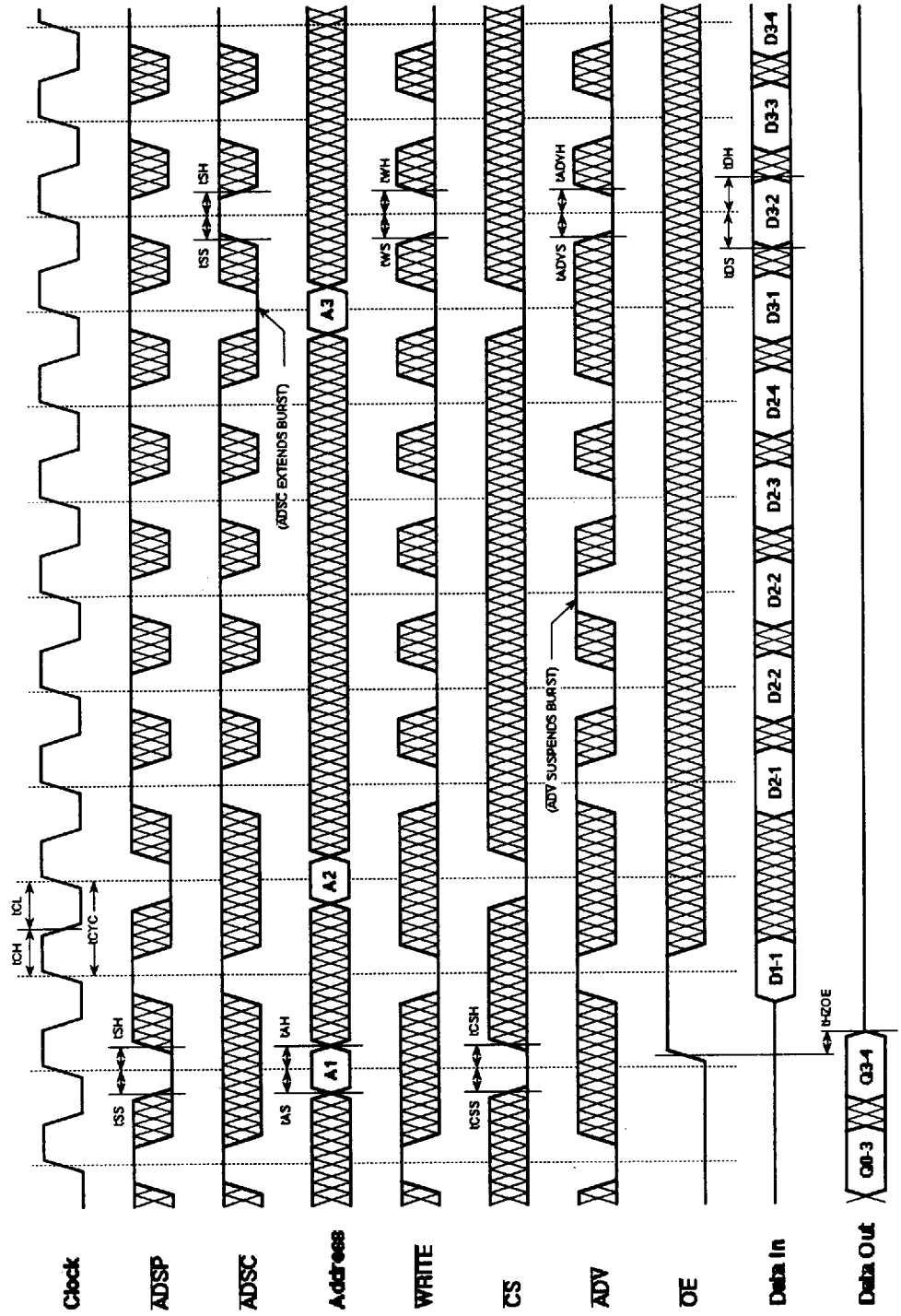
1. All address inputs must meet the specified setup and hold times for all rising clock (Clk) edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clocks after leaving ZZ state.

TIMING WAVEFORM OF READ CYCLE

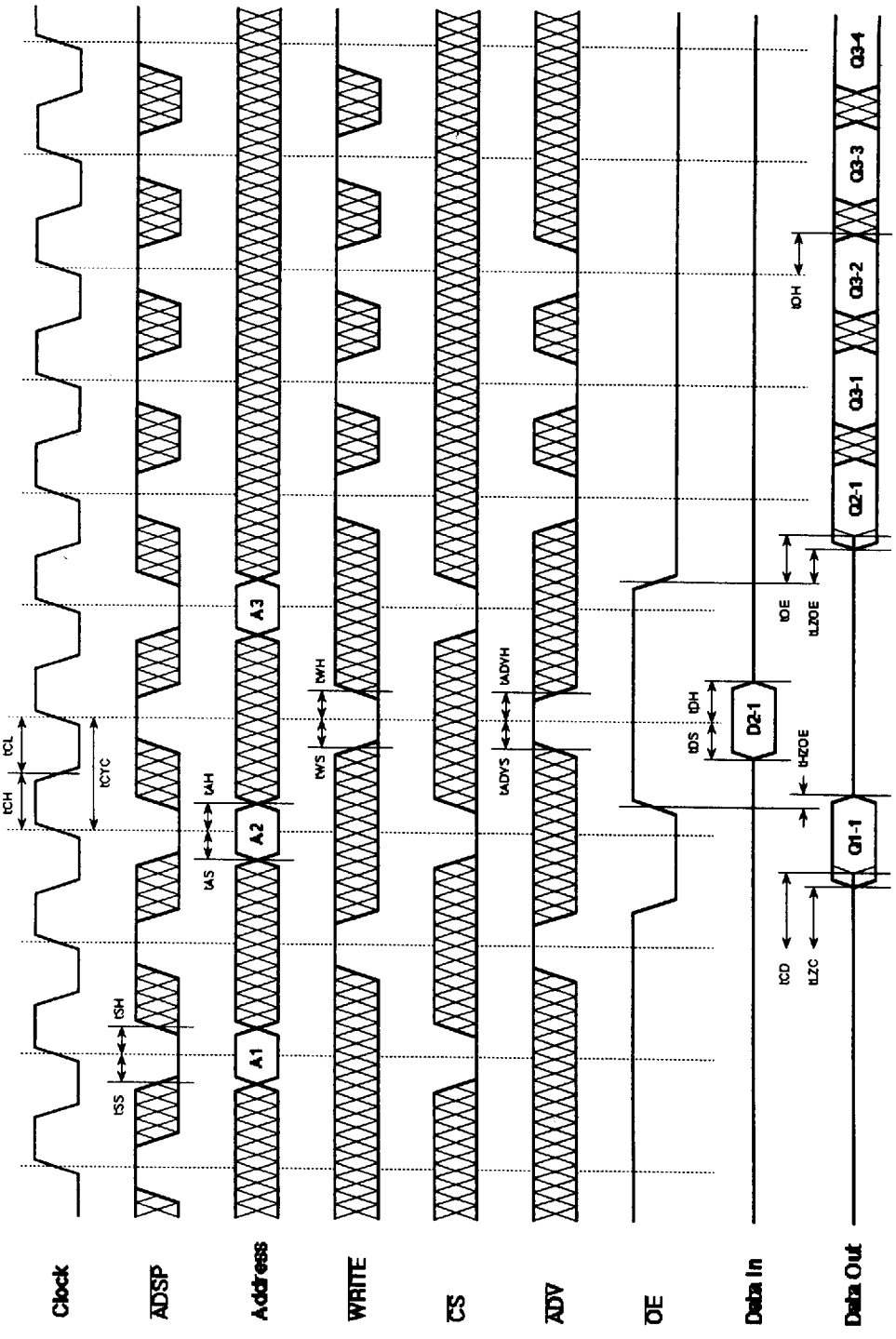


NOTE : The meaning of $\overline{CS}$=Low is $\overline{CS1}$=Low, CS2=High, and $\overline{CS2}$=Low. $\overline{CS}$=High means $\overline{CS1}$=High or CS2=Low or $\overline{CS2}$=High.

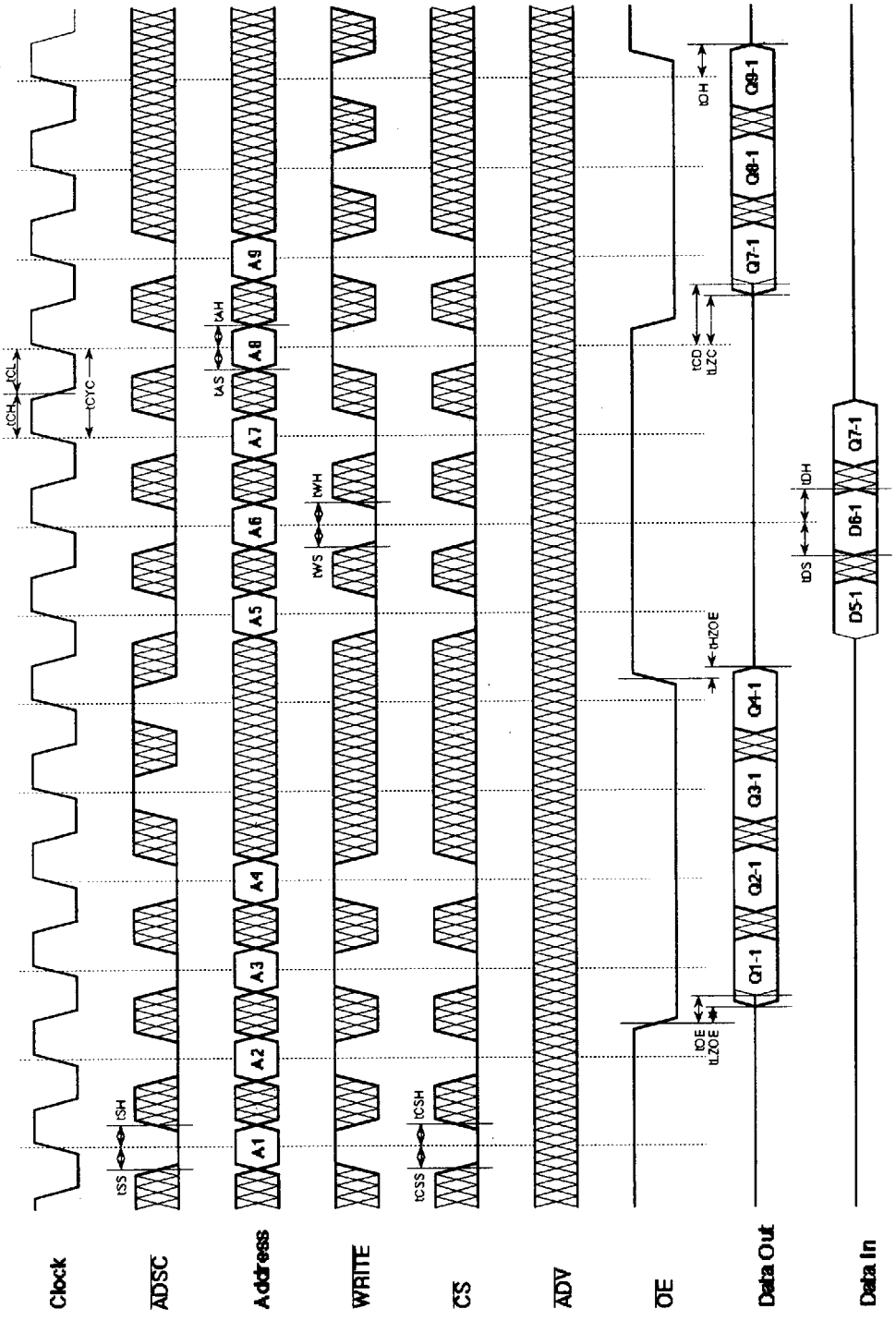
TIMING WAVEFORM OF WRITE CYCLE



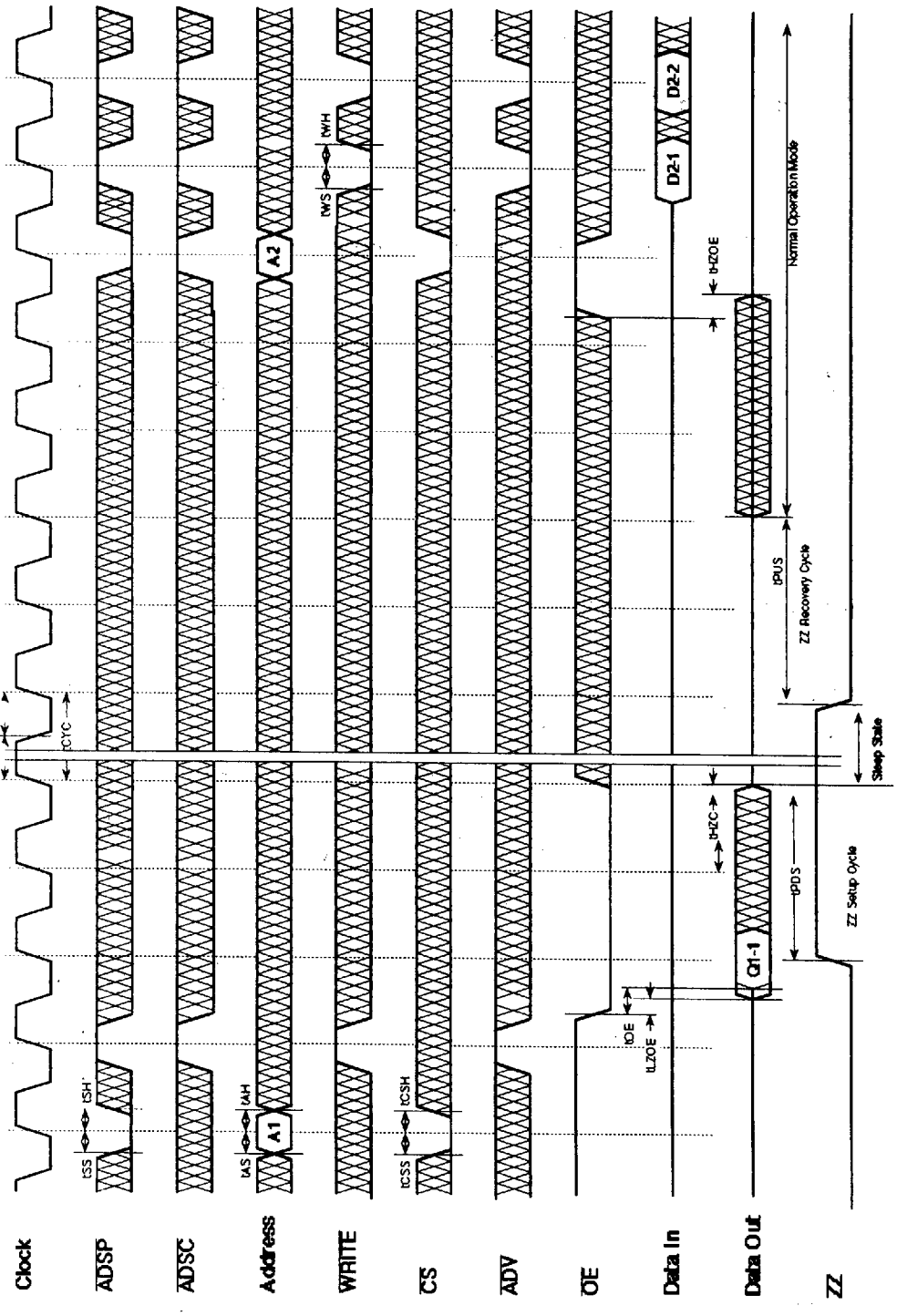
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



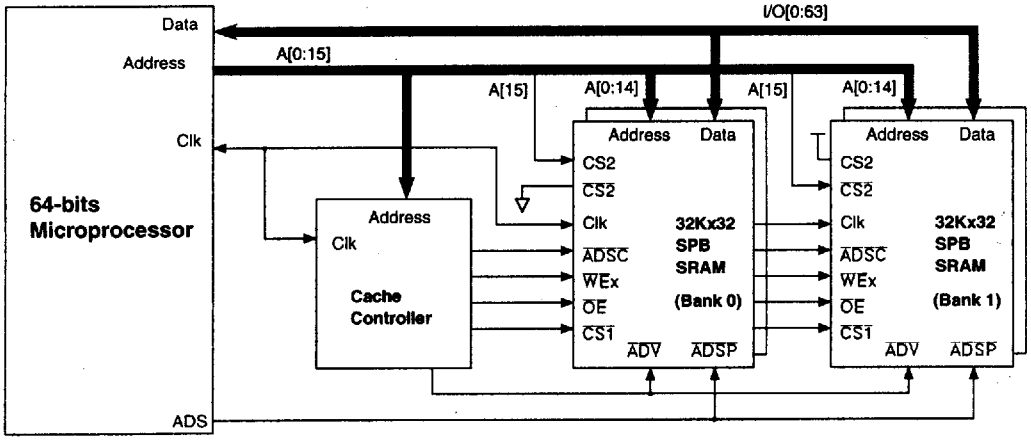
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 32Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING

(Refer to non-interleave write timing for interleave write timing) ;

2 Cycle Enable - 1 Cycle Disable Mode can reduce Data Contention in Dual Bank Operation.