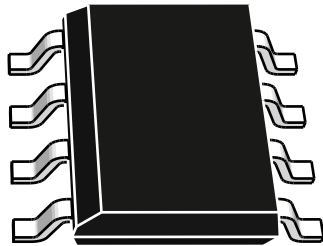
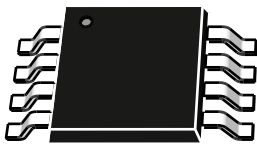


**Low-power dual operational amplifier**

Datasheet - production data

**SO8**  
(plastic micropackage)**TSSOP8**  
(thin shrink small outline package)**MiniSO8****DFN8 2 x 2 mm**  
(plastic micropackage)**Features**

- Frequency compensation implemented internally
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.1 MHz (temperature compensated)

- Very low supply current/amplifier, essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rail
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V to  $(V_{CC+}) - 1.5$  V

**Related products:**

- See LM2904W for enhanced ESD performances

**Description**

This circuit consists of two independent, high gain operational amplifiers (op amps) that have frequency compensation implemented internally. They are designed specifically for automotive and industrial control systems. The circuit operates from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which can now be more easily implemented in single power supply systems. For example, these circuits can be directly supplied from the standard 5 V which is used in logic systems and easily provides the required interface electronics without requiring any additional power supply.

In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from a single power supply.

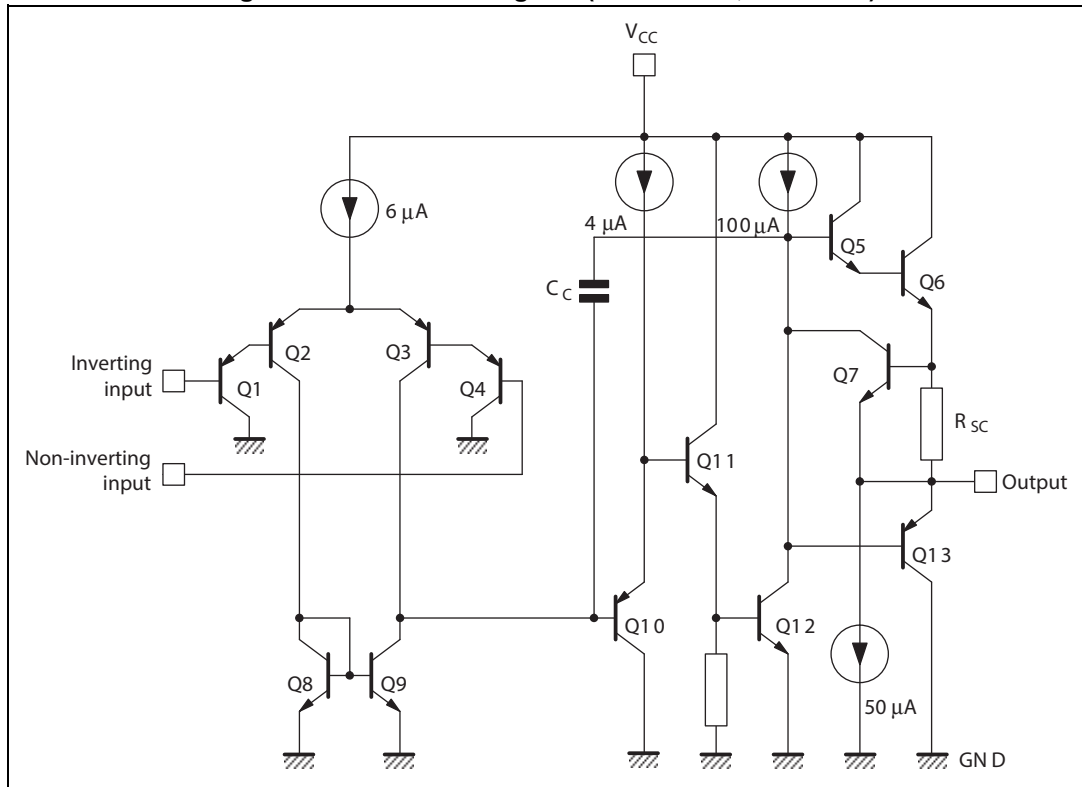
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# 1 Schematic diagram

Figure 1. Schematic diagram (1/2 LM2904, LM2904A)



## 2 Package pin connections

Figure 2. SO8, TSSOP8, and MiniSO8 package pin connections (top view)

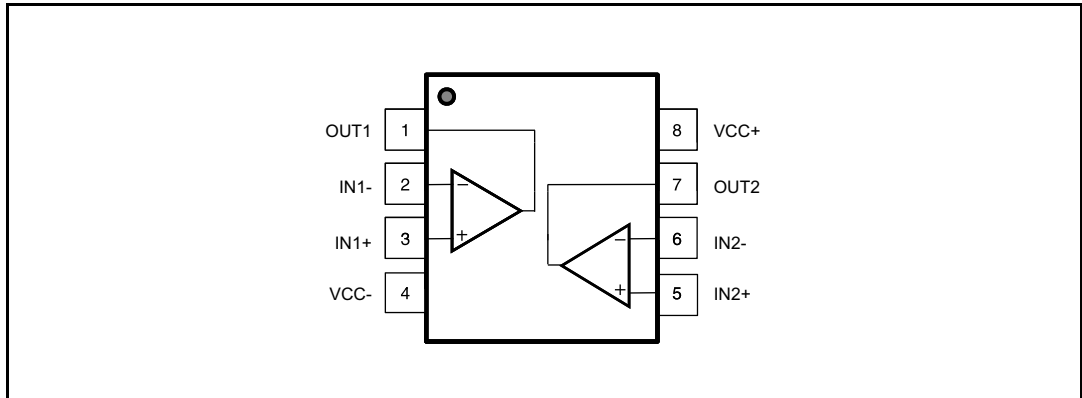
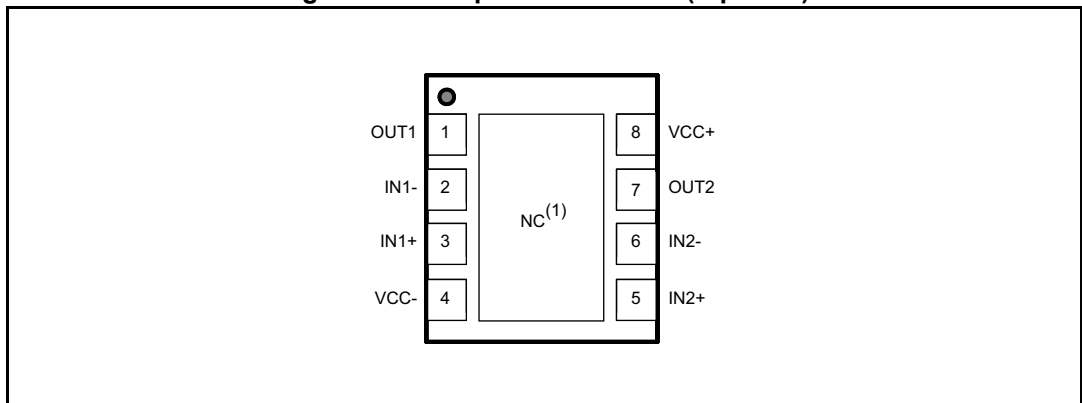


Figure 3. DFN8 pin connections (top view)



1. The exposed pad of the DFN8 2x2 can be connected to (VCC-) or left floating.

### 3 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>	±16 or 32	V
$V_{id}$	Differential input voltage <sup>(2)</sup>	±32	
$V_{in}$	Input voltage	-0.3 to 32	
	Output short-circuit duration <sup>(3)</sup>	Infinite	s
$I_{in}$	Input current <sup>(4)</sup> : $V_{in}$ driven negative	5 mA in DC or 50 mA in AC, (duty cycle = 10 %, T = 1 s)	mA
	Input current <sup>(5)</sup> : $V_{in}$ driven positive above AMR value	0.4	
$T_{oper}$	Operating free-air temperature range	-40 to 125	°C
$T_{stg}$	Storage temperature range	-65 to 150	
$T_j$	Maximum junction temperature	150	
$R_{thja}$	Thermal resistance junction to ambient <sup>(6)</sup>		°C/W
	SO8	125	
	TSSOP8	120	
	MiniSO8	190	
$R_{thjc}$	Thermal resistance junction to case <sup>(6)</sup>		°C/W
	SO8	40	
	TSSOP8	37	
	MiniSO8	39	
ESD	HBM: human body model <sup>(7)</sup>	300	V
	MM: machine model <sup>(8)</sup>	200	
	CDM: charged device model <sup>(9)</sup>	1.5	kV

- All voltage values, except differential voltage are with respect to network ground terminal.
- Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
- Short-circuits from the output to  $V_{CC}$  can cause excessive heating if ( $V_{CC+}$ ) > 15 V. The maximum output current is approximately 40 mA, independent of the magnitude of  $V_{CC}$ . Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
- This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward-biased and thereby acting as input diode clamp. In addition to this diode action, there is NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the  $V_{CC}$  voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3 V.
- The junction base/substrate of the input PNP transistor polarized in reverse must be protected by a resistor in series with the inputs to limit the input current to 400  $\mu$ A max ( $R = (V_{in}-32 V)/400 \mu$ A).
- Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
- Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kW resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
- Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5  $\Omega$ ). This is done for all couples of connected pin combinations while the other pins are floating.
- Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	3 to 30	V
$V_{icm}$	Common-mode input voltage range	0 to $(V_{CC+}) - 1.5$	
$T_{oper}$	Operating free-air temperature range	-40 to 125	°C

## 4 Electrical characteristics

Table 3.  $V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = \text{ground}$ ,  $V_O = 1.4\text{ V}$ ,  $T_{\text{amb}} = 25\text{ °C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input offset voltage, $T_{\text{amb}} = 25\text{ °C}$ , LM2904 <sup>(1)</sup>		2	7	mV
	Input offset voltage, $T_{\text{amb}} = 25\text{ °C}$ , LM2904A <sup>(1)</sup>		1	2	
	Input offset voltage, $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$ , LM2904 <sup>(1)</sup>			9	
	Input offset voltage, $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$ , LM2904A <sup>(1)</sup>			4	
$\Delta V_{io}/\Delta T$	Input offset voltage drift		7	30	$\mu\text{V}/\text{°C}$
$I_{io}$	Input offset current, $T_{\text{amb}} = 25\text{ °C}$		2	30	nA
	Input offset current, $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$			40	
$\Delta I_{io}/\Delta T$	Input offset current drift		10	300	$\text{pA}/\text{°C}$
$I_{ib}$	Input bias current, $T_{\text{amb}} = 25\text{ °C}$ <sup>(2)</sup>		20	150	nA
	Input bias current, $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$ <sup>(2)</sup>			200	
$A_{vd}$	Large signal voltage gain, $V_{CC+} = 15\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $V_O = 1.4\text{ V}$ to $11.4\text{ V}$ , $T_{\text{amb}} = 25\text{ °C}$	50	100		V/mV
	Large signal voltage gain, $V_{CC+} = 15\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $V_O = 1.4\text{ V}$ to $11.4\text{ V}$ , $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	25			
SVR	Supply voltage rejection ratio ( $R_S \leq 10\text{ k}\Omega$ ), $T_{\text{amb}} = 25\text{ °C}$	65	100		dB
	Supply voltage rejection ratio ( $R_S \leq 10\text{ k}\Omega$ ), $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	65			
$I_{CC}$	Supply current, all amp, no load, $T_{\text{amb}} = 25\text{ °C}$ , $V_{CC+} = 5\text{ V}$		0.7	1.2	mA
	Supply current, all amp, no load, $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$ , $V_{CC+} = 30\text{ V}$			2	
$V_{icm}$	Input common mode voltage range ( $V_{CC+} = 30\text{ V}$ ), $T_{\text{amb}} = 25\text{ °C}$ <sup>(3)</sup>	0		$(V_{CC+}) - 1.5$	V
	Input common mode voltage range ( $V_{CC+} = 30\text{ V}$ ), $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	0		$(V_{CC+}) - 2$	
CMR	Common-mode rejection ratio ( $R_S = 10\text{ k}\Omega$ ), $T_{\text{amb}} = 25\text{ °C}$	70	85		dB
	Common-mode rejection ratio ( $R_S = 10\text{ k}\Omega$ ), $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	60			
$I_{\text{source}}$	Output short-circuit current, $V_{CC+} = 15\text{ V}$ , $V_O = 2\text{ V}$ , $V_{id} = 1\text{ V}$	20	40	60	mA
$I_{\text{sink}}$	Output sink current, $V_O = 2\text{ V}$ , $V_{CC+} = 5\text{ V}$	10	20		
		Output sink current, $V_O = 0.2\text{ V}$ , $V_{CC+} = 15\text{ V}$	12	50	$\mu\text{A}$

Table 3.  $V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = \text{ground}$ ,  $V_O = 1.4\text{ V}$ ,  $T_{\text{amb}} = 25\text{ }^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{OH}$	High level output voltage ( $V_{CC+} = 30\text{ V}$ ), $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ , $R_L = 2\text{ k}\Omega$	26			V
	High level output voltage ( $V_{CC+} = 30\text{ V}$ ), $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	26	27		
	High level output voltage ( $V_{CC+} = 30\text{ V}$ ), $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ , $R_L = 10\text{ k}\Omega$	27			
	High level output voltage ( $V_{CC+} = 30\text{ V}$ ), $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	27	28		
$V_{OL}$	Low level output voltage ( $R_L = 10\text{ k}\Omega$ ), $T_{\text{amb}} = 25\text{ }^\circ\text{C}$		5	20	V
	Low level output voltage ( $R_L = 10\text{ k}\Omega$ ), $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$			20	
SR	Slew rate, $V_{CC+} = 15\text{ V}$ , $V_{\text{in}} = 0.5\text{ to }3\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , unity gain, $T_{\text{amb}} = 25\text{ }^\circ\text{C}$	0.3	0.6		V/ $\mu\text{s}$
	Slew rate, $V_{CC+} = 15\text{ V}$ , $V_{\text{in}} = 0.5\text{ to }3\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , unity gain, $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	0.2			
GBP	Gain bandwidth product $f = 100\text{ kHz}$ , $V_{CC+} = 30\text{ V}$ , $V_{\text{in}} = 10\text{ mV}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$	0.7	1.1		MHz
THD	Total harmonic distortion, $f = 1\text{ kHz}$ , $A_V = 20\text{ dB}$ , $R_L = 2\text{ k}\Omega$ , $V_o = 2\text{ V}_{pp}$ , $C_L = 100\text{ pF}$ , $V_{CC+} = 30\text{ V}$		0.02		%
$e_n$	Equivalent input noise voltage, $f = 1\text{ kHz}$ , $R_S = 100\text{ }\Omega$ , $V_{CC+} = 30\text{ V}$		55		nV/ $\sqrt{\text{Hz}}$
$V_{O1}/V_{O2}$	Channel separation, $1\text{ kHz} \leq f \leq 20\text{ kHz}$ <sup>(4)</sup>		120		dB

- $V_O = 1.4\text{ V}$ ,  $R_S = 0\text{ }\Omega$ ,  $5\text{ V} < V_{CC+} < 30\text{ V}$ ,  $0\text{ V} < V_{\text{ic}} < (V_{CC+}) - 1.5\text{ V}$ .
- The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output, so there is no change in the loading charge on the input lines.
- The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is  $(V_{CC+}) - 1.5\text{ V}$ , but either or both inputs can go to +32 V without damage.
- Due to the proximity of external components, ensure that the stray capacitance does not cause coupling between these external parts. This can typically be detected at higher frequencies because this type of capacitance increases.



Figure 4. Open-loop frequency response

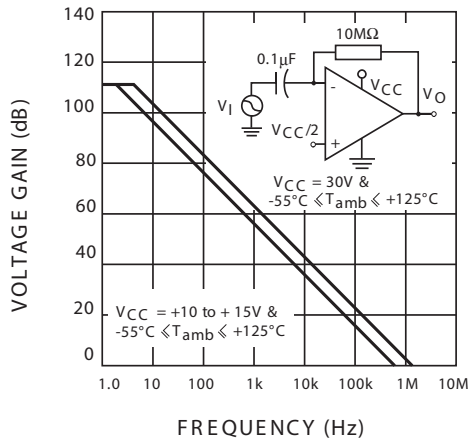


Figure 5. Large signal frequency response

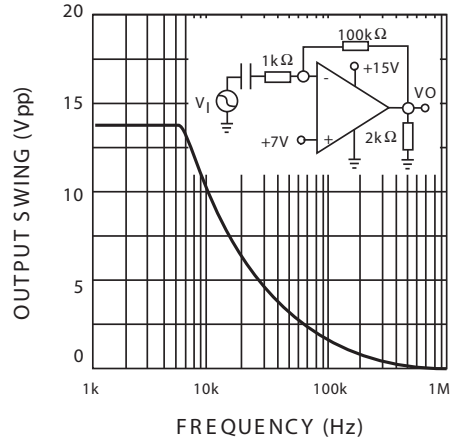


Figure 6. Voltage follower large signal response

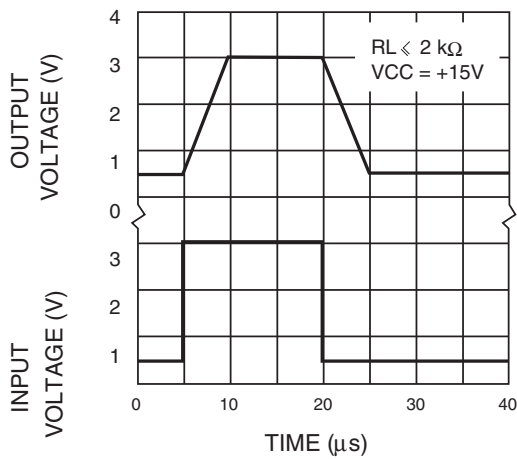


Figure 7. Current sinking output characteristics

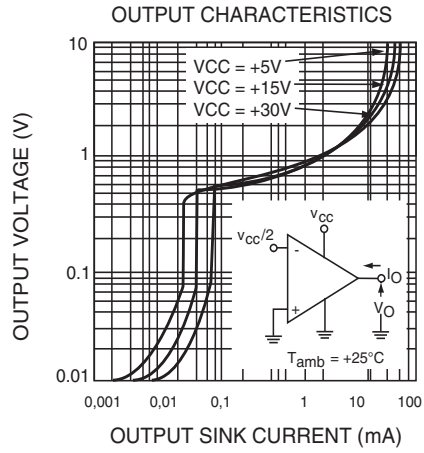


Figure 8. Voltage follower small signal response

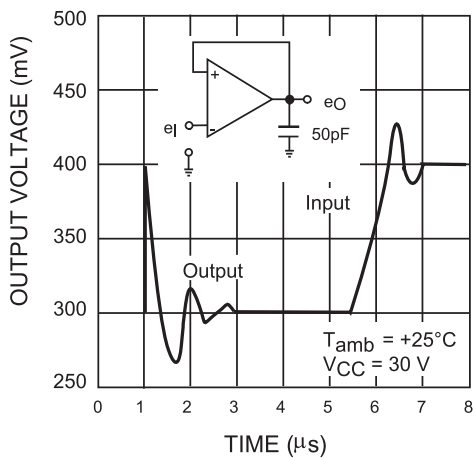


Figure 9. Current sourcing output characteristics

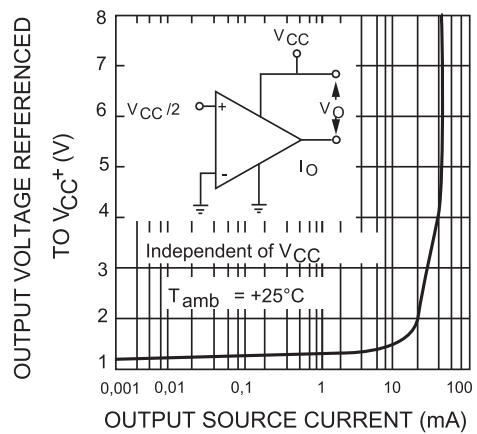


Figure 10. Input current versus temperature

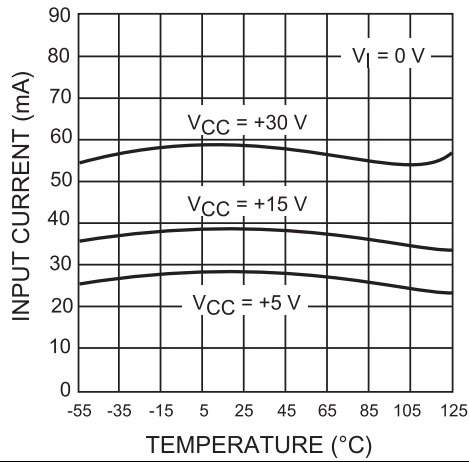


Figure 11. Current limiting

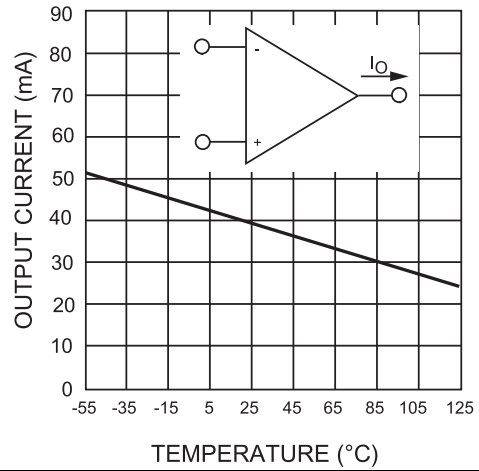


Figure 12. Input voltage range

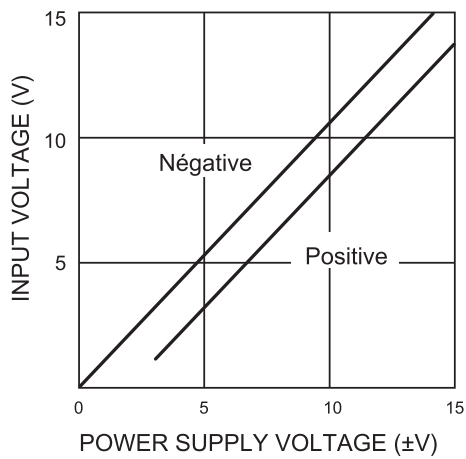


Figure 13. Supply current

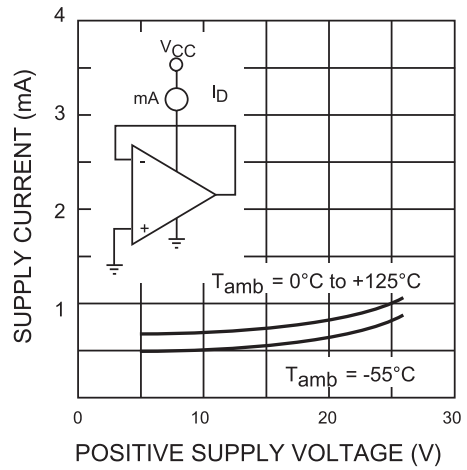


Figure 14. Voltage gain

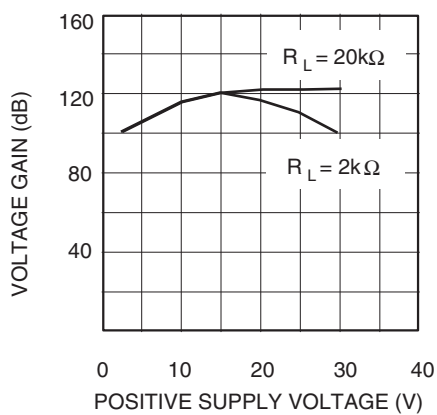
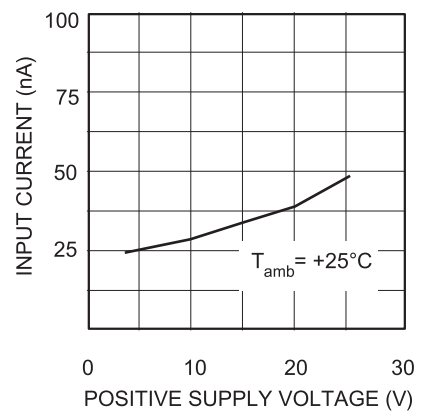
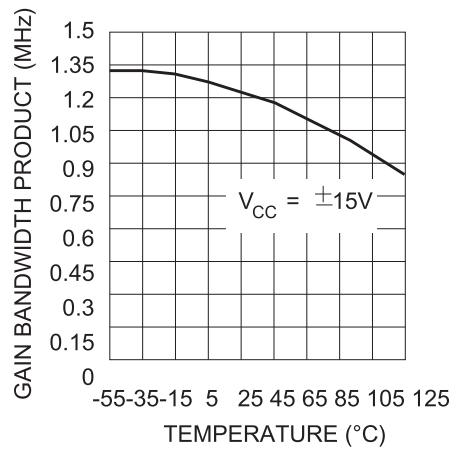


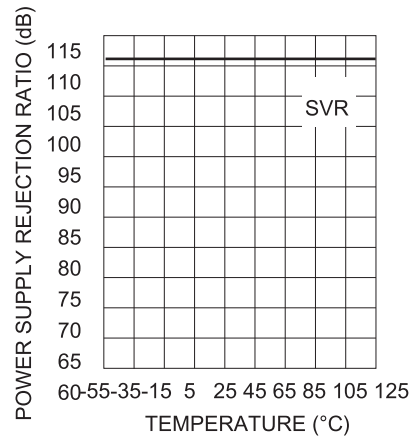
Figure 15. Input current versus supply voltage



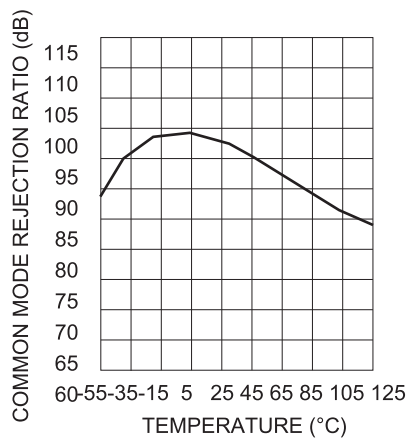
**Figure 16. Gain bandwidth product**



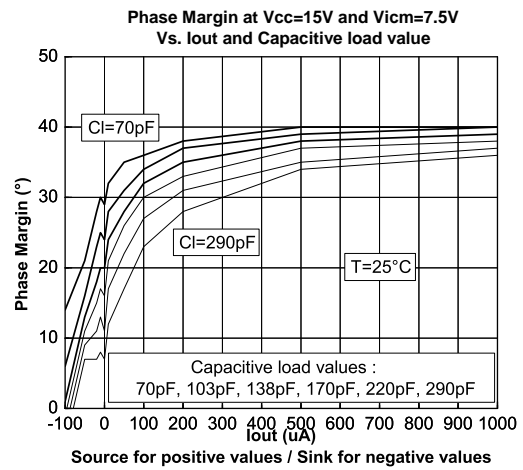
**Figure 17. Power supply rejection ratio**



**Figure 18. Common-mode rejection ratio**

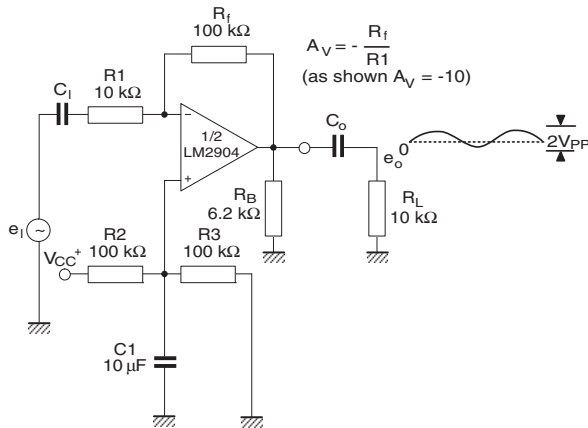


**Figure 19. Phase margin vs capacitive load**

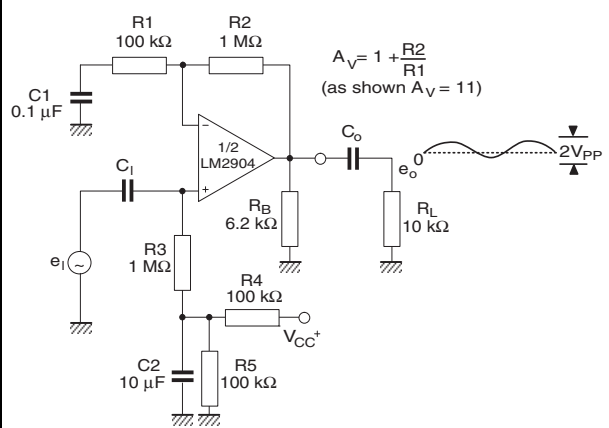


### 4.1 Typical single-supply applications

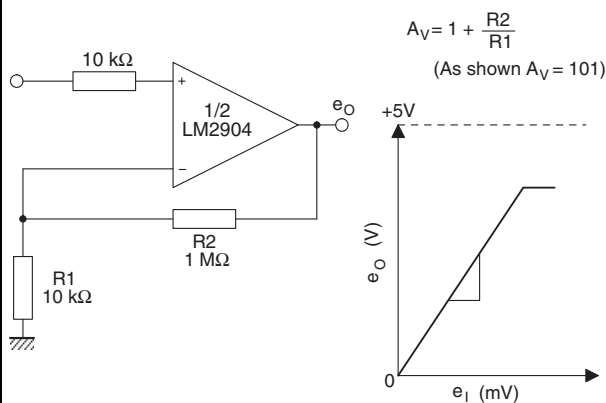
**Figure 20. AC coupled inverting amplifier**



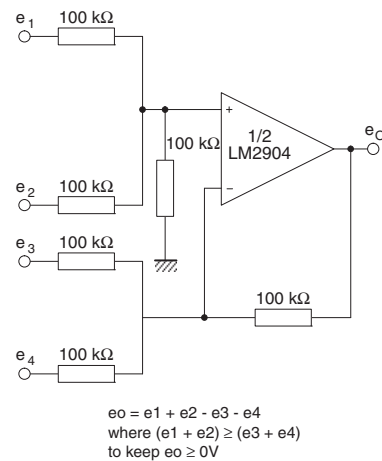
**Figure 21. AC coupled non-inverting amplifier**



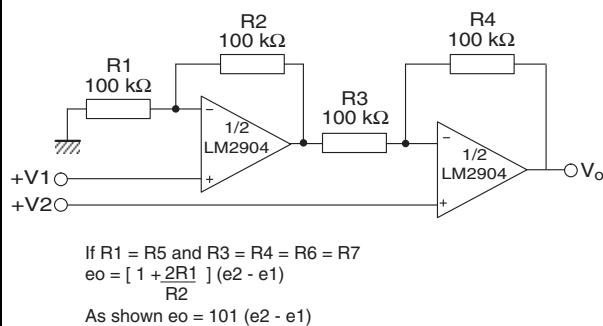
**Figure 22. Non-inverting DC gain**



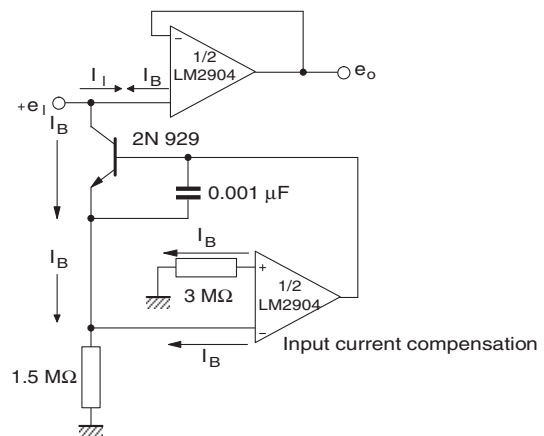
**Figure 23. DC summing amplifier**

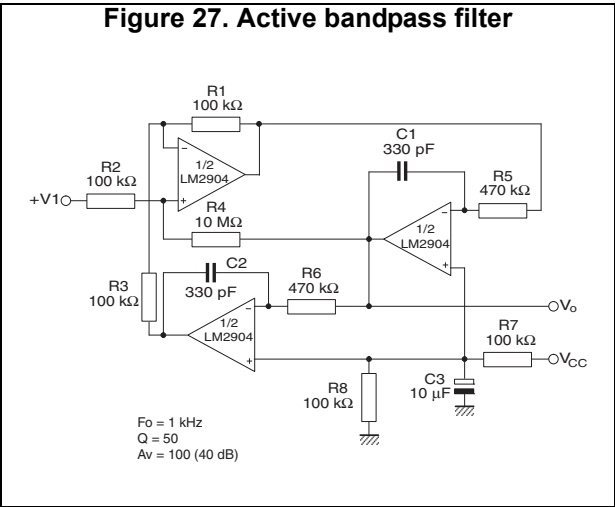
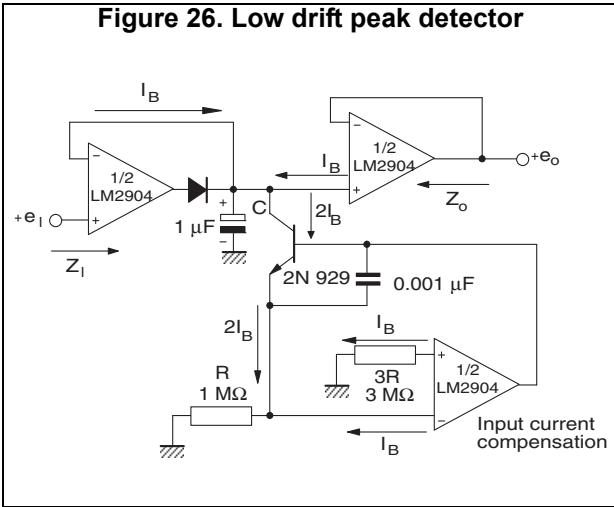


**Figure 24. High input Z, DC differential amplifier**



**Figure 25. Using symmetrical amplifiers to reduce input current**





## 5 Macromodel

An accurate macromodel of the LM2904, LM2904A is available on STMicroelectronics' web site at: [www.st.com](http://www.st.com). This model is a trade-off between accuracy and complexity (that is, time simulation) of the LM2904, LM2904A operational amplifier. It emulates the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. It also helps to validate a design approach and to select the right operational amplifier, *but it does not replace on-board measurements*.

## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 6.1 SO8 package information

Figure 28. SO8 package outline

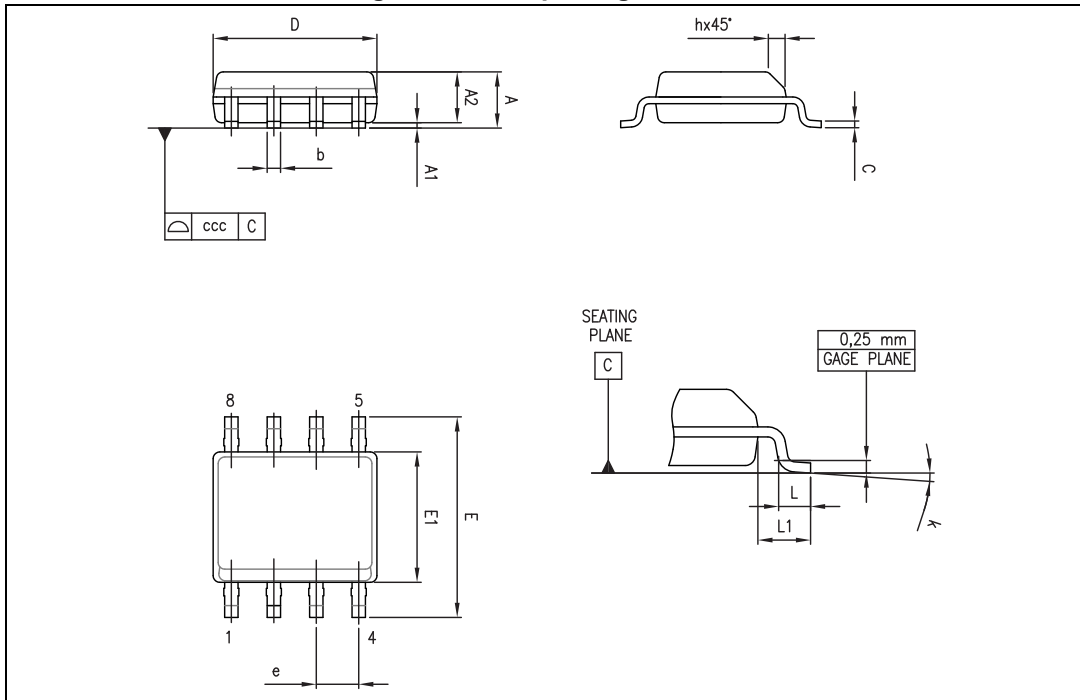


Table 4. SO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004



## 6.2 TSSOP8 package information

Figure 29. TSSOP8 package outline

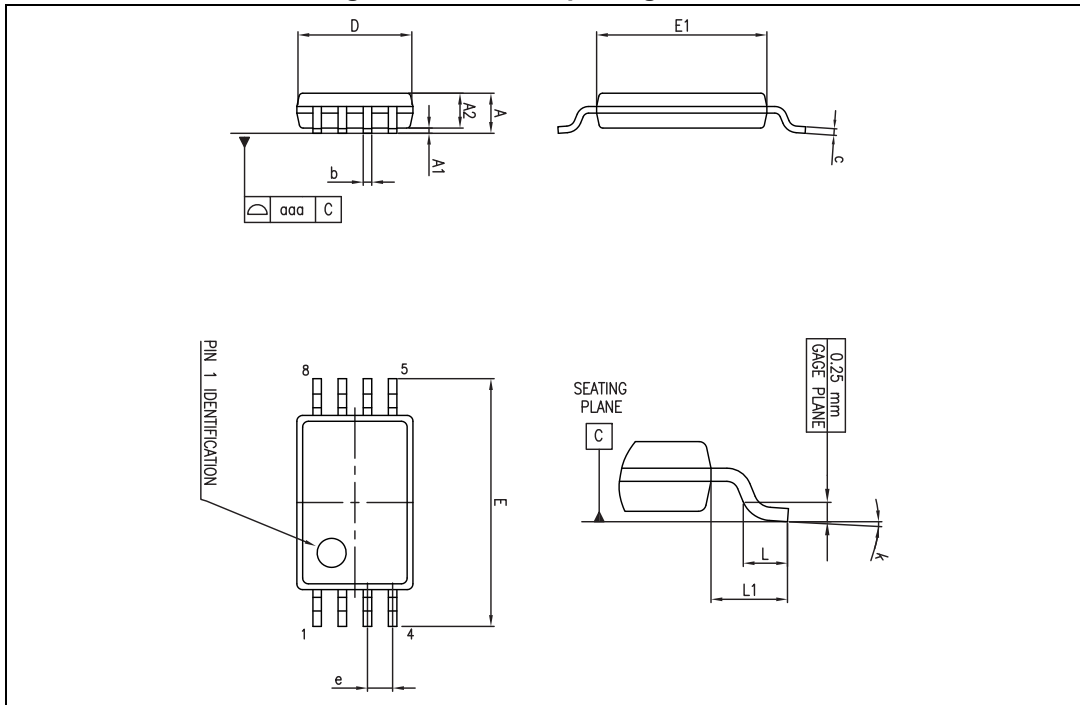


Figure 30. TSSOP8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa			0.10			0.004

### 6.3 MiniSO8 package information

Figure 31. MiniSO8 package outline

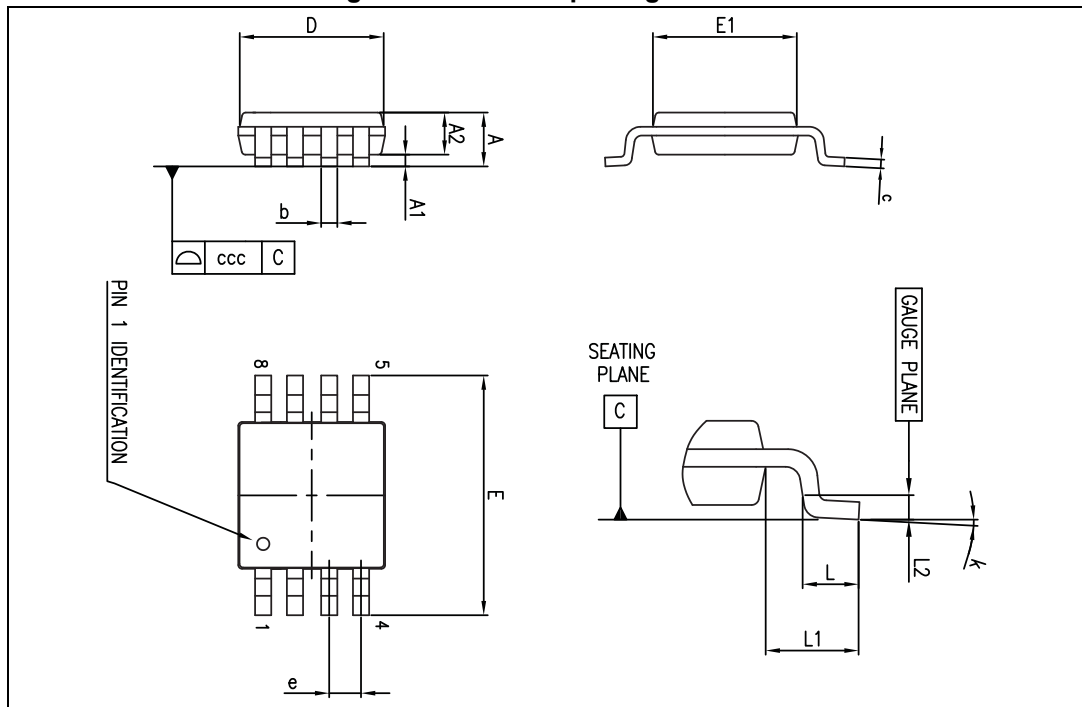


Table 5. MiniSO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

### 6.4 DFN8 2 x 2 mm package information

Figure 32. DFN8 2 x 2 mm package outline

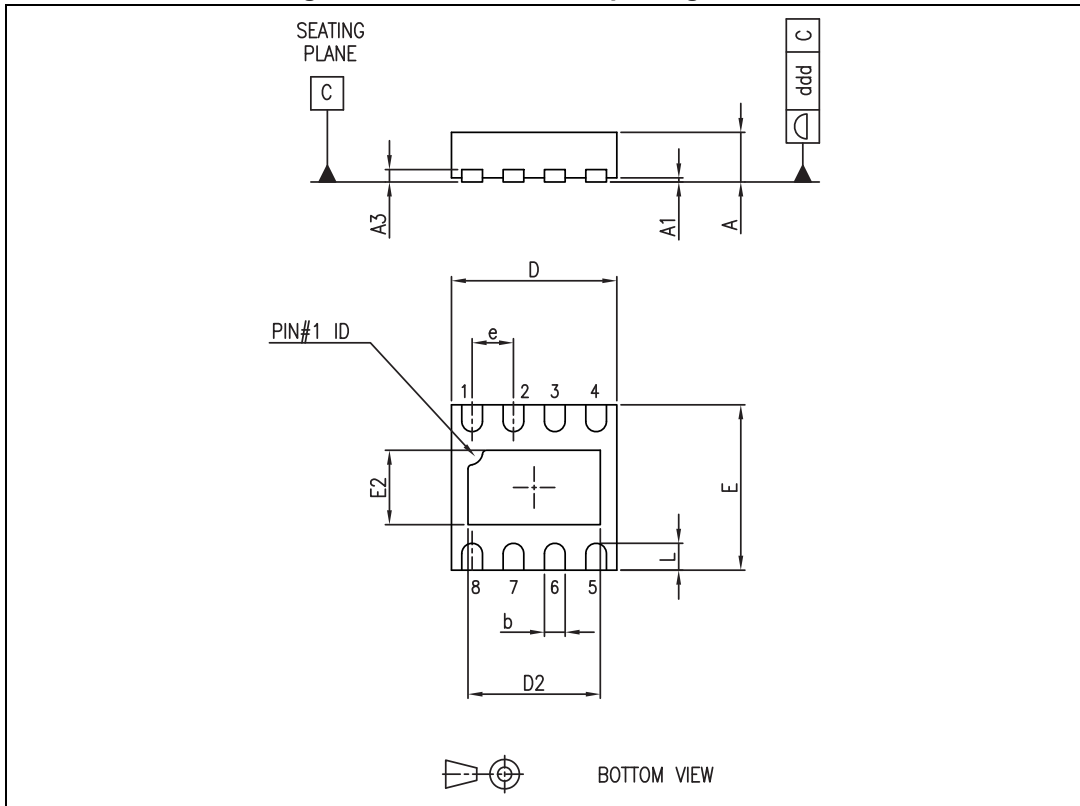
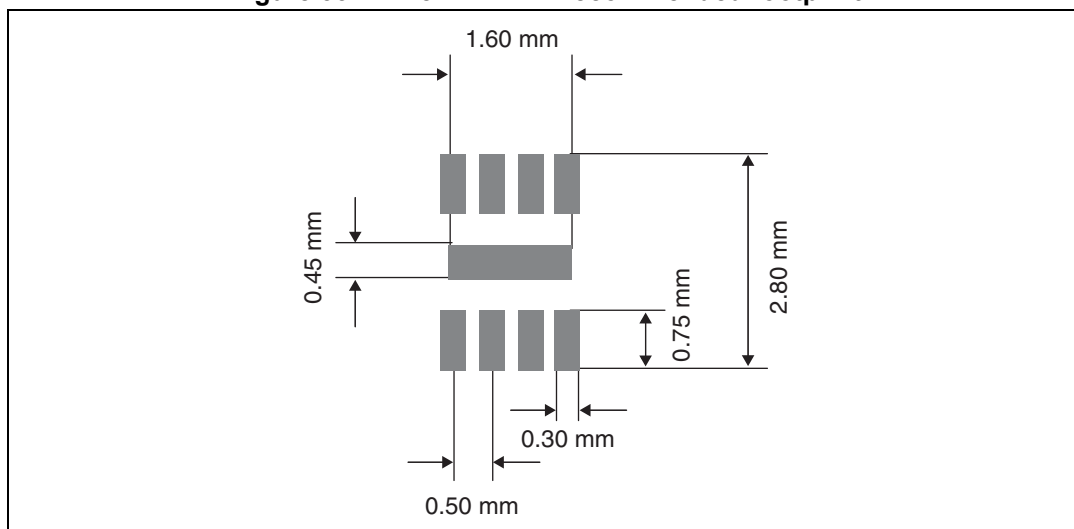


Table 6. DFN8 2 x 2 mm mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L			0.50			0.020
ddd			0.08			0.003

Figure 33. DFN8 2 x 2 mm recommended footprint



## 7 Ordering information

**Table 7. Order codes**

Order code	Temperature range	Package	Packing	Marking
LM2904D/DT	-40 °C to 125 °C	SO8	Tube or tape and reel	2904
LM2904PT		TSSOP8	Tape and reel	
LM2904ST		MiniSO8		K403
LM2904Q2T		DFN8 2 x 2		K1Y
LM2904YDT <sup>(1)</sup>		SO8		2904Y
LM2904AYDT <sup>(1)</sup>		(automotive grade level)		2904AY
LM2904YPT <sup>(2)</sup>		TSSOP8		2904Y
LM2904AYPT <sup>(2)</sup>		(automotive grade level)		904AY
LM2904YST <sup>(1)</sup>		MiniSO8	K409	
		(automotive grade level)		

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.
2. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.

## 8 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
02-Jan-2002	1	Initial release.
20-Jun-2005	2	PPAP references inserted in the datasheet, see <a href="#">Table 9 on page 21</a> . ESD protection inserted in <a href="#">Table 1 on page 5</a> .
10-Oct-2005	3	PPAP part numbers added in table <a href="#">Table 9 on page 21</a> .
12-Dec-2005	4	Pin connections identification added on cover page figure. Thermal resistance junction to case information added see <a href="#">Table 1 on page 5</a> .
01-Feb-2006	5	Maximum junction temperature parameter added in <a href="#">Table 1 on page 5</a> .
02-May-2006	6	Minimum slew rate parameter in temperature <a href="#">Table 3 on page 7</a> .
13-Jul-2006	7	Modified ESD values and added explanation on $V_{CC}$ , $V_{id}$ in <a href="#">Table 1 on page 5</a> . Added macromodel information.
28-Feb-2007	8	Modified ESD/HBM values in <a href="#">Table 1 on page 5</a> . Updated MiniSO8 package information. Added note relative to automotive grade level part numbers in <a href="#">Table 9 on page 21</a> .
18-Jun-2007	9	Power dissipation value corrected in <a href="#">Table 1: Absolute maximum ratings</a> . <a href="#">Table 2: Operating conditions</a> added. Equivalent input noise voltage parameter added in <a href="#">Table 3</a> . Electrical characteristics curves updated. <a href="#">Figure 19: Phase margin vs capacitive load</a> added. <a href="#">Section 6: Package information</a> updated.
18-Dec-2007	10	Removed power dissipation parameter from <a href="#">Table 1: Absolute maximum ratings</a> . Removed $V_{opp}$ from electrical characteristics in <a href="#">Table 3</a> . Corrected MiniSO8 package mechanical data in <a href="#">Section 6.4: MiniSO8 package information</a> .
08-Apr-2008	11	Added table of contents. Corrected the scale of <a href="#">Figure 7</a> (mA not $\mu$ A). Corrected SO8 package information.
02-Jun-2009	12	Added input current information in <a href="#">Table 1: Absolute maximum ratings</a> . Added L1 parameters in <a href="#">Table 6: SO8 package mechanical data</a> . Added new order codes, LM2904AYD/DT, LM2904AYPT and LM2904AYST in <a href="#">Table 9: Order codes</a> .
13-Apr-2010	13	Added LM2904A on cover page. Corrected footnote (5) in <a href="#">Table 1: Absolute maximum ratings</a> . Removed order code LM2904AYST from <a href="#">Table 9: Order codes</a> .

Table 8. Document revision history (continued)

Date	Revision	Changes
24-Jan-2012	14	<p>Removed macromodel from <a href="#">Chapter 5</a> (now available on <a href="http://www.st.com">www.st.com</a>).</p> <p>Added DFN8 2 x 2 mm package information in <a href="#">Chapter 6</a> and related order codes in <a href="#">Chapter 7</a>.</p> <p>Removed LM2904YD and LM2904AYD order codes from <a href="#">Table 9</a>.</p> <p>Changed note for LM2904YST order code in <a href="#">Table 9</a>.</p>
24-Jan-2014	15	<p>Updated: marking info for LM2904AYPT, package silhouette drawings in the cover page, <math>\Delta V_{iQ}/\Delta T</math> and <math>\Delta I_{iQ}/\Delta T</math> symbols in <a href="#">Table 3 on page 7</a></p> <p>Added: ESD info in <a href="#">Features section</a> and <a href="#">Section 2: Package pin connections</a></p> <p>Removed: LM2904N from <a href="#">Table 9: Order codes</a>.</p>
02-Oct-2015	16	<p><a href="#">Figure 1: Schematic diagram (1/2 LM2904, LM2904A)</a>: updated</p>

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