STD11N65M2, STP11N65M2, STU11N65M2

N-channel 650 V, 0.6 Ω typ., 7 A MDmesh™ M2 Power MOSFET in DPAK, TO-220 and IPAK packages

Datasheet - production data

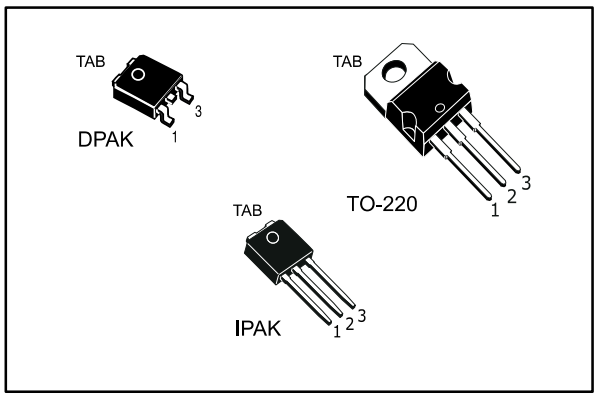
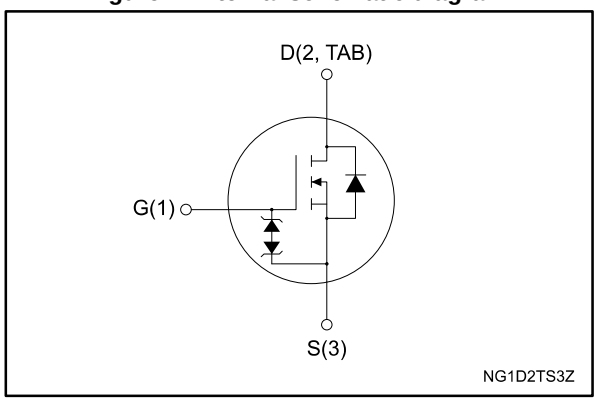


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD11N65M2	650 V	0.68 Ω	7 A	85 W
STP11N65M2				
STU11N65M2				

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STD11N65M2	11N65M2	DPAK	Tape and reel
STP11N65M2		TO-220	Tube
STU11N65M2		IPAK	

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	7	A
	Drain current (continuous) at T_{case} = 100 °C	4.4	
I_{DM}(1)	Drain current (pulsed)	28	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	85	W
dv/dt(2)(3)	Peak diode recovery voltage slope	15	V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Operating junction temperature		

Notes:

(1) Pulse width limited by T_{jmax}.

(2) starting T_j = 25 °C, I_D = I_{AS}, V_{DD} = 50 V.

(3) I_{SD} ≤ 7 A, di/dt=400 A/µs, V_{DS} peak < $V_{(BR)DSS}$ V_{DD} = 80% $V_{(BR)DSS}$.

(4) V_{DS} ≤ 520 V.

Table 3: Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220	IPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.47			°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient		62.5	100	
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	50			

Notes:

(1) When mounted on a 1-inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}(1)	Avalanche current, repetitive or not repetitive	1.5	A
E_{AS}(2)	Single pulse avalanche energy	110	mJ

Notes:

(1) Pulse width limited by T_{jmax}.

(2) starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_{case} = 125 °C			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3.5 A		0.6	0.68	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	410	-	pF
C_{oss}	Output capacitance		-	20	-	
C_{rss}	Reverse transfer capacitance		-	0.95	-	
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	83	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	6.4	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 7 A, V_{GS} = 10 V (see *Figure 17: "Gate charge test circuit"*)	-	12.5	-	nC
Q_{gs}	Gate-source charge		-	3.2	-	
Q_{gd}	Gate-drain charge		-	5.8	-	

Notes:

(1) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 3.5 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 16: "Switching times test circuit for resistive load"* and *Figure 21: "Switching time waveform"*)	-	9.5	-	ns
t_r	Rise time		-	7.5	-	
$t_{d(off)}$	Turn-off delay time		-	26	-	
t_f	Fall time		-	15	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7	A
I_{SDM}(1)	Source-drain current (pulsed)		-		28	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 7 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 7 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 18: "Test circuit for inductive load switching and diode recovery times"*)	-	318		ns
Q_{rr}	Reverse recovery charge		-	2.5		µC
I_{RRM}	Reverse recovery current		-	15.5		A
t_{rr}	Reverse recovery time	I_{SD} = 7 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 18: "Test circuit for inductive load switching and diode recovery times"*)	-	437		ns
Q_{rr}	Reverse recovery charge		-	3.2		µC
I_{RRM}	Reverse recovery current		-	15		A

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for DPAK and IPAK

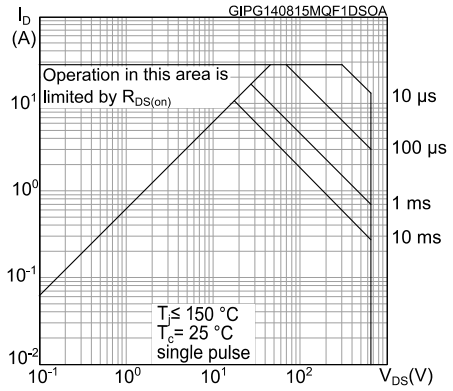


Figure 3: Thermal impedance for DPAK and IPAK

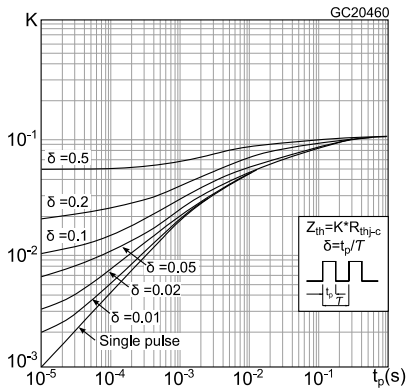


Figure 4: Safe operating area for TO-220

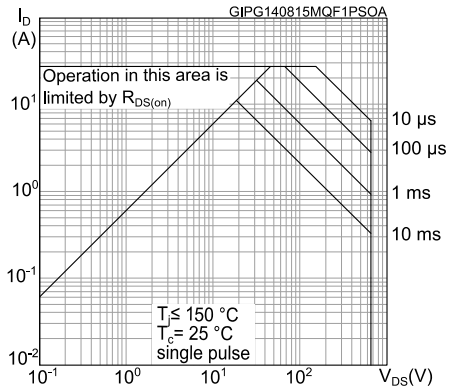


Figure 5: Thermal impedance for TO-220

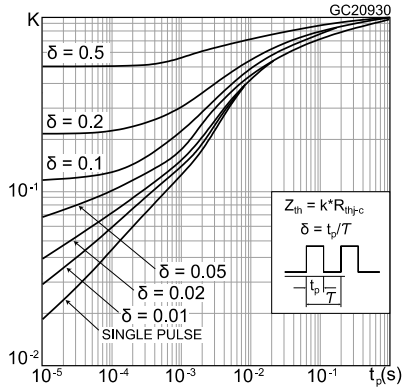


Figure 6: Output characteristics

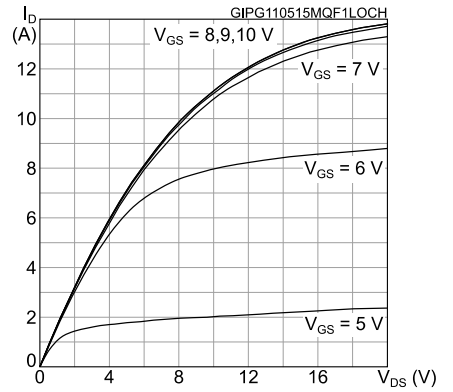


Figure 7: Transfer characteristics

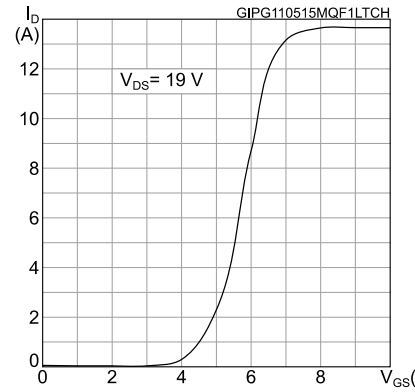


Figure 8: Gate charge vs gate-source voltage

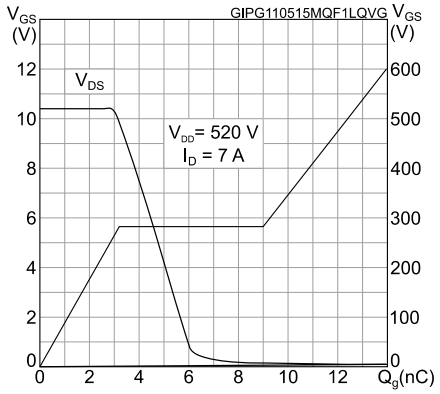


Figure 9: Static drain-source on-resistance

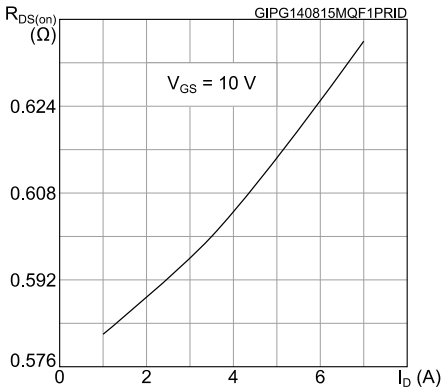


Figure 10: Capacitance variations

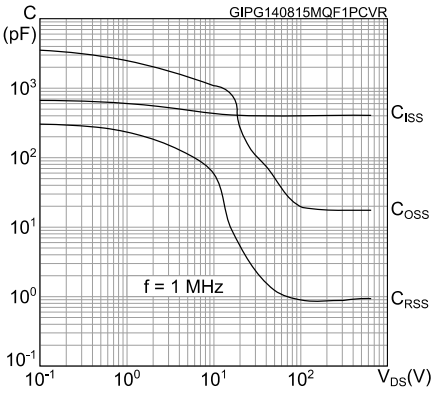


Figure 11: Normalized gate threshold voltage vs temperature

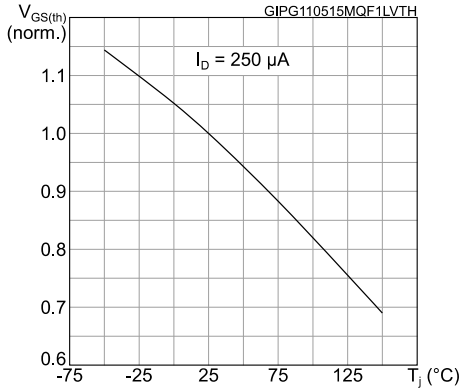


Figure 12: Normalized on-resistance vs temperature

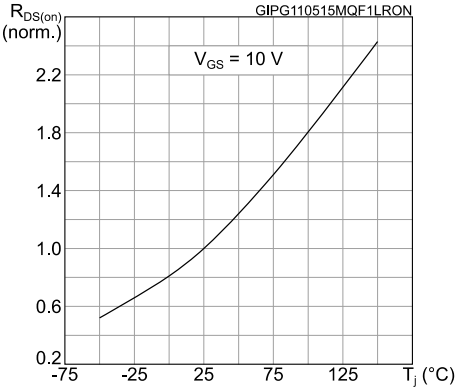


Figure 13: Normalized V(BR)DSS vs temperature

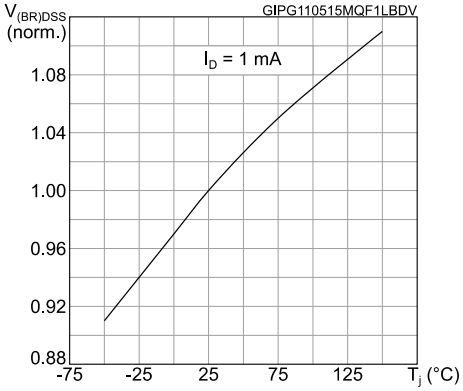


Figure 14: Output capacitance stored energy

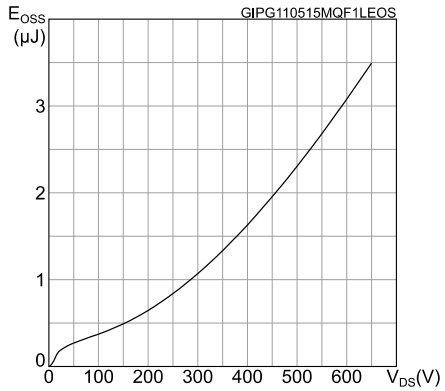
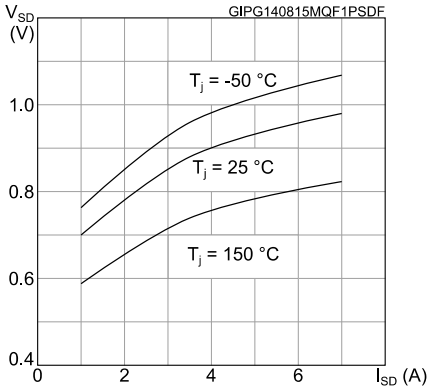


Figure 15: Source- drain diode forward characteristics



3 Test circuits

Figure 16: Switching times test circuit for resistive load

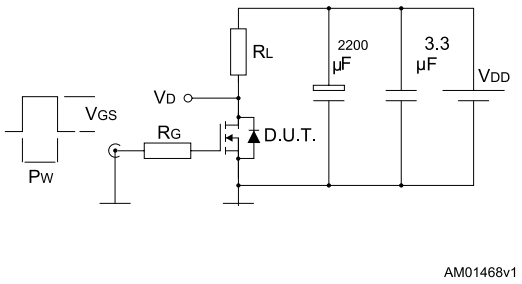


Figure 17: Gate charge test circuit

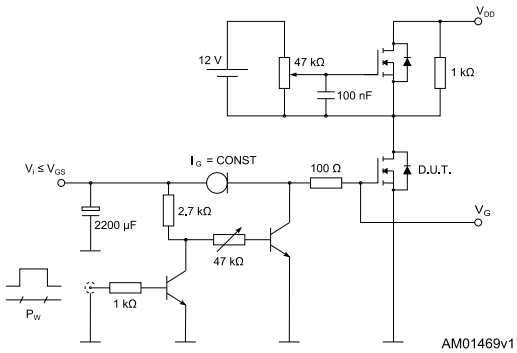


Figure 18: Test circuit for inductive load switching and diode recovery times

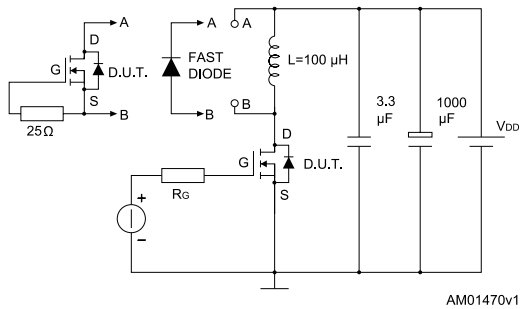


Figure 19: Unclamped inductive load test circuit

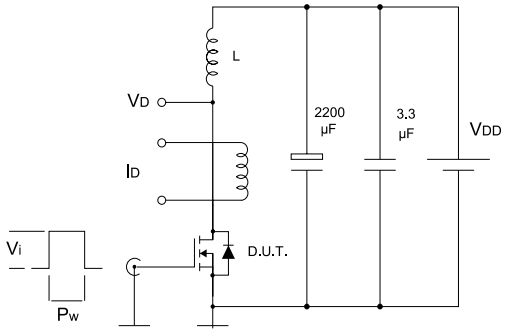


Figure 20: Unclamped inductive waveform

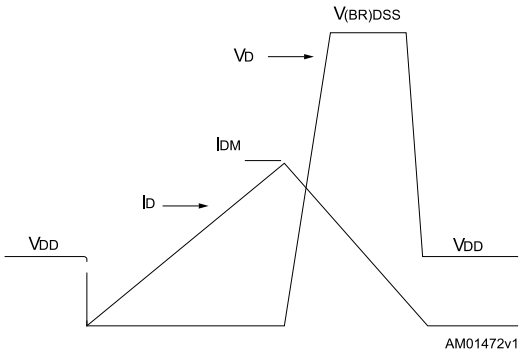
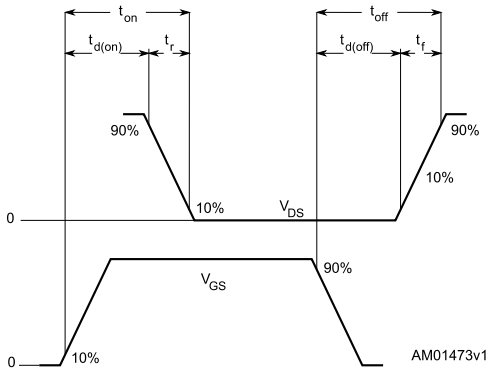


Figure 21: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 22: DPAK (TO-252) type A package outline

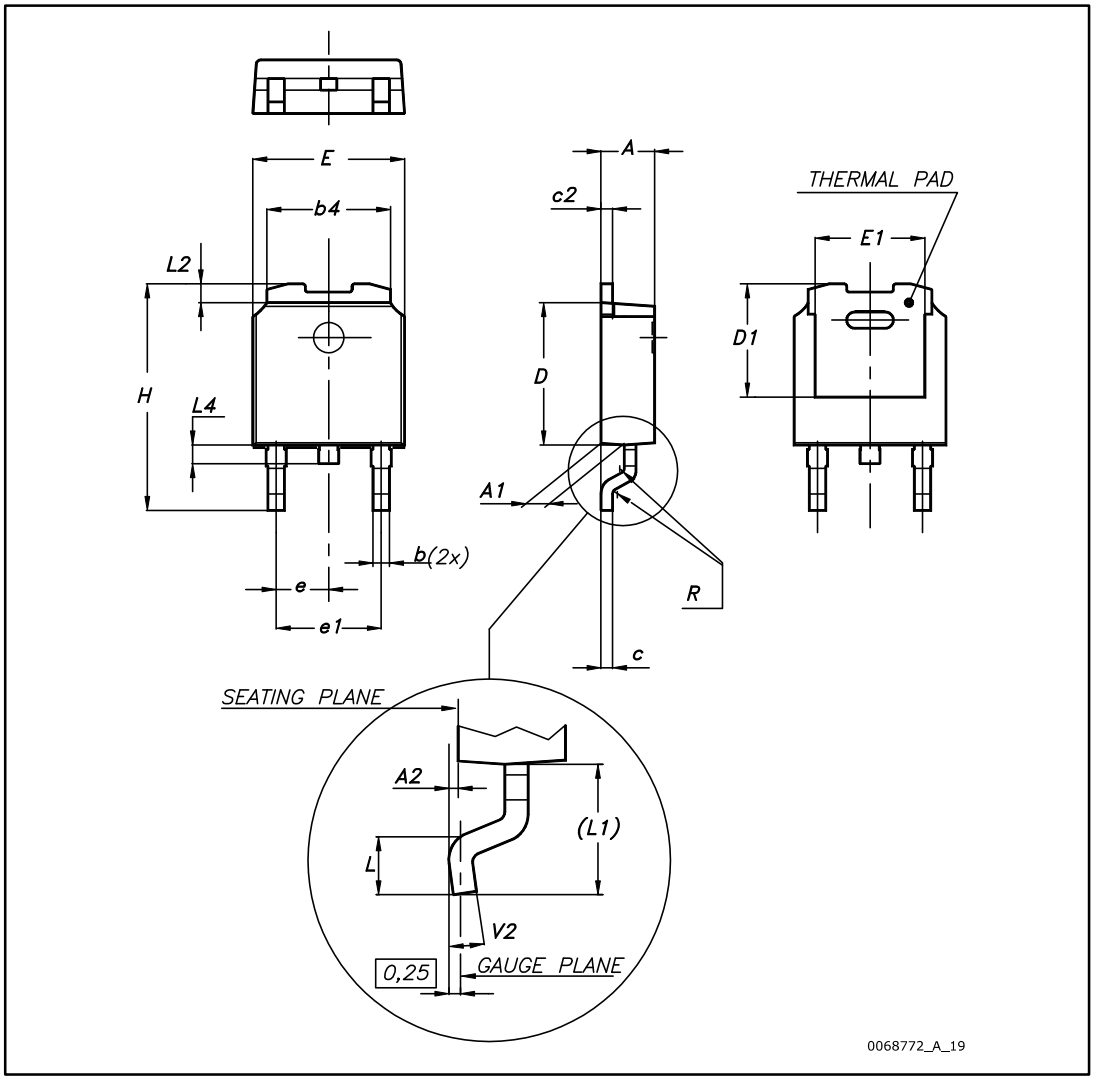
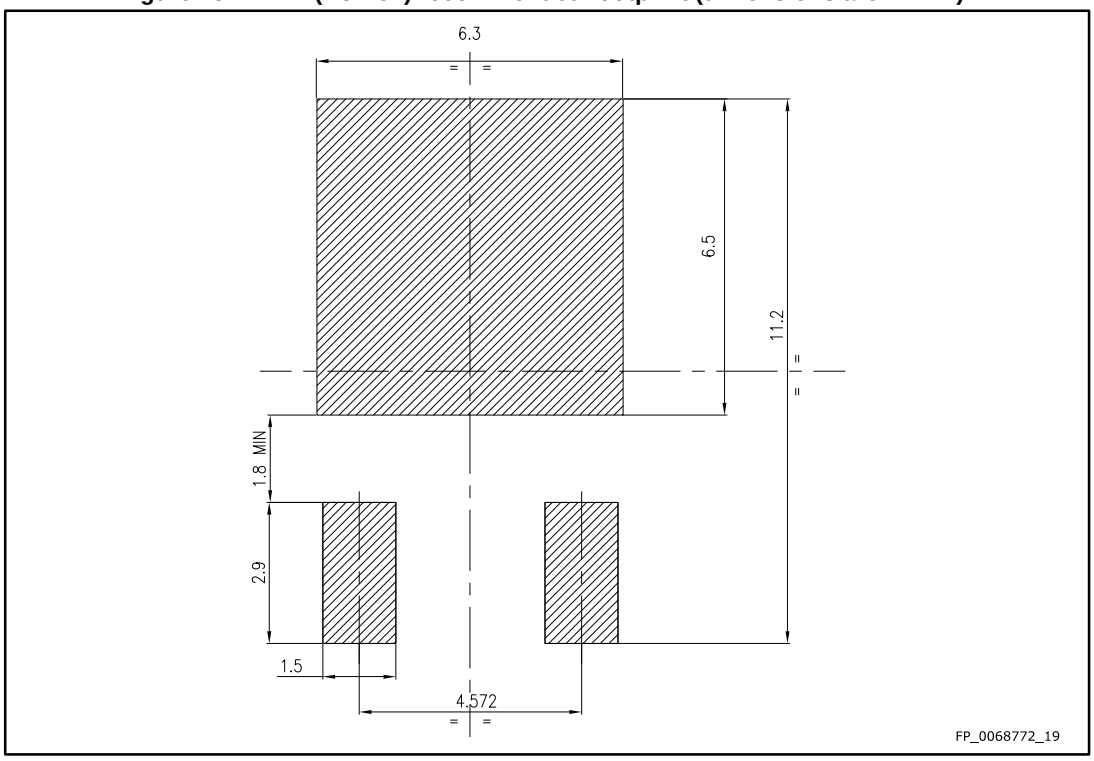


Table 9: DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 23: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) packing information

Figure 24: DPAK (TO-252) tape outline

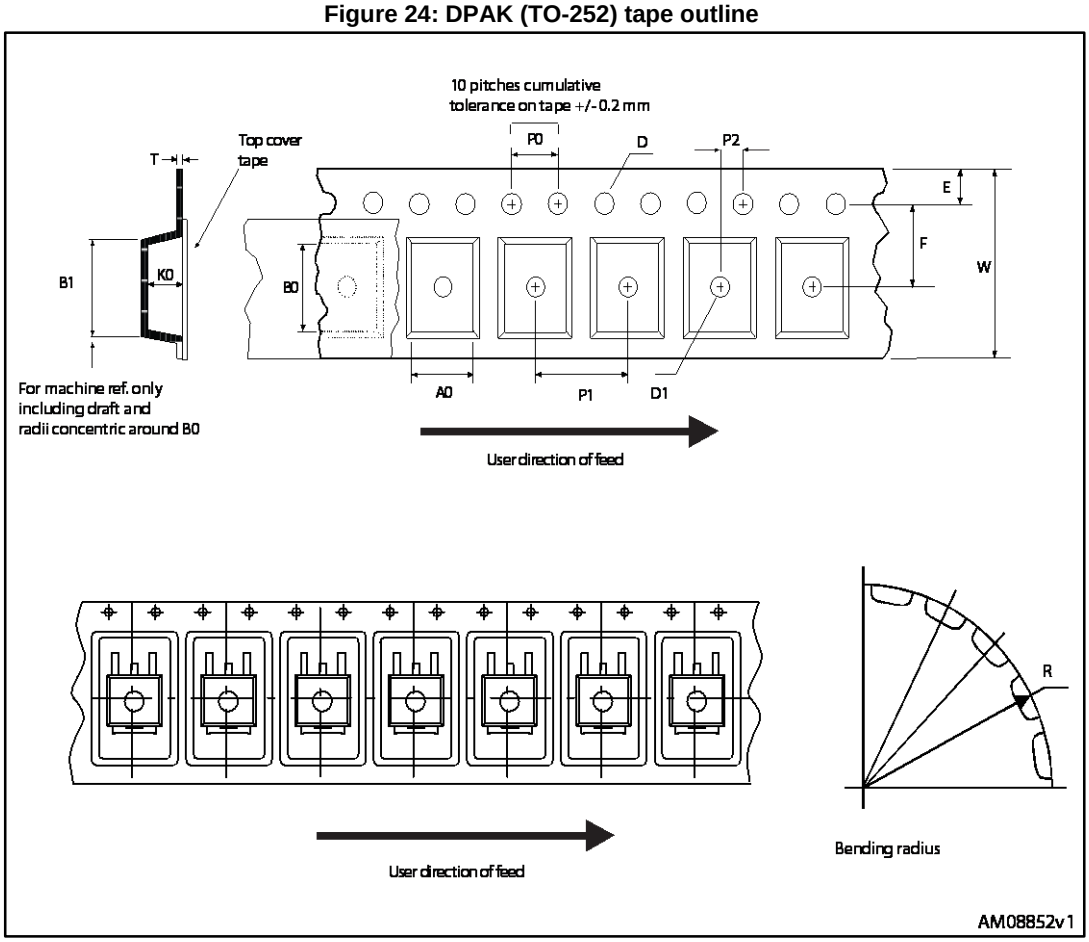


Figure 25: DPAK (TO-252) reel outline

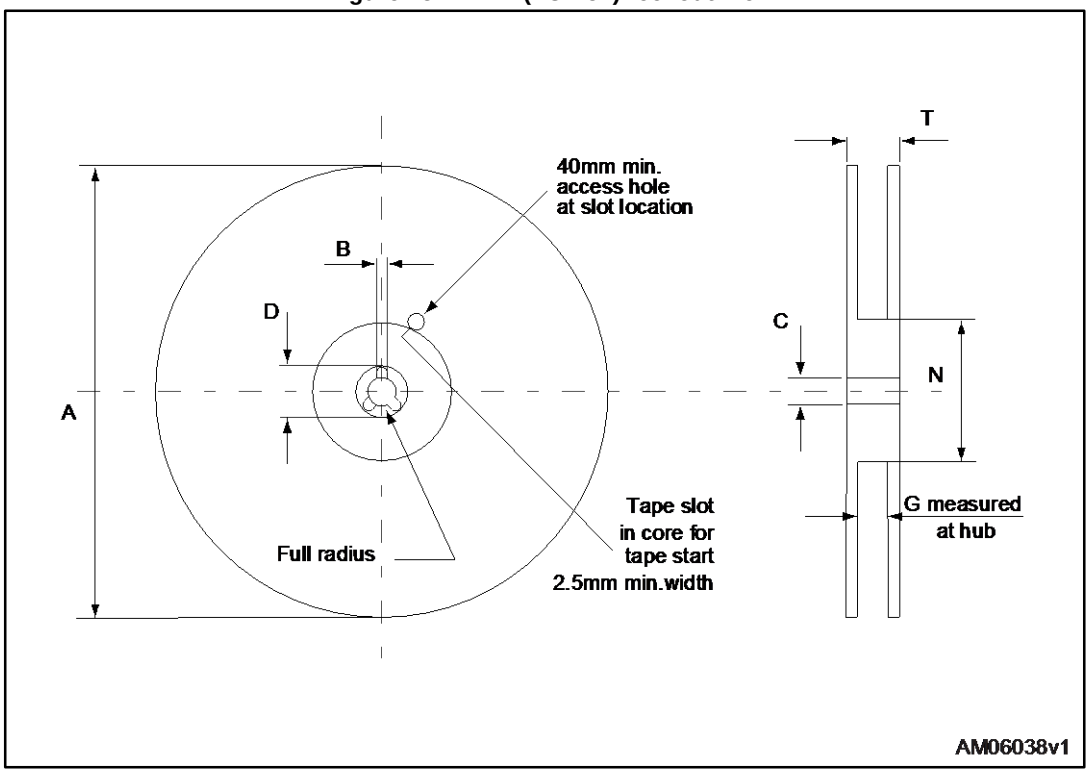


Table 10: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.3 TO-220 type A package information

Figure 26: TO-220 type A package outline

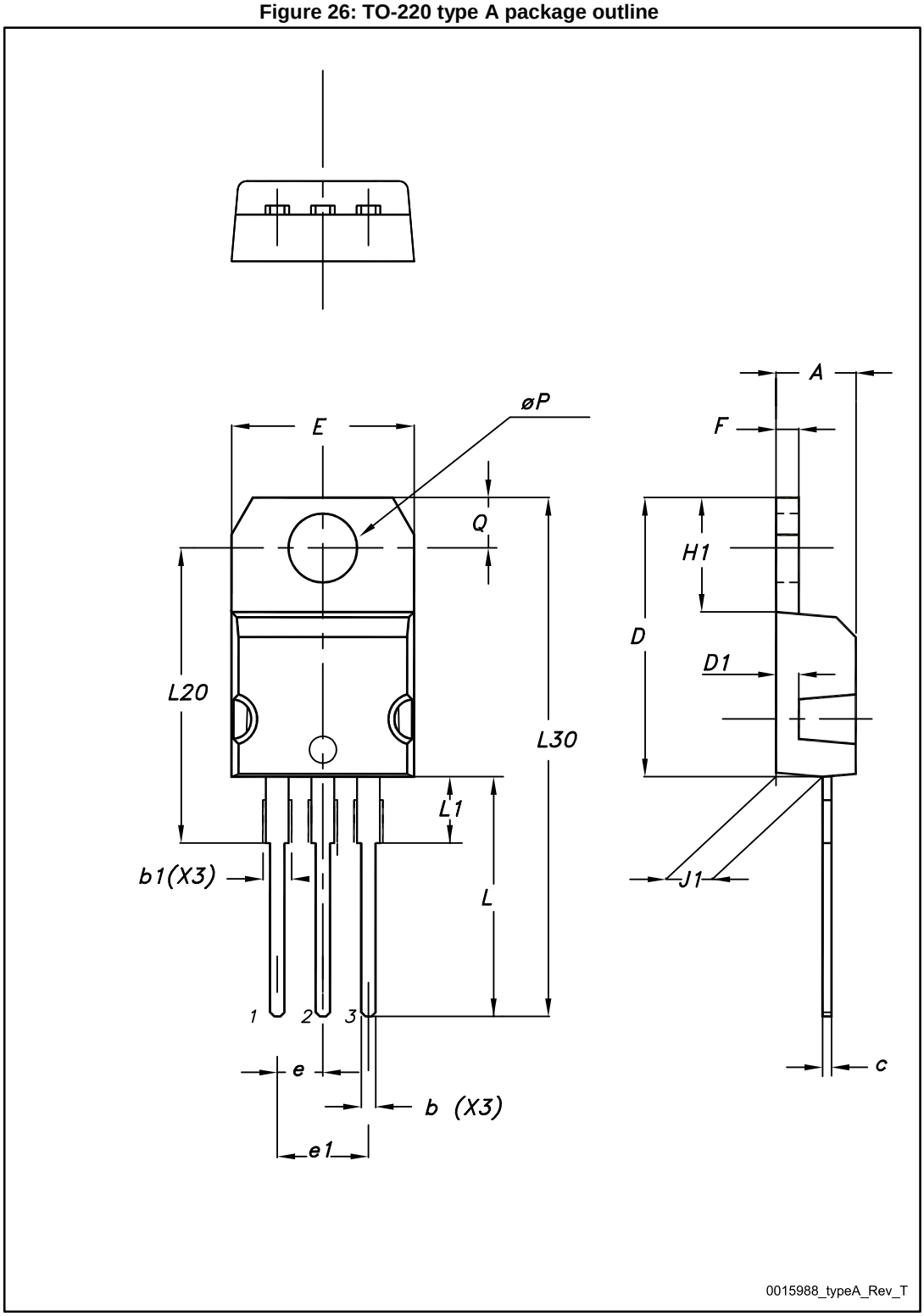


Table 11: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.4 IPAK (TO-251) Type A package information

Figure 27: IPAK (TO-251) type A package outline

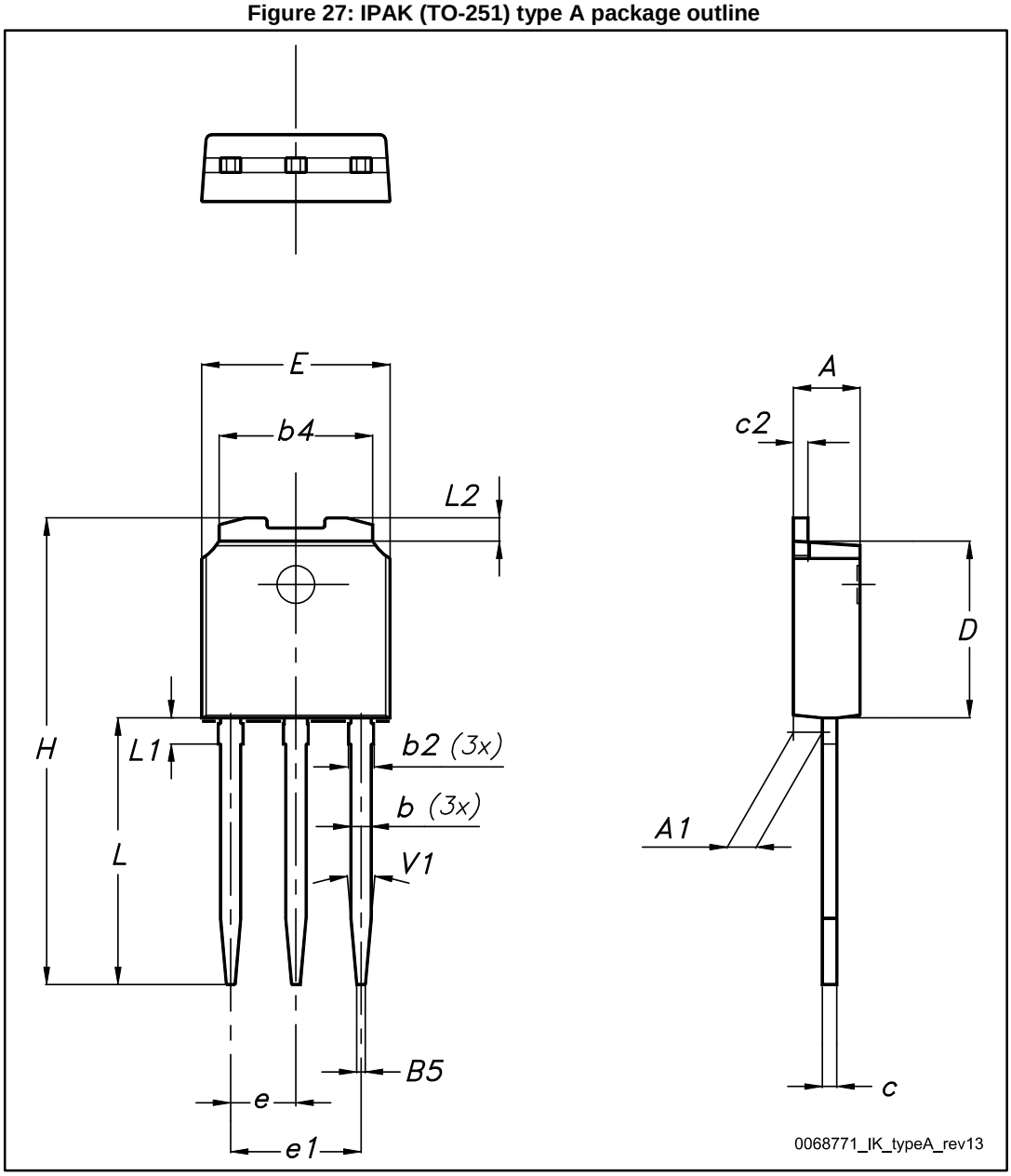


Table 12: IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.5 IPAK (TO-251) Type C package information

Figure 28: IPAK (TO-251) type C package outline

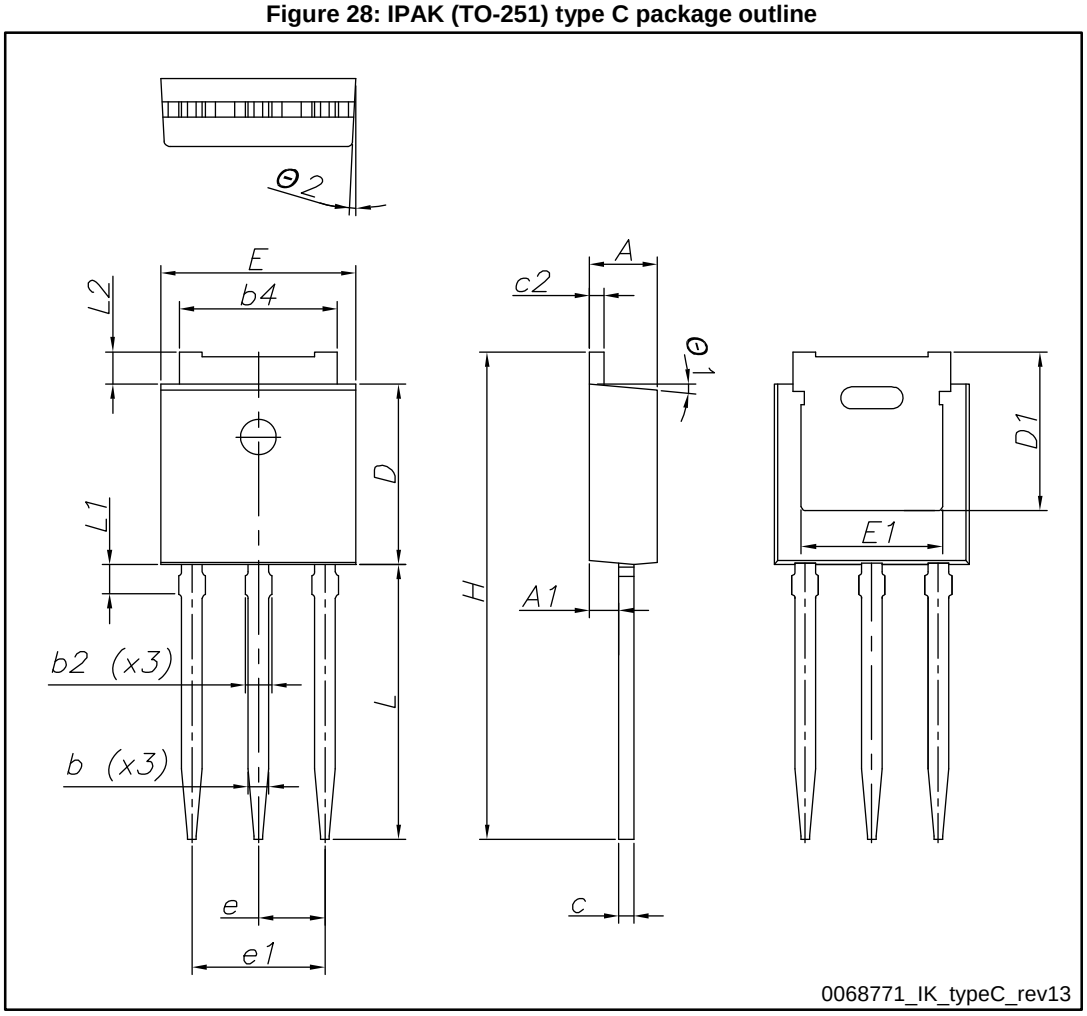


Table 13: IPAK (TO-251) type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.90	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

5 Revision history

Table 14: Document revision history

Date	Revision	Changes
16-May-2014	1	First release.
14-Aug-2015	2	Text and formatting changes throughout document. On cover page: - updated *Title*, *Features* and *Description* In section *Electrical characteristics*: - updated and renamed table *Static* (was On /off states) Updated section *Electrical characteristics (curves)* Updated and renamed section *Package information* (was Package mechanical data)
17-Aug-2015	3	Datasheet promoted from preliminary data to production data. In section *Electrical ratings*: - updated and renamed table *Absolute maximum ratings* In section *Electrical characteristics*: - updated table *Source-drain diode* In section *Electrical characteristics (curves)* - updated figure *Thermal impedance for DPAK and IPAK* Added section *IPAK (TO-251) Type C package information*
07-Sep-2015	4	Minor text and formatting changes throughout document.

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