



STS7C4F30L

N-CHANNEL 30V - 0.018Ω - 7A SO-8

P-CHANNEL 30V - 0.070Ω - 4A SO-8

STripFET™ POWER MOSFET

TYPE	V _{bss}	R _{DS(on)}	I _D
STS7C4F30L(N-Channel)	30 V	<0.022 Ω	7 A
STS7C4F30L(P-Channel)	30 V	<0.080 Ω	4 A

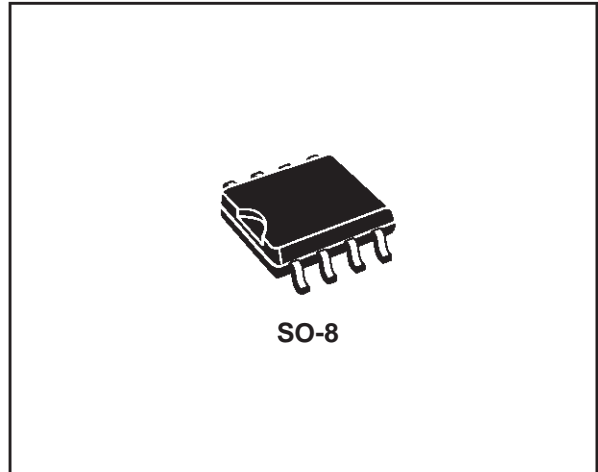
- TYPICAL R_{DS(on)} (N-Channel) = 0.018 Ω
- TYPICAL R_{DS(on)} (P-Channel) = 0.070 Ω
- 100% AVALANCHE TESTED
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

DESCRIPTION

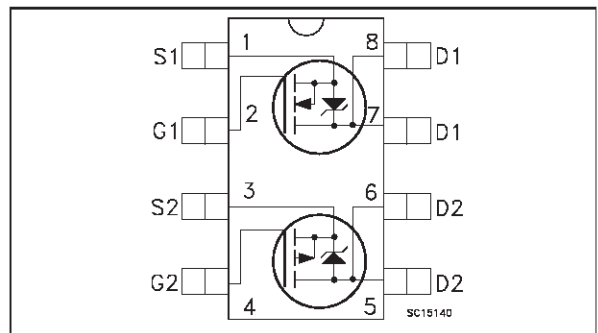
This Power MOSFET is the second generation of STMicroelectronics unique "Single Feature Size" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC/DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN CELLULAR PHONES



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	N-CHANNEL	P-CHANNEL	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30	30	V
V _{GS}	Gate- source Voltage	± 20	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C Single Operating	7	4	A
I _D	Drain Current (continuous) at T _C = 100°C Single Operating	4.4	2.5	A
I _{DM} (●)	Drain Current (pulsed)	28	16	A
P _{TOT}	Total Dissipation at T _C = 25°C Dual Operating Total Dissipation at T _C = 25°C Single Operating	2 1.6	2 1.6	W W
T _{stg}	Storage Temperature	-60 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(●) Pulse width limited by safe operating area.
Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

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THERMAL DATA

$R_{thj-amb}$	Thermal Resistance Junction-ambient	Single Operating	78	$^{\circ}\text{C}/\text{W}$
T_j	Maximum Lead Temperature For Soldering Purpose	Dual Operating	62.5	$^{\circ}\text{C}/\text{W}$
			300	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu\text{A}$ $V_{GS} = 0$	n-ch p-ch	30 30			V V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_C = 125^{\circ}\text{C}$				1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$ $V_{GS} = \pm 20 \text{ V}$	n-ch p-ch			± 100 ± 100	nA nA

ON (*)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu\text{A}$	n-ch p-ch	1 1	1.6 1.6	2.5 2.5	V V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 \text{ V}$ $I_D = 4 \text{ A}$ $V_{GS} = 10 \text{ V}$ $I_D = 2 \text{ A}$ $V_{GS} = 4.5 \text{ V}$ $I_D = 4 \text{ A}$ $V_{GS} = 4.5 \text{ V}$ $I_D = 2 \text{ A}$	n-ch p-ch n-ch p-ch		0.018 0.070 0.021 0.085	0.022 0.080 0.026 0.10	Ω Ω Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$g_{fs}^{(*)}$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 3.5 \text{ V}$ $V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 2 \text{ V}$	n-ch p-ch		10 10		S S
C_{iss}	Input Capacitance		n-ch p-ch		1050 1350		pF pF
C_{oss}	Output Capacitance Reverse Transfer	$V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0 \text{ A}$	n-ch p-ch		250 490		pF pF
C_{rss}	Capacitances		n-ch p-ch		85 130		pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	N-CHANNEL $V_{DD} = 15\text{ V}$ $I_D = 4\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$	n-ch p-ch		22 25		ns ns
t_r	Rise Time	P-CHANNEL $V_{DD} = 15\text{ V}$ $I_D = 2\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig.3)	n-ch p-ch		60 35		ns ns
Q_g	Total Gate Charge	N-CHANNEL $V_{DD}=24\text{V}$ $I_D=7\text{A}$ $V_{GS}=5\text{V}$	n-ch p-ch		17.5 12.5	23 16	nC nC
Q_{gs}	Gate-Source Charge	P-CHANNEL $V_{DD}=24\text{V}$ $I_D=4\text{A}$ $V_{GS}=5\text{V}$ (see test circuit, Figure 5)	n-ch p-ch		4 5		nC nC
Q_{gd}	Gate-Drain Charge		n-ch p-ch		7 3		nC nC

SWITCHING OFF

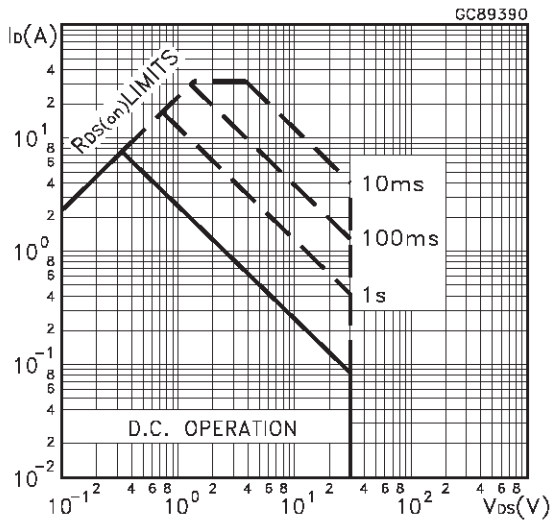
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	N-CHANNEL $V_{DD} = 15\text{ V}$ $I_D = 4\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$	n-ch p-ch		42 125		ns ns
t_f	Fall Time	P-CHANNEL $V_{DD} = 15\text{ V}$ $I_D = 2\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig.3)	n-ch p-ch		10 35		ns ns

SOURCE DRAIN DIODE

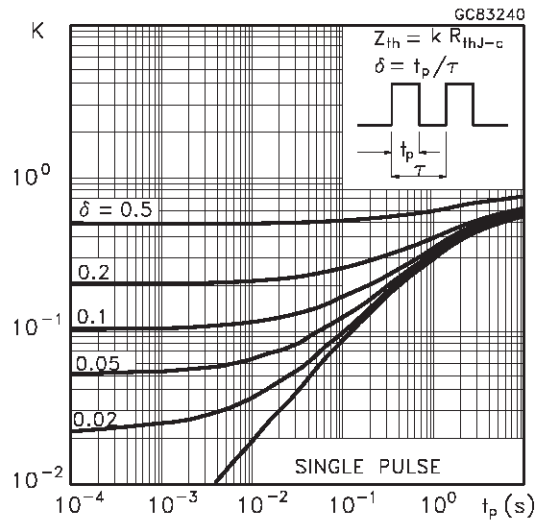
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current		n-ch p-ch			7 4	ns ns
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)		n-ch p-ch			28 16	ns ns
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 4\text{ A}$, $V_{GS} = 0$	n-ch p-ch			1.2 1.2	V V
t_{rr}	Reverse Recovery Time	N-CHANNEL $I_{SD} = 7\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$	n-ch p-ch		50 45		ns
Q_{rr}	Reverse Recovery Charge	P-CHANNEL $I_{SD} = 4\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, Figure 5)	n-ch p-ch		40 36		nC
I_{RRM}	Reverse Recovery Current		n-ch p-ch		1.6 1.6		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 (•) Pulse width limited by safe operating area.

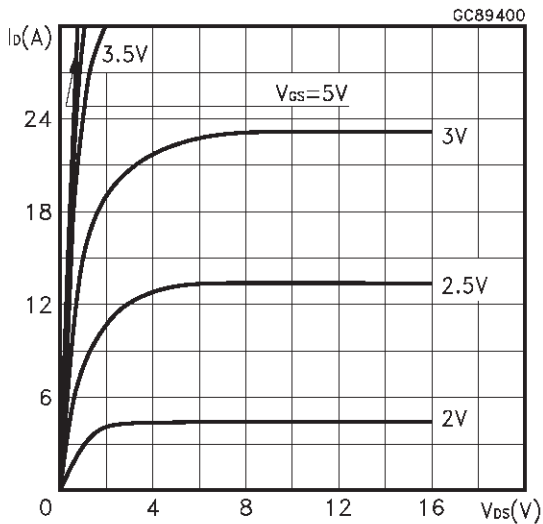
Safe Operating Area n-ch



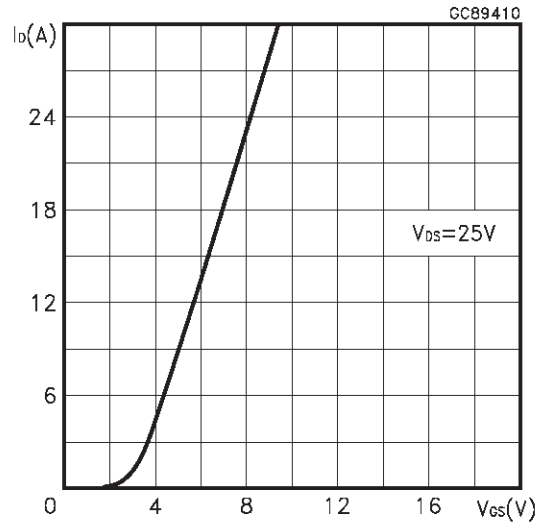
Thermal Impedance n-ch



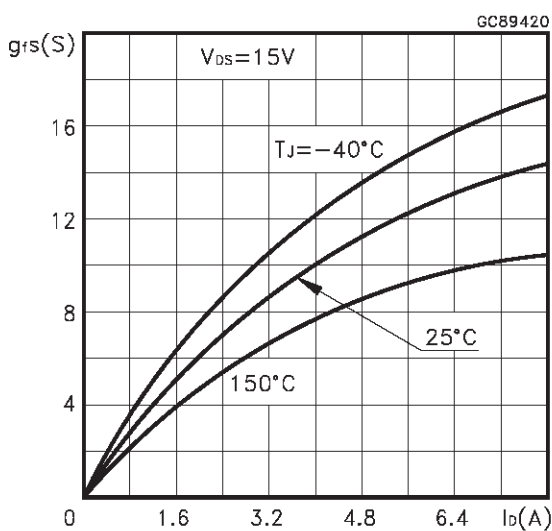
Output Characteristics n-ch



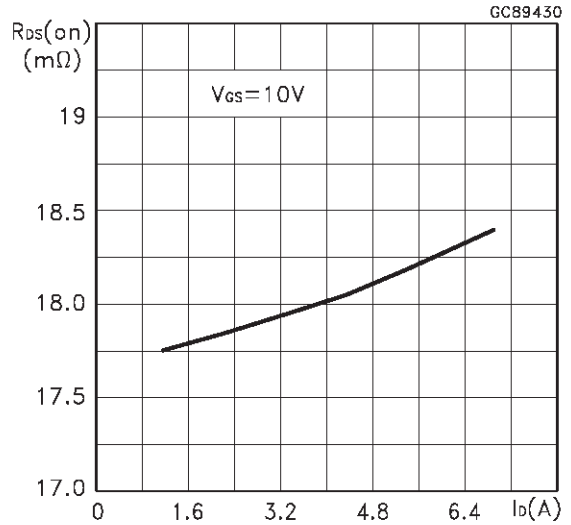
Transfer Characteristics n-ch



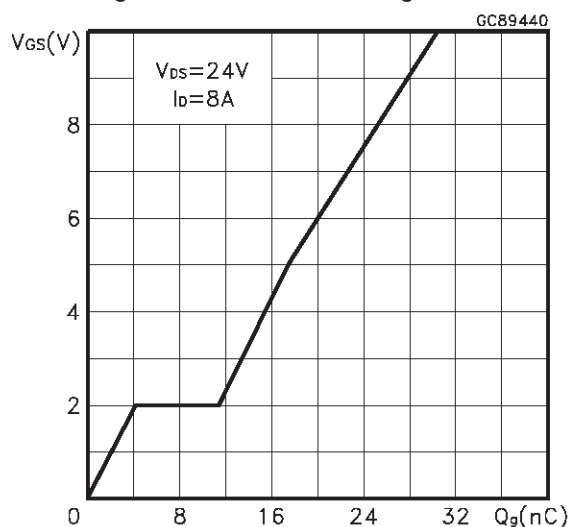
Transconductance n-ch



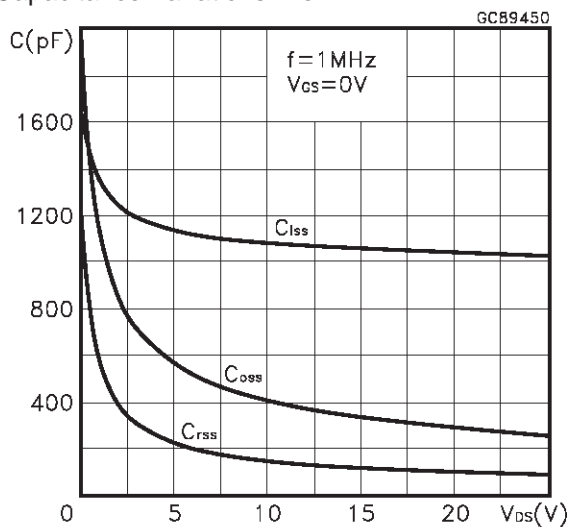
Static Drain-source On Resistance n-ch



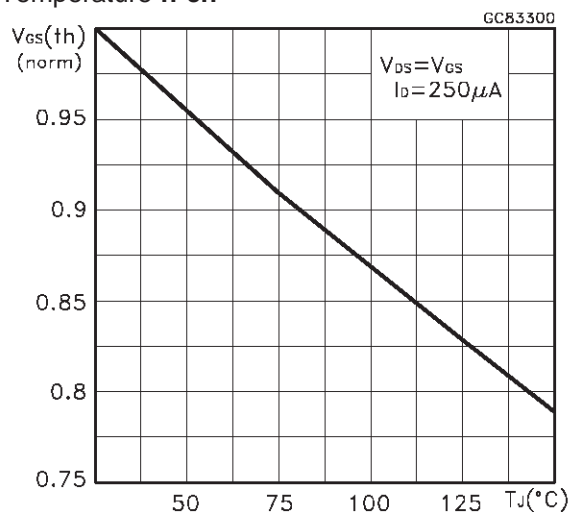
Gate Charge vs Gate-source Voltage n-ch



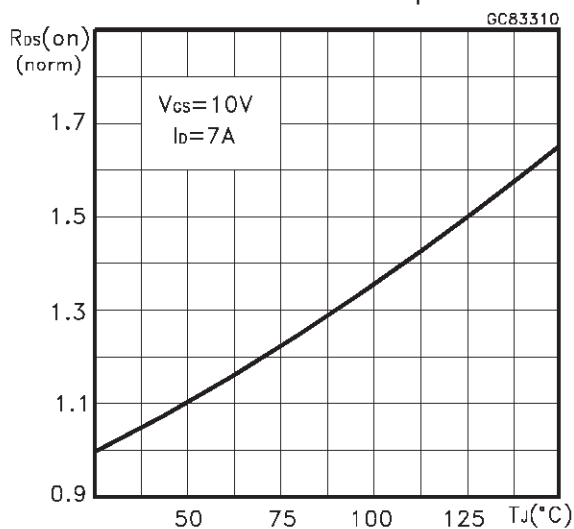
Capacitance Variations n-ch



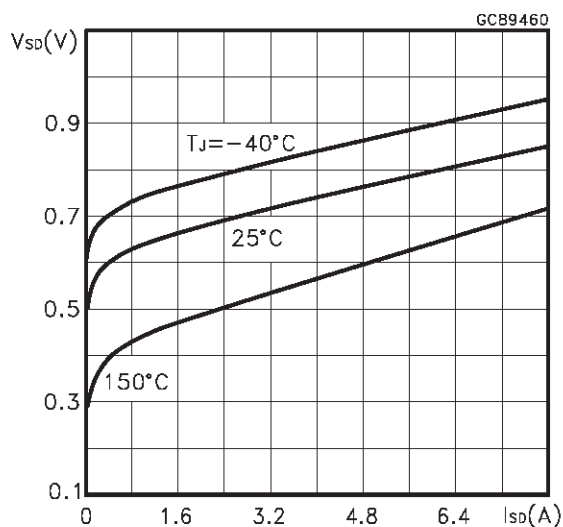
Normalized Gate Threshold Voltage vs Temperature n-ch



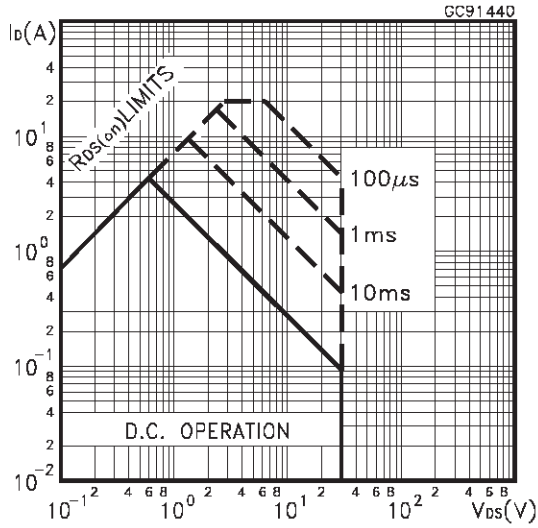
Normalized On Resistance vs Temperature n-ch



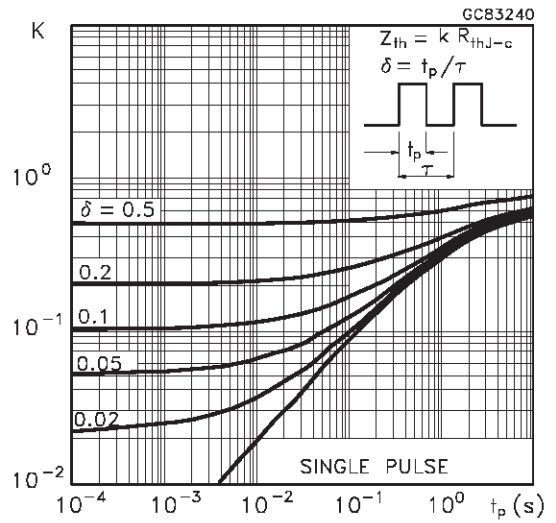
Source-drain Diode Forward Characteristics n-ch



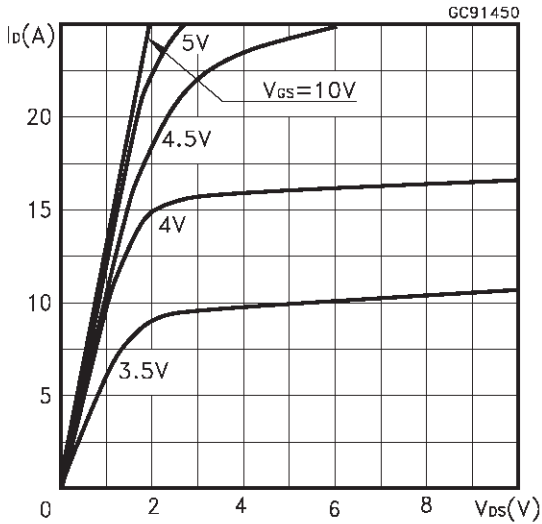
Safe Operating Area p-ch



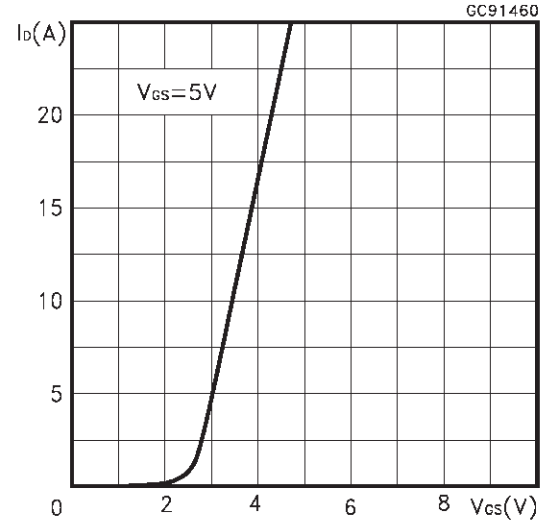
Thermal Impedance p-ch



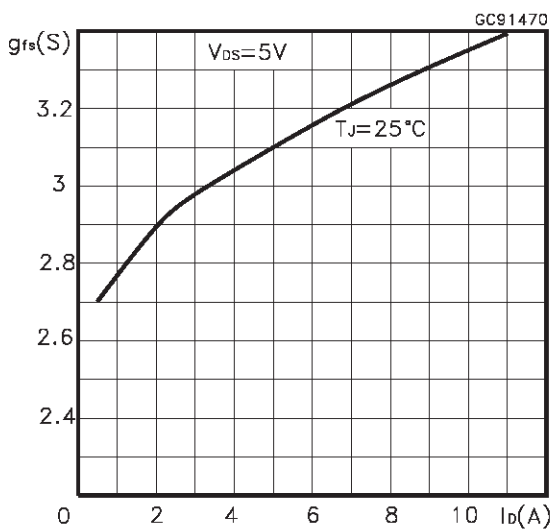
Output Characteristics p-ch



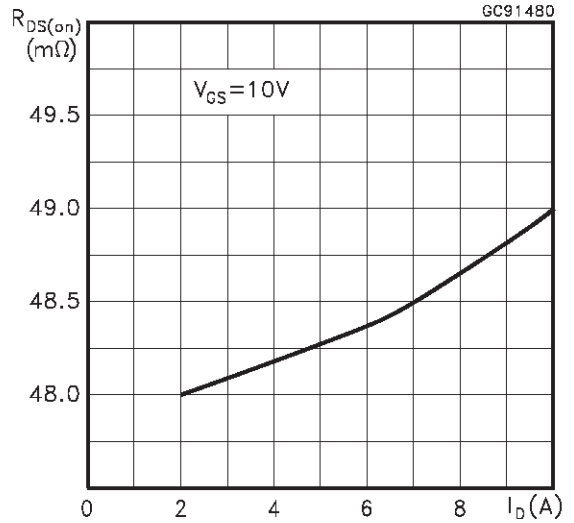
Transfer Characteristics p-ch



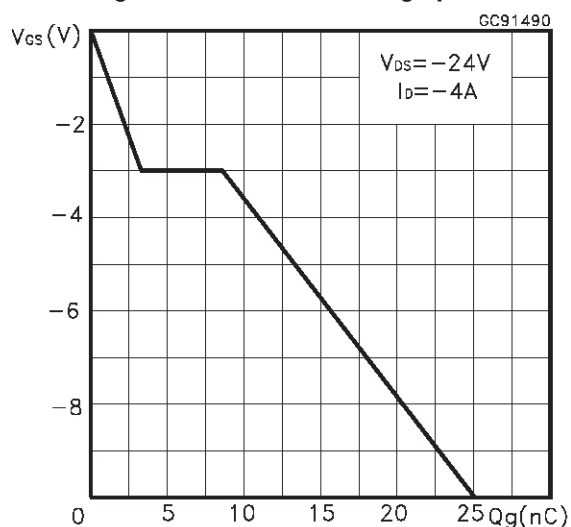
Transconductance p-ch



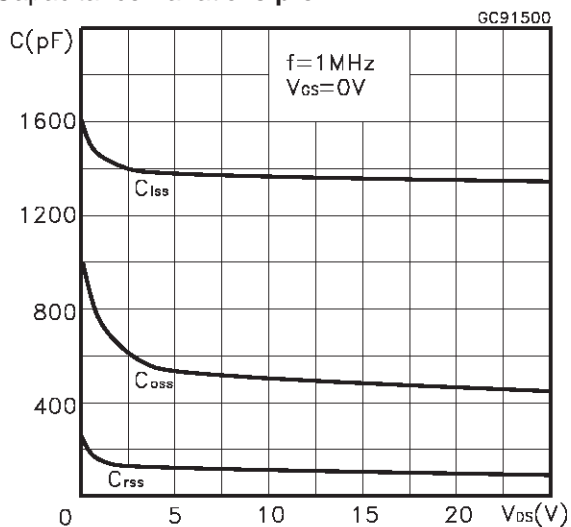
Static Drain-source On Resistance p-ch



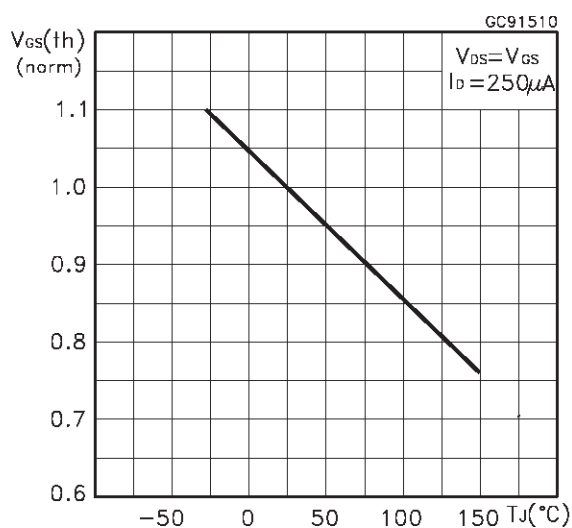
Gate Charge vs Gate-source Voltage **p-ch**



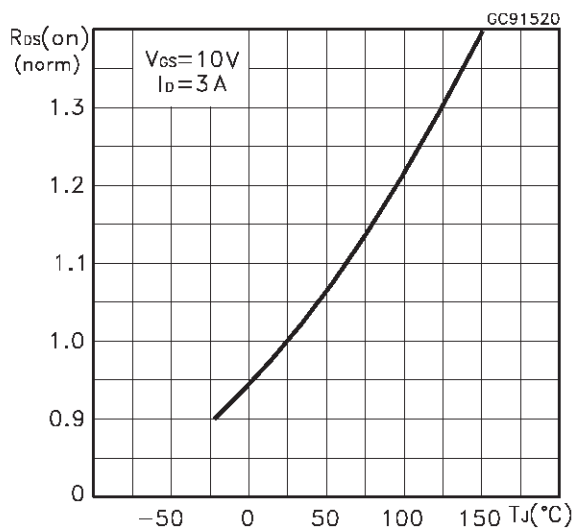
Capacitance Variations **p-ch**



Normalized Gate Threshold voltage vs Temperature **p-ch**



Static Drain-source On Resistance **p-ch**



Source-drain Diode Forward Characteristics **p-ch**

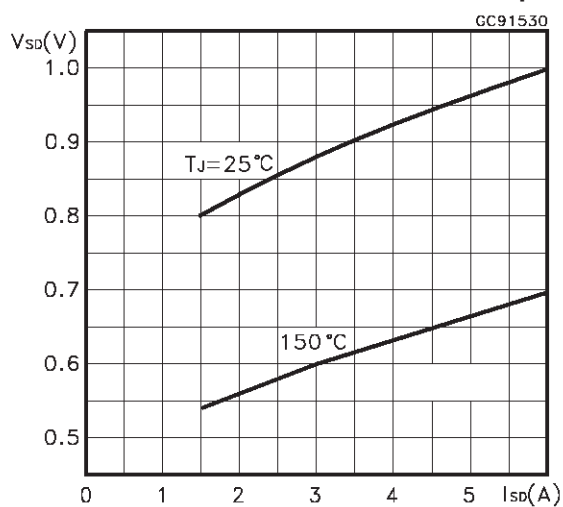


Fig. 1: Unclamped Inductive Load Test Circuit

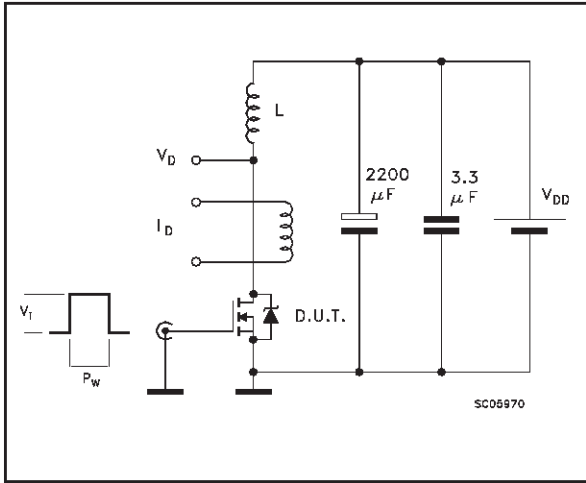


Fig. 2: Unclamped Inductive Waveform

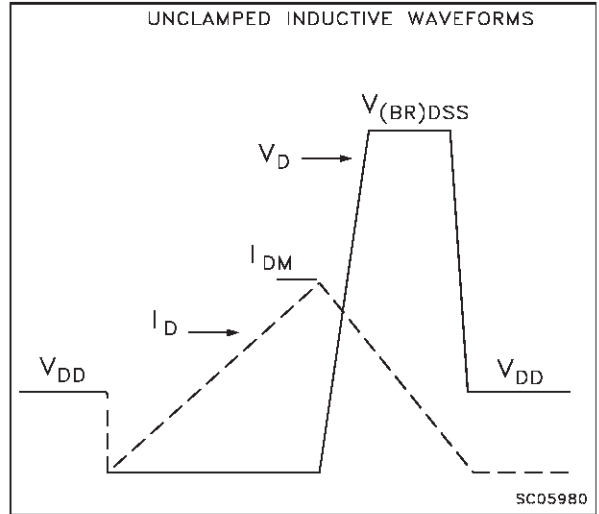


Fig. 3: Switching Times Test Circuits For Resistive Load

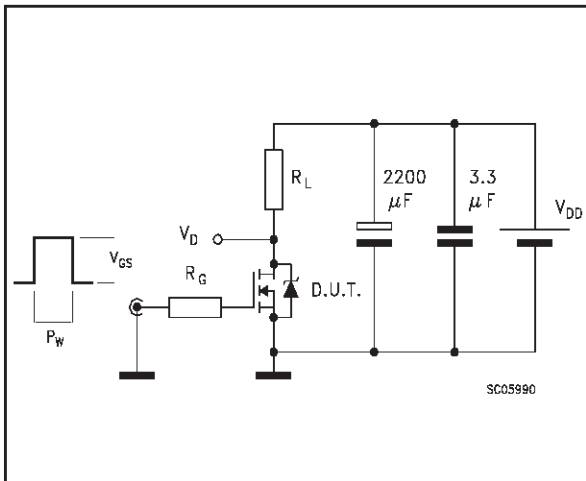


Fig. 4: Gate Charge test Circuit

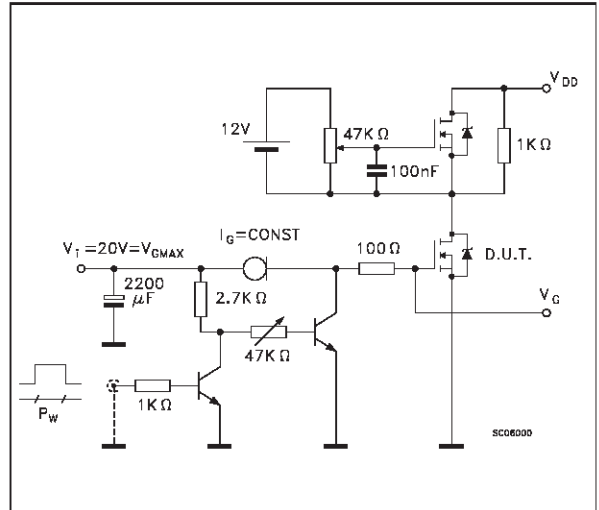
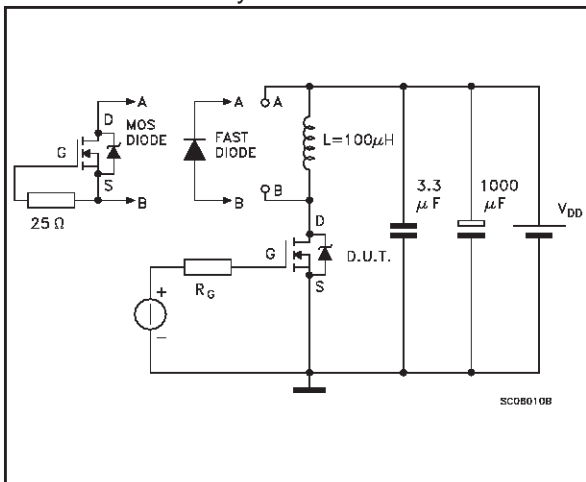
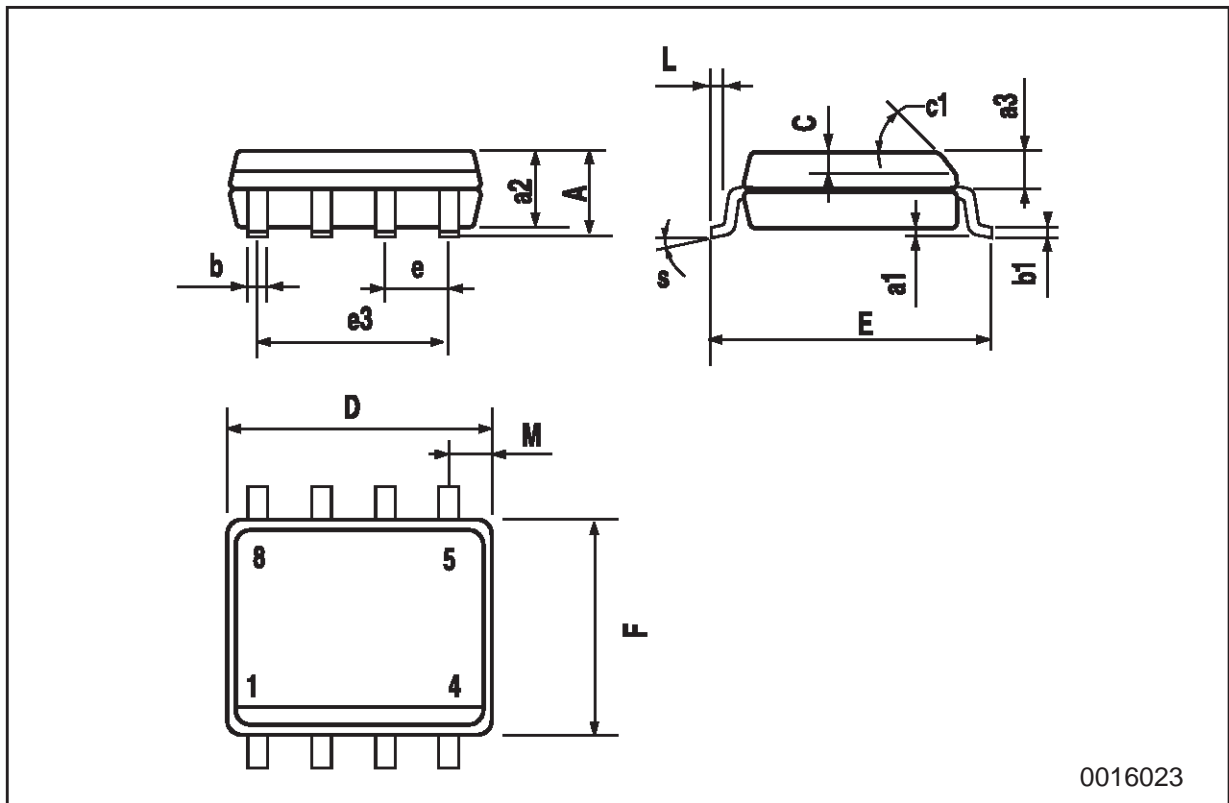


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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