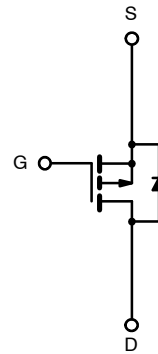
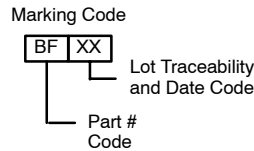
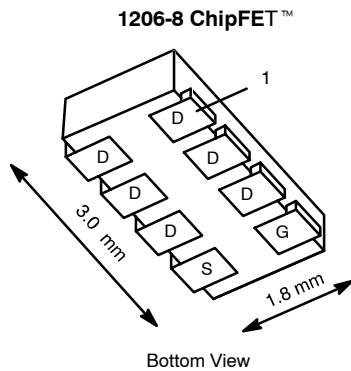


P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-12	0.031 @ $V_{GS} = -4.5$ V	-7.6
	0.041 @ $V_{GS} = -2.5$ V	-6.6
	0.054 @ $V_{GS} = -1.8$ V	-5.8

TrenchFET[®]
Power MOSFETs
1.8-V Rated



P-Channel MOSFET

Ordering Information: Si5475DC-T1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	5 secs	Steady State	Unit
Drain-Source Voltage	V_{DS}	-12		V
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	-7.6	-5.5	A
	$T_A = 85^\circ\text{C}$	-3.5	-3.9	
Pulsed Drain Current	I_{DM}	± 20		A
Continuous Source Current ^a	I_S	-2.1	-1.1	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	2.5	1.3	W
	$T_A = 85^\circ\text{C}$	1.3	0.7	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{b, c}		260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 5$ sec	40	50	$^\circ\text{C/W}$
		Steady State	80	95	
Maximum Junction-to-Foot (Drain)	R_{thJF}	15	20		

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

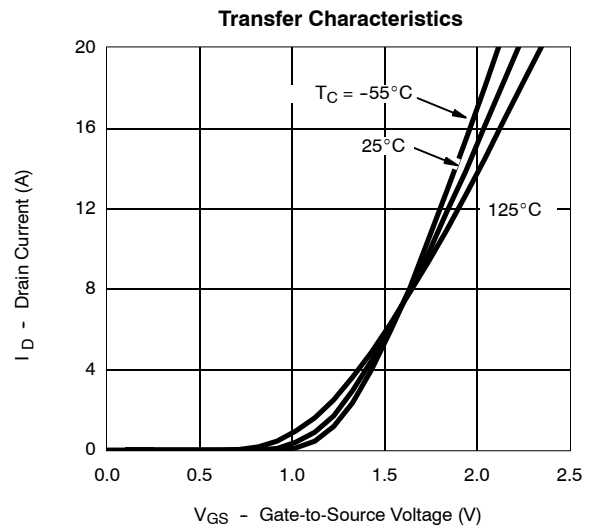
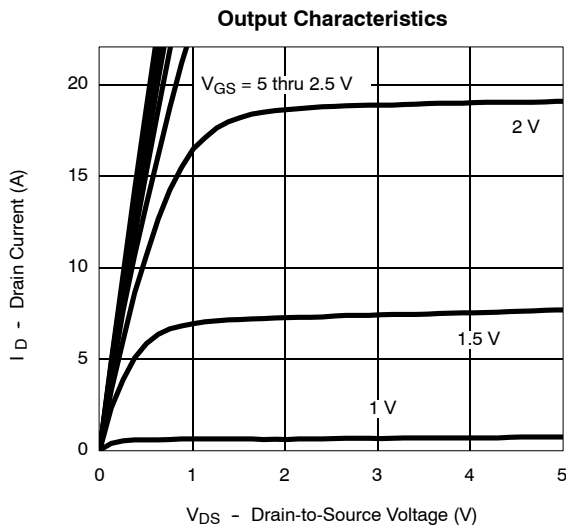


SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -1 mA	-0.45			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -9.6 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -9.6 V, V _{GS} = 0 V, T _J = 85 °C			-5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-20			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -5.5 A		0.027	0.031	Ω
		V _{GS} = -2.5 V, I _D = -4.8 A		0.035	0.041	
		V _{GS} = -1.8 V, I _D = -2 A		0.045	0.054	
Forward Transconductance ^a	g _{fs}	V _{DS} = -5 V, I _D = -5.2 A		19		S
Diode Forward Voltage ^a	V _{SD}	I _S = -1.1 A, V _{GS} = 0 V		-0.7	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -6 V, V _{GS} = -4.5 V, I _D = -5.5 A		19	29	nC
Gate-Source Charge	Q _{gs}			3.9		
Gate-Drain Charge	Q _{gd}			3.6		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -6 V, R _L = 6 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω		15	25	ns
Rise Time	t _r			20	30	
Turn-Off Delay Time	t _{d(off)}			122	180	
Fall Time	t _f			80	120	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = -1.1 A, di/dt = 100 A/μs		40	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

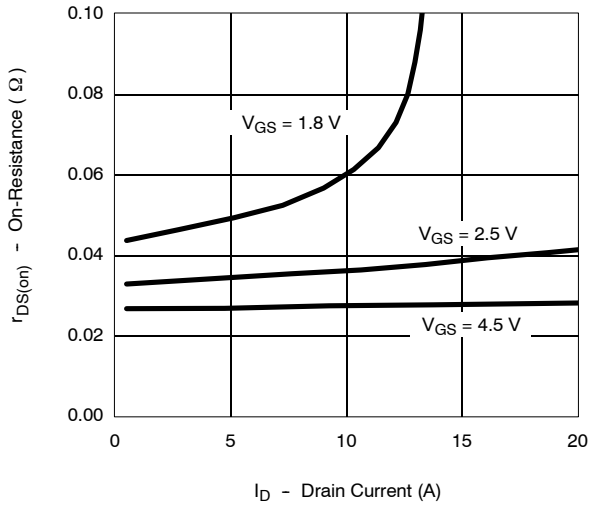
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



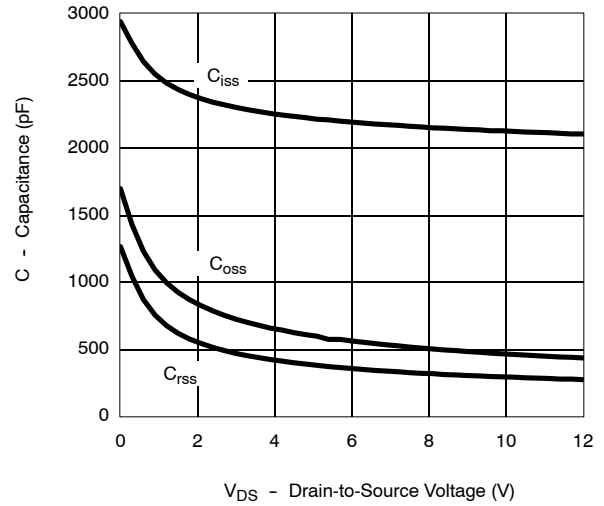


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

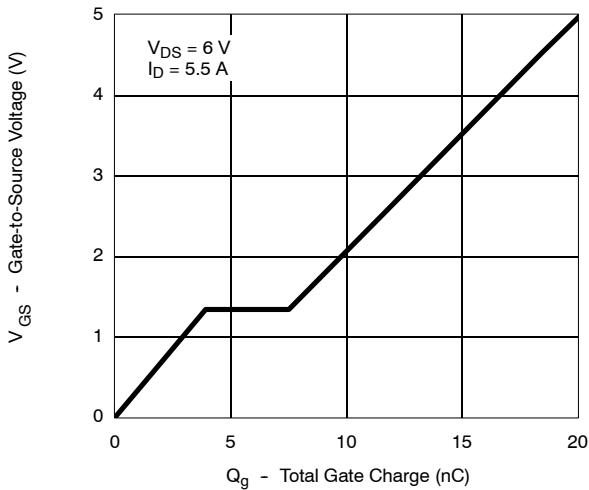
On-Resistance vs. Drain Current



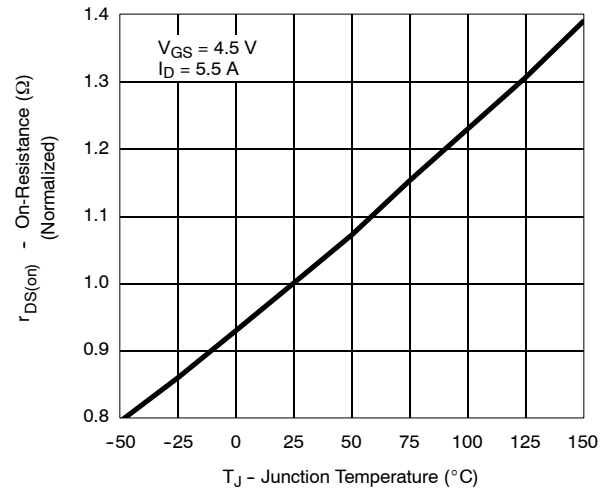
Capacitance



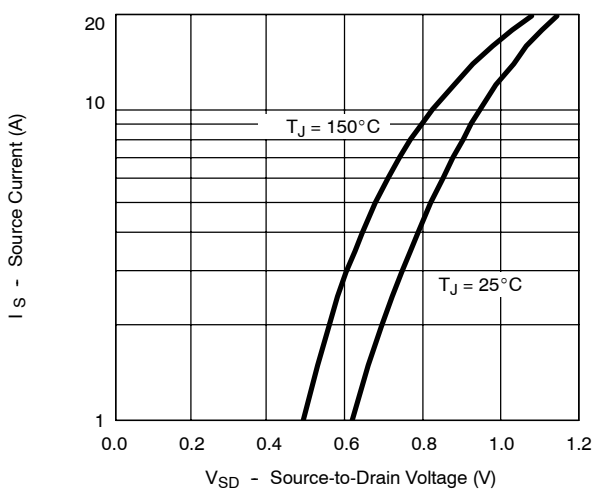
Gate Charge



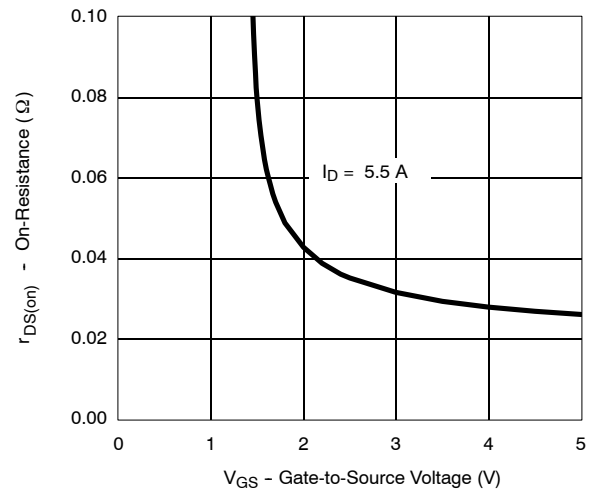
On-Resistance vs. Junction Temperature



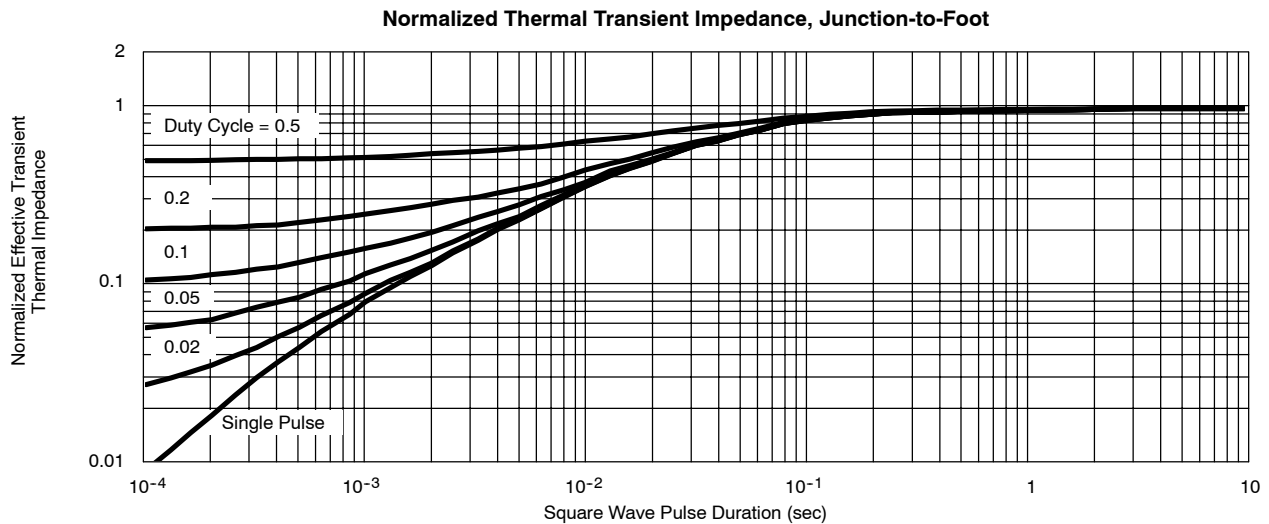
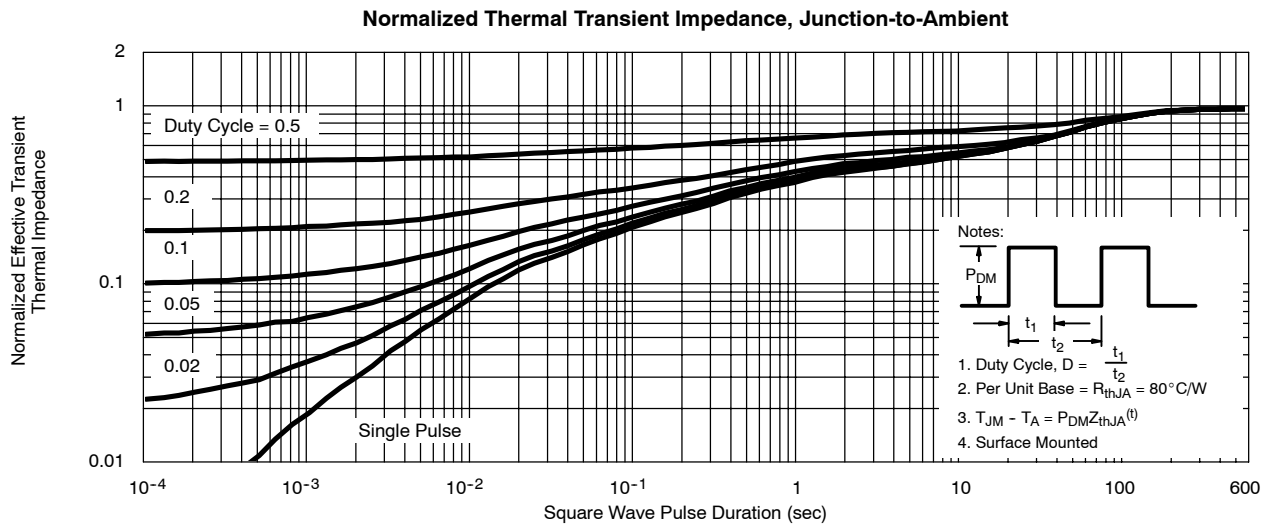
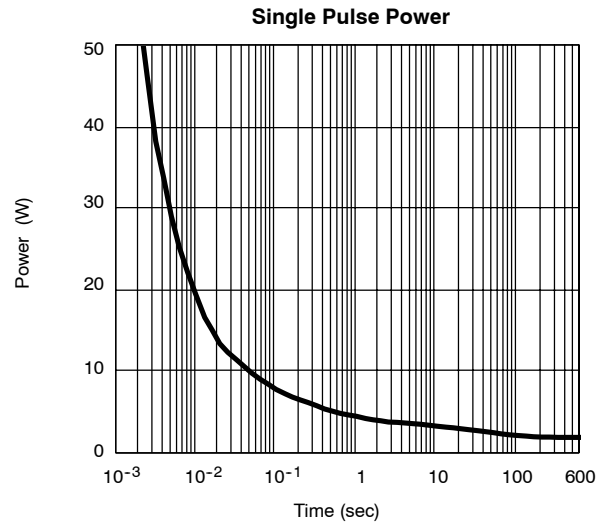
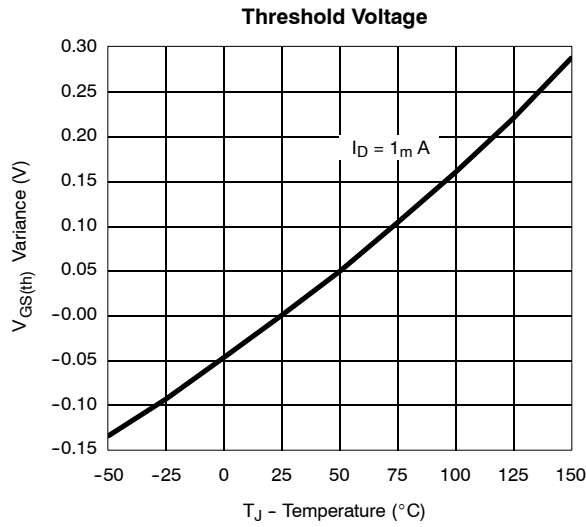
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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