ap	plication	UC1861-1868
	INFO	UC2861-2868
	available	UC3861-3868

Resonant-Mode Power Supply Controllers

FEATURES

- Controls Zero Current Switched (ZCS) or Zero Voltage Switched (ZVS) Quasi-Resonant Converters
- Zero-Crossing Terminated One-Shot
 Timer
- Precision 1%, Soft-Started 5V Reference
- Programmable Restart Delay Following Fault
- Voltage-Controlled Oscillator (VCO) with Programmable Minimum and Maximum Frequencies from 10kHz to 1MHz
- Low Start-Up Current (150µA typical)
- Dual 1 Amp Peak FET Drivers
- UVLO Option for Off-Line or DC/DC Applications

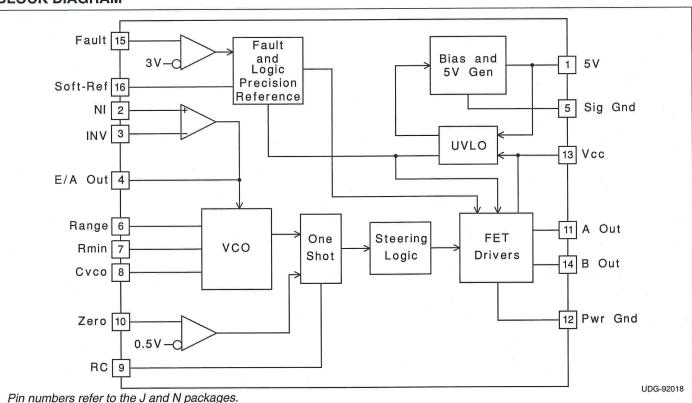
DESCRIPTION

The UC1861-1868 family of ICs is optimized for the control of Zero Current Switched and Zero Voltage Switched quasi-resonant converters. Differences between members of this device family result from the various combinations of UVLO thresholds and output options. Additionally, the one-shot pulse steering logic is configured to program either on-time for ZCS systems (UC1865-1868), or off-time for ZVS applications (UC1861-1864).

The primary control blocks implemented include an error amplifier to compensate the overall system loop and to drive a voltage controlled oscillator (VCO), featuring programmable minimum and maximum frequencies. Triggered by the VCO, the one-shot generates pulses of a programmed maximum width, which can be modulated by the Zero Detection comparator. This circuit facilitates "true" zero current or voltage switching over various line, load, and temperature changes, and is also able to accommodate the resonant components' initial tolerances.

Under-Voltage Lockout is incorporated to facilitate safe starts upon power-up. The supply current during the under-voltage lockout period is typically less than 150μ A, and the outputs are actively forced to the low state. (continued)

Device	1861	1862	1863	1864	1865	1866	1867	1868
UVLO	16.5/10.5	16.5/10.5	8/7	8/7	16.5/10.5	16.5/10.5	8/7	8/7
Outputs	Alternating	Parallel	Alternating	Parallel	Alternating	Parallel	Alternating	Parallel
"Fixed"	Off Time	Off Time	Off Time	Off Time	On Time	On Time	On Time	On Time



BLOCK DIAGRAM

SLUS289B - OCTOBER 1998 - REVISED SEPTEMBER 2007

DESCRIPTION (cont.)

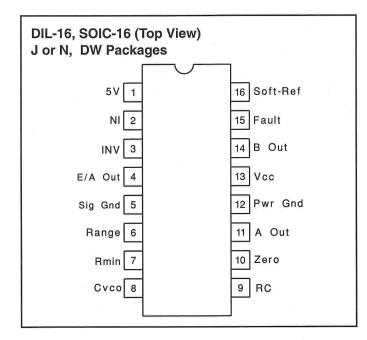
UVLO thresholds for the UC1861/62/65/66 are 16.5V (ON) and 10.5V (OFF), whereas the UC1863/64/67/68 thresholds are 8V (ON) and 7V (OFF). After V_{CC} exceeds the UVLO threshold, a 5V generator is enabled which provides bias for the internal circuits and up to 10mA for external usage.

A Fault comparator serves to detect fault conditions and set a latch while forcing the output drivers low. The Soft-Ref pin serves three functions: providing soft start, restart

ABSOLUTE MAXIMUM RATINGS

V _{CC}
Output Current
Source or Sink (Pins 11 & 14) 0.5A
DC Pulse (0.5µs) 1.5A
Power Ground Voltage ±0.2V
Inputs (Pins 2, 3, 10, & 15)
Error Amp Output Current ±2mA
Power Dissipation1W
Junction Temperature (Operating)
Lead Temperature (Soldering, 10 seconds)

All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the J and N packages. Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.



delay, and the internal system reference.

Each device features dual 1 Amp peak totem pole output drivers for direct interface to power MOSFETS. The outputs are programmed to alternate in the UC1861/63/65/67 devices. The UC1862/64/66/68 outputs operate in unison allowing a 2 Amp peak current.

CONNNECTION DIAGRAMS

PLCC-20 & LCC-20 (Top Q & L Package	View)	
9	PACKAGE PIN F	UNCTION
	FUNCTION	PIN
	Soft Ref	1
	5V	2
the second se	NI	3
	INV	4
3 2 1 20 19	E/A Out	5
	Sig Gnd	6
[4 18]	Range	7
[5 17]	RMIN	8
6 16	Cvco	9
1-	RC	10
[7 15]	Zero	11
[8 14]	NC	12
9 10 11 12 13	NC	13
	A Out	14
	Pwr Gnd	15
	Pwr Gnd	16
	Vcc	17
	B Out	18
	NC	19
	Fault	20
1		

ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications apply for -55°C≤Ta≤125°C for the UC186x, -25°C≤Ta≤85°C for the UC286x, and 0°C≤Ta≤70°C for the UC386x, Vcc=12V, Cvco=1nF, Range=7.15k, RMIN=86.6k, C=200pF, R=4.02k, and Csr=0.1µF. Ta=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
5V Generator					
Output Voltage	$12V \le Vcc \le 20V, -10mA \le Io \le 0mA$	4.8	5.0	5.2	V
Short Circuit Current	Vo = 0V	-150		-15	mA
Soft-Reference					
Restart Delay Current	V = 2V	10	20	35	μA
Soft Start Current	V = 2V	-650	-500	-350	μΑ
Reference Voltage	$T_J = 25^{\circ}C, IO = 0A$	4.95	5.00	5.05	V
	$12V \le Vcc \le 20V$, $-200\mu A \le Io \le 200\mu A$	4.85		5.15	V
Line Regulation	$12V \le Vcc \le 20V$		2	20	mV
Load Regulation	$-200\mu A \le IO \le 200\mu A$	1	10	30	mV
Error Amplifier (Note 3)					
Input Offset Voltage	VCM = 5V, Vo = 2V, IO = 0A	-10		10	mV
Input Bias Current	VCM = 0V	-2.0	-0.3	1	μΑ
Voltage Gain	$Vcm = 5V, 0.5V \le Vo \le 3.7V, Io = 0A$	70	100		dB
Power Supply Rejection Ratio	$Vcm = 5V, Vo = 2V, 12V \le Vcc \le 20V$	70	100	1	dB
Error Amplifier (Note 3) (cont.)					
Common Mode Rejection Ratio	$0V \le Vcm \le 6V, Vo = 2V$	65	100		dB
Vout Low	$V_{ID} = -100 \text{mV}, IO = 200 \mu \text{A}$		0.17	0.25	V
Vout High	$V_{ID} = 100 \text{mV}, IO = -200 \mu \text{A}$	3.9	4.2	н т.	V
Unity Gain Bandwidth	(Note 4)	0.5	0.8		MHz
Voltage Controlled Oscillator					
Maximum Frequency	VID (Error Amp) = 100mV, TJ = 25°C	450	500	550	kHz
	VID (Error Amp) = 100mV	425	· · ·	575	kHz
Minimum Frequency	VID (Error Amp) = -100 mV, TJ = 25° C	45	50	55	kHz
	VID (Error Amp) = -100mV	42		58	kHz
One Shot					т. п.
Zero Comparator Vth		0.45	0.50	0.55	V
Propagation Delay	(Note 4)	ч.	120	200	ns
Maximum Pulse Width	VZERO = 1V	850	1000	1150	ns
Maximum to Minimum Pulse	VZERO = 0V UCx861 – UCx864	2.5	4	5.5	
Width Ratio	VZERO = 0V UCx865 – UCx868. –55°C to +85°C	4	5.5	7	
	VZERO = 0V UCx865 – UCx868, +125°C	3.8	5.5	7	
Output Stage			1		1
Rise and Fall Time	CLOAD = 1nF (Note 4)		25	45	ns
Output Low Saturation	Io = 20mA		0.2	0.5	V
	Io = 200mA		0.5	2.2	V
Output High Saturation	IO = -200 mA, down from Vcc		1.7	2.5	V
UVLO Low Saturation	IO = 20mA		0.8	1.5	V
Fault Comparator					
Fault Comparator Vth		2.85	3.00	3.15	V
Delay to Output	(Note 4) (Note 5)		100	200	ns

ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications apply for –55°C≤TA≤125°C for the UC186x, –25°C≤TA≤85°C for the UC286x, and 0°C≤TA≤70°C for the UC386x, Vcc=12V, Cvco=1nF, Range=7.15k, RMIN=86.6k, C=200pF, R=4.02k, and Csr=0.1µF. TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UVLO					1
Vcc Turn-on Threshold	UCx861, UCx862, UCx865, UCx866	15	16.5	18	V
	UCx863, UCx864, UCx867, UCx868	7	8.0	9	V
Vcc Turn-off Threshold	UCx861, UCx862, UCx865, UCx866	9.5	10.5	11.5	V
	UCx863, UCx864, UCx867, UCx868	6	7.0	8	V
Icc Start	Vcc = Vcc(on) - 0.3V		150	300	μΑ
Icc Run	VID = 100mV		25	32	mA

Note 1: Currents are defined as positive into the pin.

Note 2: Pulse measurement techniques are used to insure that TJ = TA.

Note 3: VID = V(NI) - V(INV).

Note 4: This parameter is not 100% tested in production but guaranteed by design.

Note 5: Vi = 0 to 4V tr(Vi) 10ns tpd = t(Vo = 6V) - t(Vi = 3V)

APPLICATION INFORMATION

UVLO & 5V GENERATOR (See Figure 1): When power is applied to the chip and Vcc is less than the upper UVLO threshold, Icc will be less than 300μ A, the 5V generator will be off, and the outputs will be actively held low.

When Vcc exceeds the upper UVLO threshold, the 5V generator turns on. Until the 5V pin exceeds 4.9V, the outputs will still remain low.

The 5V pin should be bypassed to signal ground with a 0.1μ F capacitor. The capacitor should have low equivalent series resistance and inductance.

FAULT AND SOFT-REFERENCE (See Figure 1): The Soft-Ref pin serves three functions: system reference, restart delay, and soft-start. Designed to source or sink 200 μ A, this pin should be used as the input reference for the error amplifier circuit. This pin requires a bypass capacitor of at least 0.1 μ F. This yields a minimum soft-start time of 1ms.

Under-Voltage Lockout sets both the fault and restart delay latches. This holds the outputs low and discharges the Soft-Ref pin. After UVLO, the fault latch is reset by the low voltage on the Soft-Ref pin. The reset fault latch resets the delay latch and Soft-Ref charges via the 0.5mA current source. The fault pin is input to a high speed comparator with a threshold of 3V. In the event of a detected fault, the fault latch is set and the outputs are driven low. If Soft-Ref is above 4V, the delay latch is set. Restart delay is timed as Soft-Ref is discharged by 20μ A. When Soft-Ref is fully discharged, the fault latch is reset if the fault input signal is low. The Fault pin can be used as a system shutdown pin.

If a fault is detected during soft-start, the fault latch is set and the outputs are driven low. The delay latch will remain reset until Soft-Ref charges to 4V. This sets the delay latch, and restart delay is timed. Note that restart delay for a single fault event is longer than for recurring faults since Soft-Ref must be discharged from 5V instead of 4V.

The restart delay to soft-start time ratio is 24:1 for a fault occurring during normal operation and 19:1 for faults occurring during soft-start. Shorter ratios can be programmed down to a limit of approximately 3:1 by the addition of a $20k\Omega$ or larger resistor from Soft-Ref to ground.

A 100k Ω resistor from Soft-Ref to 5V will have the effect of permanent shut down after a fault since the internal 20 μ A current source can't pull Soft-Ref low. This feature can be used to require recycling Vcc after a fault. Care must be taken to insure Soft-Ref is indeed low at start up, or the fault latch will never be reset.

APPLICATION INFORMATION

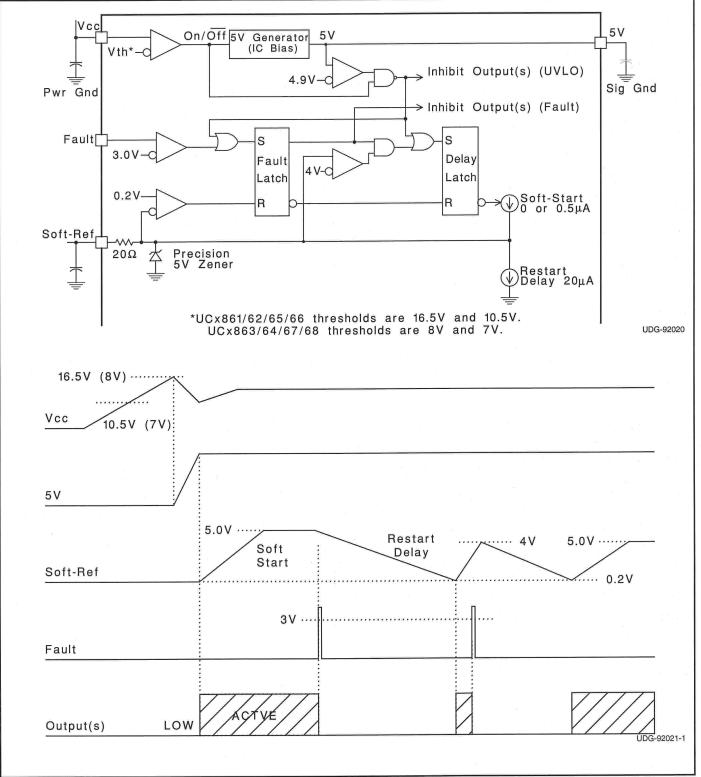


Figure 1. UVLO, 5V, fault and soft-ref.

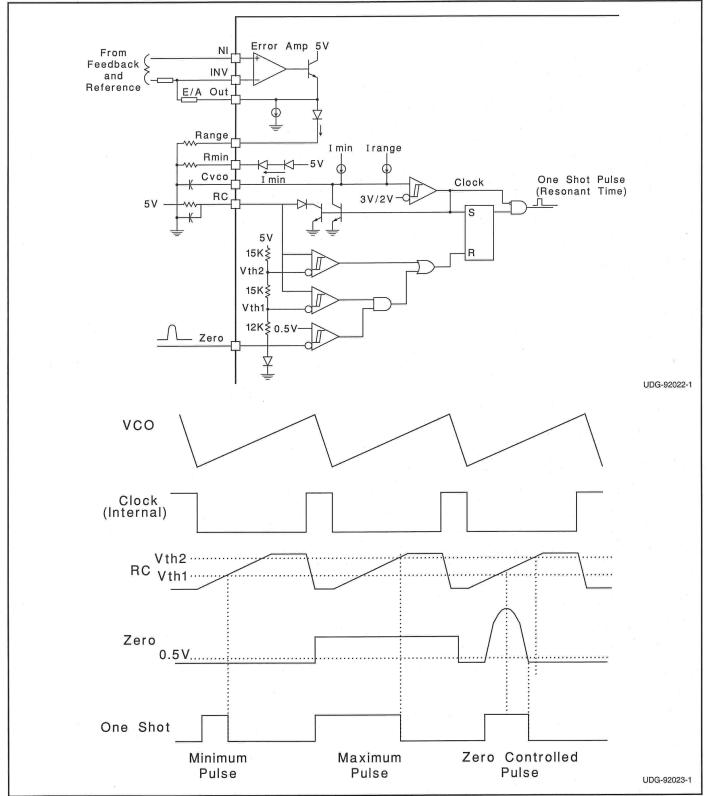


Figure 2. Error Amp, Voltage Controlled Oscillator, and One Shot

APPLICATION INFORMATION

Minimum oscillator frequency is set by Rmin and Cvco. The minimum frequency is approximately given by the equation:

$$F_{MIN} \cong \frac{3.6}{R_{MIN} \bullet C_{VCO}}$$

Maximum oscillator frequency is set by Rmin, Range & Cvco. The maximum frequency is approximately given by the equation:

$$F_{MAX} \cong \frac{3.6}{(R_{MIN} / / Range) \bullet C_{VCO}}$$

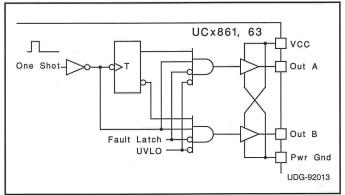
The Error Amplifier directly controls the oscillator frequency. E/A output low corresponds to minimum frequency and output high corresponds to maximum frequency. At the end of each oscillator cycle, the RC pin is discharged to one diode drop above ground. At the beginning of the oscillator cycle, V(RC) is less than Vth1 and so the output of the zero detect comparator is ignored. After V(RC) exceeds Vth1, the one shot pulse will be terminated as soon as the zero pin falls below 0.5V or V(RC) exceeds Vth2. The minimum one shot pulse width is approximately given by the equation:

Tpw(min) 0.3 R C.

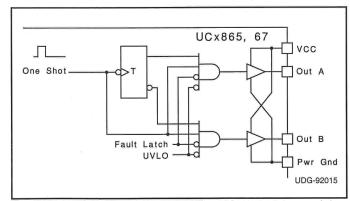
The maximum pulse width is approximately given by:

Tpw(max) 1.2 R C.

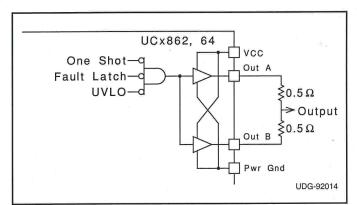
STEERING LOGIC



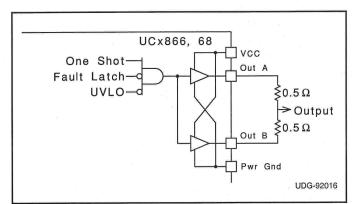
The steering logic is configured on the UC1861,63 to result in dual non-overlapping square waves at outputs A & B. This is suited to drive dual switch ZVS systems.



The steering logic is configured on the UC1865,67 to result in alternating pulse trains at outputs A & B. This is suited to drive dual switch ZCS systems.



The steering logic is configured on the UC1862,64 to result in inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZVS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.



The steering logic is configured on the UC1866,68 to result in non-inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZCS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.

APPLICATION INFORMATION (cont.)

Internal One Shot	
Out AUCx861,63	
UCx862,64	
Out AUCx865,67	
UCx866,68	UDG-92017

Figure 3. Current waveforms.



20-May-2016

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
5962-9203101M2A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
5962-9203101MEA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
5962-9203102MEA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
5962-9203103Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9203103Q2A UC1863L/ 883B	Samples
5962-9203103QEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9203103QE A UC1863J/883B	Samples
5962-9203103V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9203103V2A UC1863L QMLV	Samples
UC1861J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1861J883B	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1863J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1863J	Samples
UC1863J883B	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9203103QE A UC1863J/883B	Samples
UC1863L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1863L	Samples
UC1863L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9203103Q2A UC1863L/ 883B	Samples
UC1864J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1864J883B	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1864L	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
UC1864L883B	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
UC1865J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1865J883B	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1867J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		



PACKAGE OPTION ADDENDUM

20-May-2016

Orderable Device	Status	Package Type		Pins		Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
UC1867L	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
UC2861DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2861DW	Samples
UC2861DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2861DW	Samples
UC2861Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	UC2861Q	Samples
UC2863DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2863DW	Samples
UC2864DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2864DW	Samples
UC3861DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3861DW	Samples
UC3861DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3861DW	Samples
UC3861N	ACTIVE	PDIP	Ν	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3861N	Samples
UC3861NG4	ACTIVE	PDIP	Ν	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3861N	Samples
UC3863DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3863DW	Samples
UC3863DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3863DW	Samples
UC3865DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3865DW	Samples
UC3867DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3867DW	Samples
UC3867DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3867DW	Samples
UC3867N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3867N	Samples
UC3867NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3867N	Samples

⁽¹⁾ The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

PACKAGE OPTION ADDENDUM



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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design. **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available. **OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UC1861, UC1863, UC1863-SP, UC1865, UC1867, UC3861, UC3863, UC3865, UC3867 :

• Catalog: UC3861, UC3863, UC1863, UC3865, UC3867

• Military: UC1861, UC1863, UC1865, UC1867

• Space: UC1863-SP



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20-May-2016

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

PACKAGE MATERIALS INFORMATION

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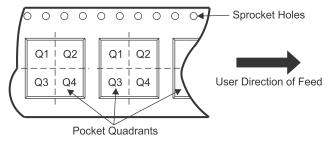
Texas Instruments

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	-	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3867DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

24-Jul-2013



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3867DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

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