TPS3808 Low-Quiescent-Current, Programmable-Delay Supervisory Circuit

1 Features

- Power-On Reset Generator with Adjustable Delay Time: 1.25 ms to 10 s
- Very Low Quiescent Current: 2.4 µA Typical
- High Threshold Accuracy: 0.5% Typ
- Fixed Threshold Voltages for Standard Voltage Rails from 0.9 V to 5 V and Adjustable Voltage Down to 0.4 V Are Available
- Manual Reset ($\overline{MR}$) Input
- Open-Drain $\overline{RESET}$ Output
- Temperature Range: –40°C to 125°C
- Small SOT-23 and 2-mm × 2-mm WSON Packages

2 Applications

- DSP or Microcontroller Applications
- Notebook and Desktop Computers
- PDAs and Hand-Held Products
- Portable and Battery-Powered Products
- FPGA and ASIC Applications

3 Description

The TPS3808 family of microprocessor supervisory circuits monitors system voltages from 0.4 V to 5 V, asserting an open-drain $\overline{RESET}$ signal when the SENSE voltage drops below a preset threshold or when the manual reset ($\overline{MR}$) pin drops to a logic low. The $\overline{RESET}$ output remains low for the user-adjustable delay time after the SENSE voltage and manual reset ($\overline{MR}$) return above the respective thresholds.

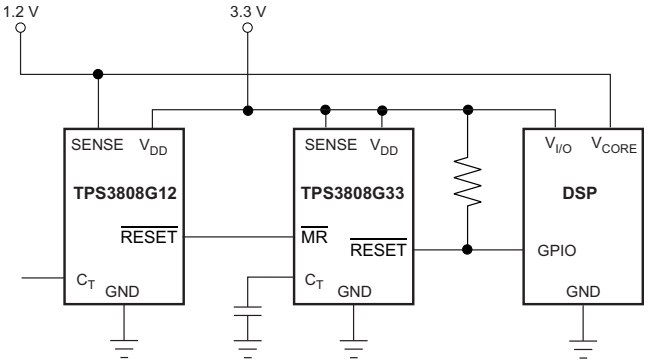
The TPS3808 device uses a precision reference to achieve 0.5% threshold accuracy for $V_{IT} \leq 3.3$ V. The reset delay time can be set to 20 ms by disconnecting the C_T pin, 300 ms by connecting the C_T pin to V_{DD} using a resistor, or can be user-adjusted between 1.25 ms and 10 s by connecting the C_T pin to an external capacitor. The TPS3808 device has a very low typical quiescent current of 2.4 µA, so it is well-suited to battery-powered applications. It is available in the SOT-23 and 2-mm × 2-mm WSON packages, and is fully specified over a temperature range of –40°C to 125°C (T_J).

Device Information[1]

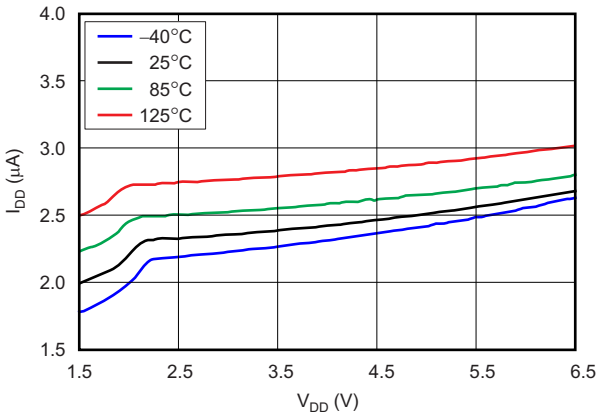
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS3808	SOT-23 (6)	2.90 mm x 1.60 mm
	WSON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



Supply Current vs Supply Voltage



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (August 2008) to Revision K **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. Moved *Switching Characteristics* table, timing diagram, and related truth table. ... 1
- Changed Figure 13; removed capacitor shown on C_T ... 14

5 Device Voltage Thresholds

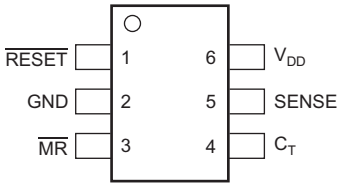
The following table shows the nominal rail to be monitored and the corresponding threshold voltage of the device.

PART NUMBER	NOMINAL SUPPLY VOLTAGE(1)	THRESHOLD VOLTAGE (V_{IT})
TPS3808G01	Adjustable	0.405 V
TPS3808G09	0.9 V	0.84 V
TPS3808G12	1.2 V	1.12 V
TPS3808G125	1.25 V	1.16 V
TPS3808G15	1.5 V	1.40 V
TPS3808G18	1.8 V	1.67 V
TPS3808G19	1.9 V	1.77 V
TPS3808G25	2.5 V	2.33 V
TPS3808G30	3 V	2.79 V
TPS3808G33	3.3 V	3.07 V
TPS3808G50	5 V	4.65 V

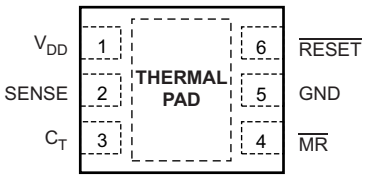
(1) Custom threshold voltages from 0.82 V to 3.3 V, 4.4 V to 5 V are available through the use of factory EEPROM programming. Minimum order quantities apply. Contact the factory for details and availability.

6 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



DRV Package
6-Pin (2.00 mm × 2.00 mm) WSON With Thermal Pad
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	WSON		
C_T	4	3	I	Reset period programming pin. Connecting this pin to V_{DD} through a 40-kΩ to 200-kΩ resistor or leaving it open results in fixed delay times (see *Electrical Characteristics*). Connecting this pin to a ground referenced capacitor ≥ 100 pF gives a user-programmable delay time. See the *Selecting the RESET Delay Time* section for more information.
GND	2	5	—	Ground
$\overline{MR}$	3	4	I	Driving the manual reset pin ($\overline{MR}$) low asserts $\overline{RESET}$. $\overline{MR}$ is internally tied to V_{DD} by a 90-kΩ pull-up resistor.
$\overline{RESET}$	1	6	O	$\overline{RESET}$ is an open-drain output that is driven to a low-impedance state when $\overline{RESET}$ is asserted (either the SENSE input is lower than the threshold voltage (V_{IT}) or the $\overline{MR}$ pin is set to a logic low). $\overline{RESET}$ remains low (asserted) for the reset period after both SENSE is above V_{IT} and $\overline{MR}$ is set to a logic high. A pull-up resistor from 10 kΩ to 1 MΩ should be used on this pin, and allows the reset pin to attain voltages higher than V_{DD}.
SENSE	5	2	I	This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage V_{IT}, then $\overline{RESET}$ is asserted.
V_{DD}	6	1	I	Supply voltage. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.
Thermal Pad	—	Pad	—	Thermal Pad. Connect to ground plane to enhance thermal performance of package.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	V_{DD}	–0.3	7	V
	V_{CT}	–0.3	V_{DD} + 0.3	V
	V_{RESET}, V_{MR}, V_{SENSE}	–0.3	7	V
Current	$\overline{RESET}$ pin	–5	5	mA
Temperature	Operating junction, T_J (2)	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Input supply range	1.7		6.5	V
V_{SENSE}	SENSE pin voltage	0		6.5	V
$V_{(Ct)}$	C_T pin voltage			V_{DD}	V
$V_{\overline{MR}}$	$\overline{MR}$ pin voltage	0		6.5	V
$V_{\overline{RESET}}$	$\overline{RESET}$ pin voltage	0		6.5	V
$I_{\overline{RESET}}$	$\overline{RESET}$ pin current	0.0003		5	mA

7.4 Thermal Information

THERMAL METRIC (1)		TPS3808		UNIT
		DBV (SOT-23)	DRV (WSON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.9	178.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	117.8	95.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.8	135	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.12	6.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.3	136.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	7.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

1.7 V ≤ V_{DD} ≤ 6.5 V, R_{LRESET} = 100 kΩ, C_{LRESET} = 50 pF, over operating temperature range (T_J = –40°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C(1).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input supply range		–40°C < T_J < 125°C	1.7		6.5	V
			0°C < T_J < 85°C	1.65		6.5	V
I_{DD}	Supply current (current into V_{DD} pin)		V_{DD} = 3.3 V, $\overline{RESET}$ not asserted $\overline{MR}$, $\overline{RESET}$, C_T open		2.4	5	µA
			V_{DD} = 6.5 V, $\overline{RESET}$ not asserted $\overline{MR}$, $\overline{RESET}$, C_T open		2.7	6	µA
V_{OL}	Low-level output voltage		1.3 V ≤ V_{DD} < 1.8 V, I_{OL} = 0.4 mA			0.3	V
			1.8 V ≤ V_{DD} ≤ 6.5 V, I_{OL} = 1 mA			0.4	V
V_{POR}	Power-up reset voltage(2)		V_{OL} (max) = 0.2 V, $I_{\overline{RESET}}$ = 15 µA			0.8	V
V_{IT}	Negative-going input threshold accuracy	TPS3808G01		–2%	±1%	2%	
			V_{IT} ≤ 3.3 V	–1.5%	±0.5%	1.5%	
			3.3 V < V_{IT} ≤ 5.0 V	–2%	±1%	2%	
			V_{IT} ≤ 3.3 V, –40°C < T_J < 85°C	–1.25%	±0.5%	1.25%	
			3.3 V < V_{IT} ≤ 5.0 V, –40°C < T_J < 85°C	–1.5%	±0.5%	1.5%	
V_{HYS}	Hysteresis on V_{IT} pin	TPS3808G01			1.5%	3%	V_{IT}
		Fixed versions			1%	2.5%	V_{IT}
$R_{\overline{MR}}$	$\overline{MR}$ Internal pullup resistance			70	90		kΩ
I_{SENSE}	Input current at SENSE pin	TPS3808G01	V_{SENSE} = V_{IT}	–25		25	nA
		Fixed versions	V_{SENSE} = 6.5 V		1.7		µA
I_{OH}	$\overline{RESET}$ leakage current		$V_{\overline{RESET}}$ = 6.5 V, $\overline{RESET}$ not asserted			300	nA
C_{IN}	Input capacitance, any pin	C_T pin	V_{IN} = 0 V to V_{DD}		5		pF
		Other pins	V_{IN} = 0 V to 6.5 V		5		pF
V_{IL}	$\overline{MR}$ logic low input			0		0.3 V_{DD}	V
V_{IH}	$\overline{MR}$ logic high input			0.7 V_{DD}		V_{DD}	V

(1) R_{LRESET} and C_{LRESET} are the resistor and capacitor connected to the RESET pin.
(2) The lowest supply voltage (V_{DD}) at which $\overline{RESET}$ becomes active. $T_{rise(VDD)}$ ≥ 15 µs/V.

7.6 Switching Characteristics

1.7 V ≤ V_{DD} ≤ 6.5 V, R_{LRESET} = 100 kΩ, C_{LRESET} = 50 pF, over operating temperature range (T_J = –40°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Input pulse width to $\overline{\text{RESET}}$	SENSE	V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		20		µs
		$\overline{\text{MR}}$	V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		0.001		
t_d	$\overline{\text{RESET}}$ delay time	C_T = Open	See *Figure 1*	12	20	28	ms
		C_T = V_{DD}		180	300	420	
		C_T = 100 pF		0.75	1.25	1.75	
		C_T = 180 nF		0.7	1.2	1.7	s
	Propagation delay	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$	V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		150		ns
	High-to-low level $\overline{\text{RESET}}$ delay	SENSE to $\overline{\text{RESET}}$	V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		20		µs

(1) R_{LRESET} and C_{LRESET} are the resistor and capacitor connected to the RESET pin.

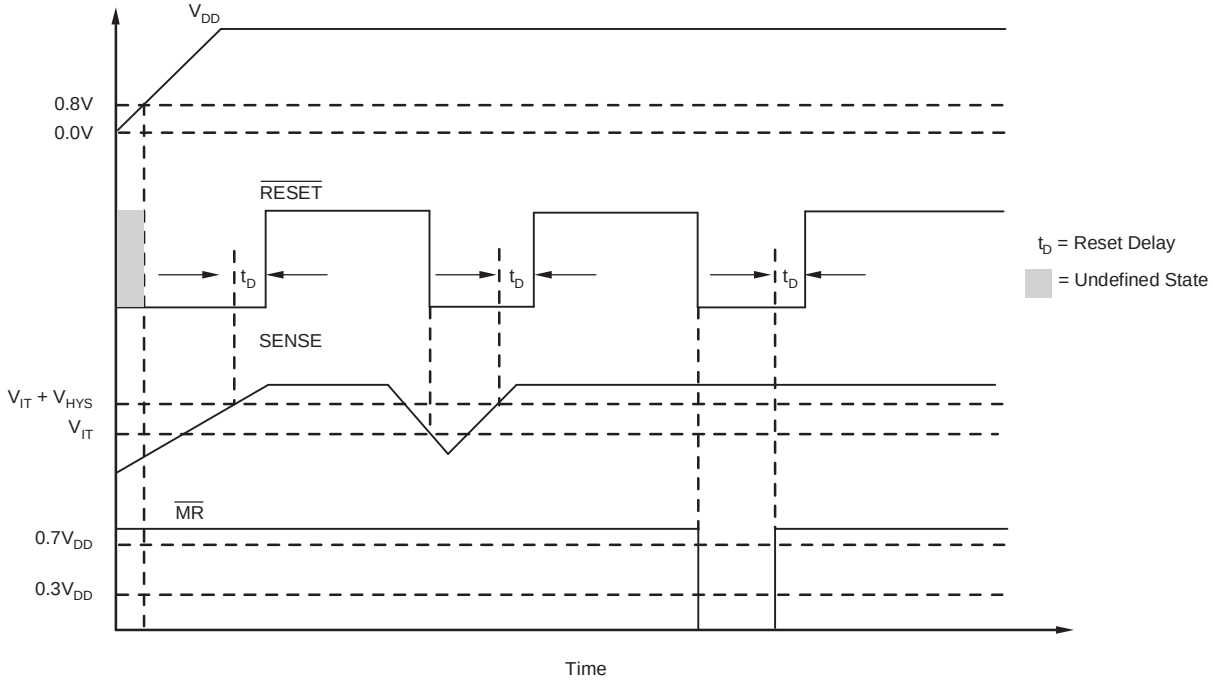


Figure 1. TPS3808 Timing Diagram Showing $\overline{\text{MR}}$ and SENSE Reset Timing

7.7 Typical Characteristics

At T_J = 25°C, V_{DD} = 3.3 V, R_{LRESET} = 100 kΩ, and C_{LRESET} = 50 pF, unless otherwise noted.

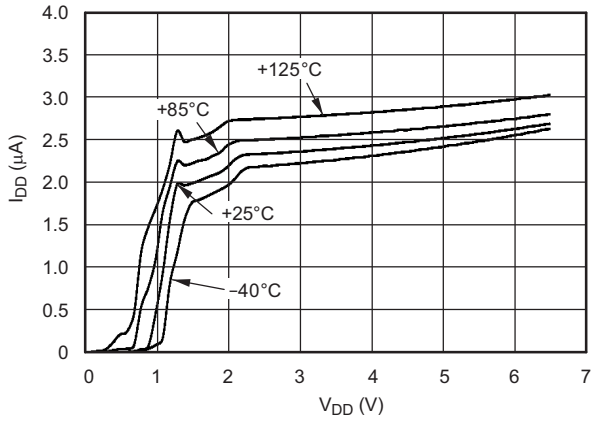


Figure 2. Supply Current vs Supply Voltage

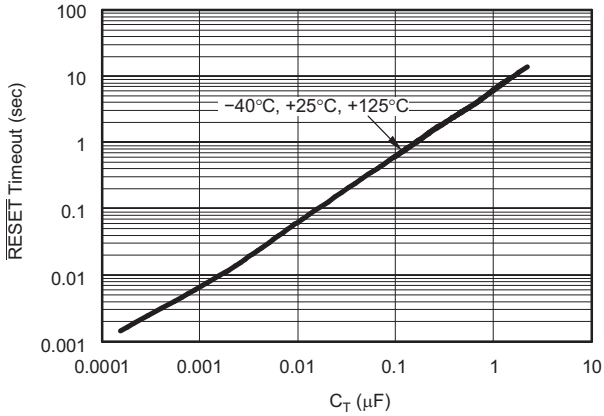


Figure 3. $\overline{\text{RESET}}$ Time-Out Period vs C_T

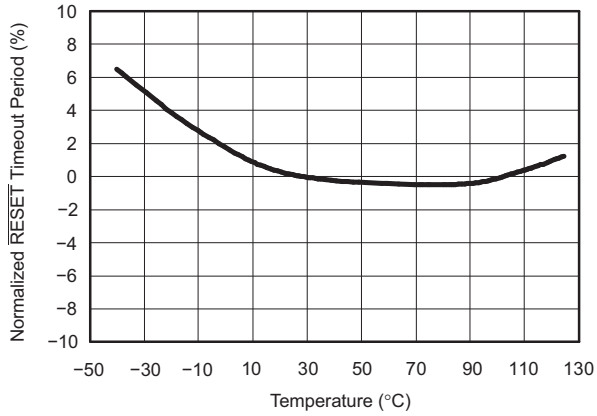


Figure 4. Normalized $\overline{\text{RESET}}$ Time-Out Period vs Temperature (C_T = Open, C_T = V_{DD}, C_T = Any)

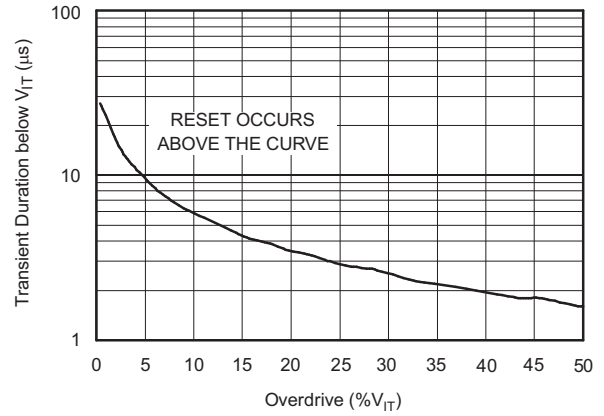


Figure 5. Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage

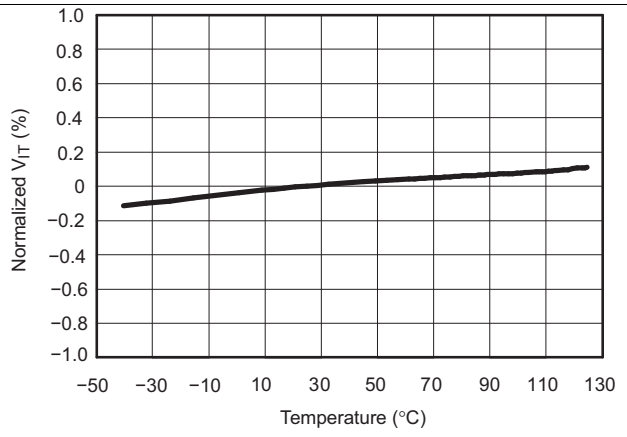


Figure 6. Normalized Sense Threshold Voltage (V_{IT}) vs Temperature

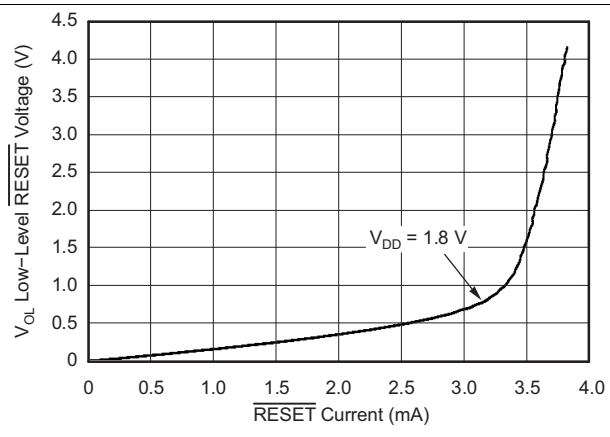


Figure 7. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current

A. R_{LRESET} and C_{LRESET} are the resistor and capacitor connected to the RESET pin.

Typical Characteristics (continued)

At T_J = 25°C, V_{DD} = 3.3 V, R_{LRESET} = 100 kΩ, and C_{LRESET} = 50 pF, unless otherwise noted.

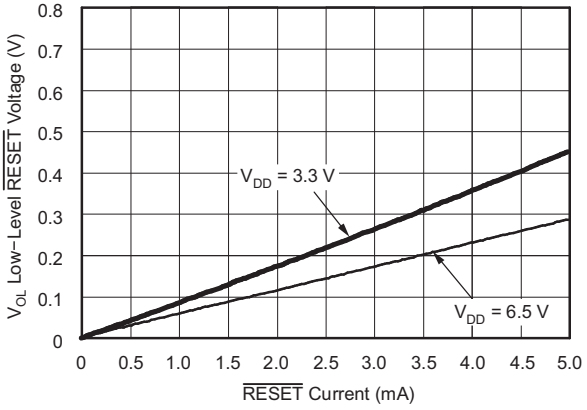


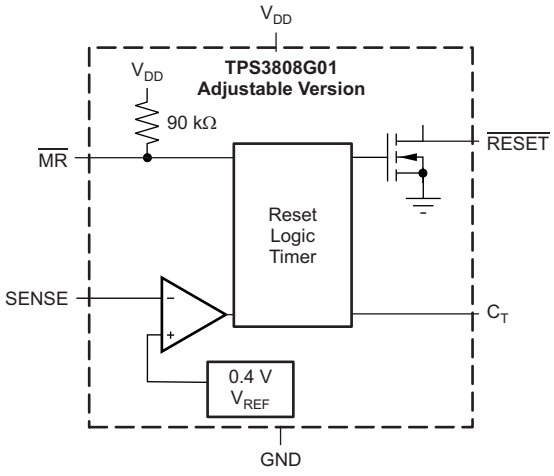
Figure 8. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current

8 Detailed Description

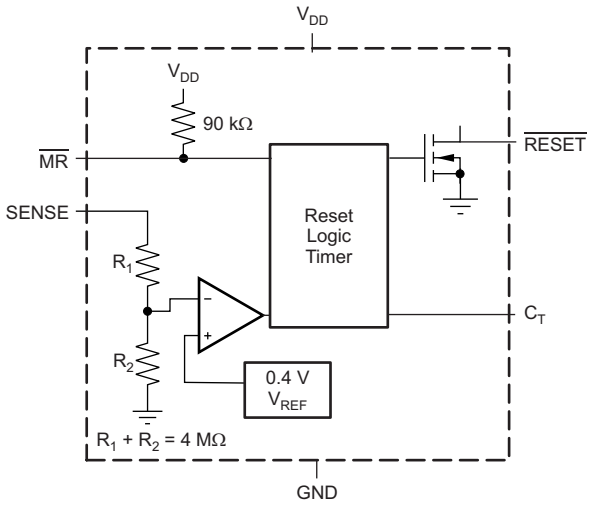
8.1 Overview

The TPS3808 microprocessor supervisory product family is designed to assert a $\overline{\text{RESET}}$ signal when either the SENSE pin voltage drops below V_{IT} or the manual reset ($\overline{\text{MR}}$) is driven low. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after both the manual reset ($\overline{\text{MR}}$) and SENSE voltages return above their respective thresholds.

8.2 Functional Block Diagram



Adjustable Voltage Version



Fixed Voltage Version

8.3 Feature Description

A broad range of voltage threshold and reset delay time adjustments are available for the TPS3808 device, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82 V to 3.3 V or from 4.4 V to 5 V, while the TPS3808G01 can be set to any voltage above 0.405 V using an external resistor divider. Two preset delay times are also user-selectable: connecting the C_T pin to V_{DD} results in a 300-ms reset delay, whereas leaving the C_T pin open yields a 20-ms reset delay. In addition, connecting a capacitor between C_T and GND allows the designer to select any reset delay period from 1.25 ms to 10 s.

8.3.1 SENSE Input

The SENSE input provides a pin at which any system voltage can be monitored. If the voltage on this pin drops below V_{IT}, then $\overline{\text{RESET}}$ is asserted. The comparator has a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$ assertions and de-assertions. It is good analog design practice to put a 1-nF to 10-nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

The TPS3808 device is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive, as shown in (Figure 5).

The TPS3808G01 can be used to monitor any voltage rail down to 0.405 V using the circuit shown in Figure 9.

Feature Description (continued)

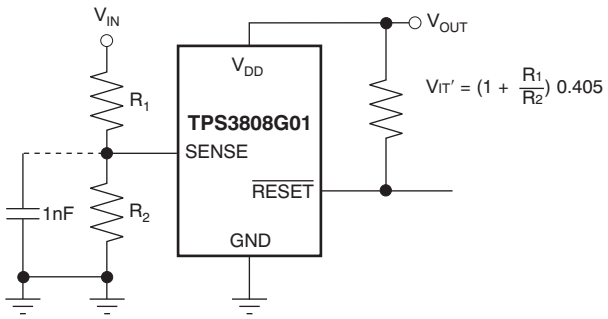


Figure 9. Using the TPS3808G01 to Monitor a User-Defined Threshold Voltage

8.3.2 Selecting the RESET Delay Time

The TPS3808 has three options for setting the $\overline{\text{RESET}}$ delay time as shown in Figure 10. Figure 10 (a) shows the configuration for a fixed 300-ms typical delay time by tying C_T to V_{DD}; a resistor from 40 kΩ to 200 kΩ must be used. Supply current is not affected by the choice of resistor. Figure 10 (b) shows a fixed 20-ms delay time by leaving the C_T pin open. Figure 10 (c) shows a ground referenced capacitor connected to C_T for a user-defined program time between 1.25 ms and 10 s.

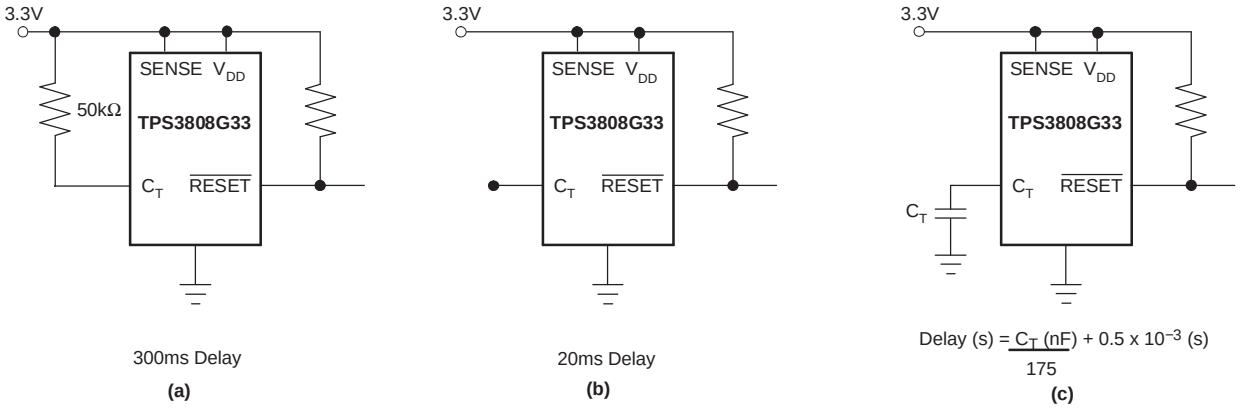


Figure 10. Configuration Used to Set the $\overline{\text{RESET}}$ Delay Time

The capacitor C_T should be ≥ 100 pF nominal value in order for the TPS3808xxx to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using Equation 1.

$$C_T\,(\text{nF}) = \left[t_D\,(\text{s}) - 0.5 \times 10^{-3}\,(\text{s})\right] \times 175 \quad (1)$$

The reset delay time is determined by the time it takes an on-chip precision 220-nA current source to charge the external capacitor to 1.23 V. When a $\overline{\text{RESET}}$ is asserted, the capacitor is discharged. When the $\overline{\text{RESET}}$ conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23 V, $\overline{\text{RESET}}$ is deasserted. Note that a low-leakage type capacitor such as a ceramic should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

Feature Description (continued)

8.3.3 Manual RESET ($\overline{MR}$) Input

The manual reset ($\overline{MR}$) input allows a processor or other logic circuits to initiate a reset. A logic low (0.3 V_{DD}) on $\overline{MR}$ causes $\overline{RESET}$ to assert. After $\overline{MR}$ returns to a logic high and SENSE is above its reset threshold, $\overline{RESET}$ is de-asserted after the user-defined reset delay expires. Note that $\overline{MR}$ is internally tied to V_{DD} using a 90-kΩ resistor, so this pin can be left unconnected if $\overline{MR}$ is not used.

See Figure 11 for how $\overline{MR}$ can be used to monitor multiple system voltages. Note that if the logic signal driving $\overline{MR}$ does not go fully to V_{DD}, there is some additional current draw into V_{DD} as a result of the internal pullup resistor on $\overline{MR}$. To minimize current draw, a logic-level FET can be used as illustrated in Figure 12.

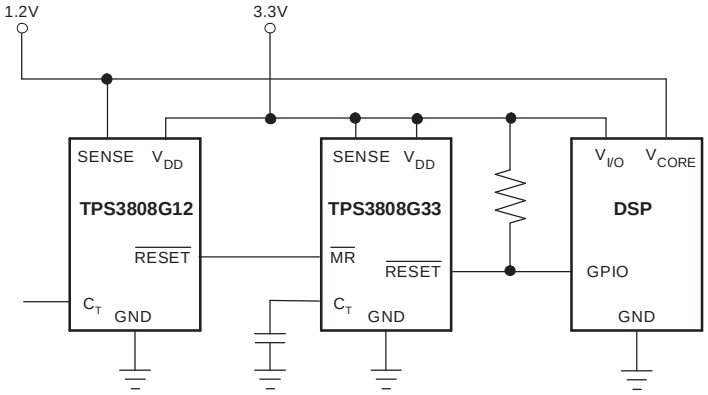


Figure 11. Using $\overline{MR}$ to Monitor Multiple System Voltages

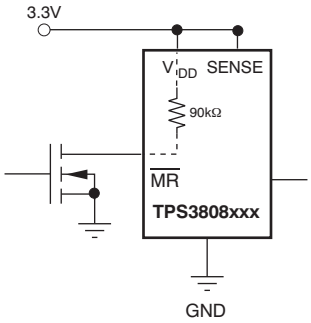


Figure 12. Using an External MOSFET to Minimize I_{DD} When $\overline{MR}$ Signal Does Not Go to V_{DD}

8.3.4 RESET Output

$\overline{RESET}$ remains high (unasserted) as long as SENSE is above its threshold (V_{IT}) and the manual reset ($\overline{MR}$) is logic high. If either SENSE falls below V_{IT} or $\overline{MR}$ is driven low, $\overline{RESET}$ is asserted, driving the $\overline{RESET}$ pin to a low impedance.

Once $\overline{MR}$ is again logic high and SENSE is above V_{IT} + V_{HYS} (the threshold hysteresis), a delay circuit is enabled that holds $\overline{RESET}$ low for a specified reset delay period. Once the reset delay has expired, the $\overline{RESET}$ pin goes to a high impedance state. The pullup resistor from the open-drain $\overline{RESET}$ to the supply line can be used to allow the reset signal for the microprocessor to have a voltage higher than V_{DD} (up to 6.5 V). The pullup resistor should be no smaller than 10 kΩ as a result of the finite impedance of the $\overline{RESET}$ line.

8.4 Device Functional Modes

Table 1. Truth Table

$\overline{MR}$	SENSE > V_{IT}	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

8.4.1 Normal Operation ($V_{DD} > V_{DD(min)}$)

When V_{DD} is greater than $V_{DD(min)}$, the $\overline{RESET}$ signal is determined by the voltage on the SENSE pin and the logic state of $\overline{MR}$.

- $\overline{MR}$ high: When the voltage on V_{DD} is greater than 1.7 V for a time of the selected t_D, the $\overline{RESET}$ signal corresponds to the voltage on SENSE relative to V_{IT}.
- $\overline{MR}$ low: in this mode, $\overline{RESET}$ is held low regardless of the value of the SENSE pin.

8.4.2 Above Power-On Reset but Less Than $V_{DD(min)}$ ($V_{POR} < V_{DD} < V_{DD(min)}$)

When the voltage on V_{DD} is less than the device $V_{DD(min)}$ voltage, and greater than the power-on reset voltage (V_{POR}), the $\overline{RESET}$ signal is asserted and low impedance, respectively, regardless of the voltage on the SENSE pin.

8.4.3 Below Power-On Reset ($V_{DD} < V_{POR}$)

When the voltage on V_{DD} is lower than the required voltage (V_{POR}) needed to internally pull the asserted output to GND, $\overline{RESET}$ is undefined and should not be relied upon for proper device function.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.2 Typical Application

A typical application of the TPS3808G25 used with a 2.5-V processor is shown in Figure 13. The open-drain $\overline{\text{RESET}}$ output is typically connected to the $\overline{\text{RESET}}$ input of a microprocessor. A pullup resistor must be used to hold this line high when $\overline{\text{RESET}}$ is not asserted. The $\overline{\text{RESET}}$ output is undefined for voltage below 0.8 V, but this characteristic is normally not a problem because most microprocessors do not function below this voltage.

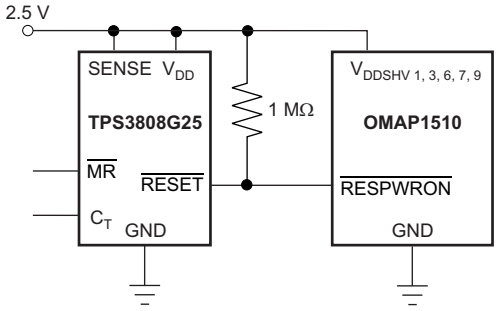


Figure 13. Typical Application of the TPS3808 With an OMAP Processor

9.2.1 Design Requirements

The TPS3808 is intended to drive the $\overline{\text{RESET}}$ input of a microprocessor. The $\overline{\text{RESET}}$ pin is pulled high with a 1-MΩ resistor and the reset delay time is controlled by C_T depending on the reset requirement times of the microprocessor. In this case, C_T is left open for a typical reset delay time of 20 ms.

9.2.2 Detailed Design Procedure

The primary constraint for this application is the reset delay time. In this case, because C_T is open, it is set to 20 ms. A 0.1-µF decoupling capacitor is connected to the V_{DD} pin and a 1-MΩ resistor is used to pull up the $\overline{\text{RESET}}$ pin high. The $\overline{\text{MR}}$ pin can be connected to an external signal if desired.

9.2.2.1 Immunity to SENSE Pin Voltage Transients

The TPS3808 is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients depends on threshold overdrive. Threshold overdrive is defined by how much the V_{SENSE} exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the $\overline{\text{RESET}}$ response. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 2:

$$\text{Overdrive} = | (V_{SENSE} / V_{IT} - 1) \times 100\% | \quad (2)$$

where:

- V_{IT} is the threshold voltage.

Figure 14 shows this relationship.

Typical Application (continued)

9.2.3 Application Curve

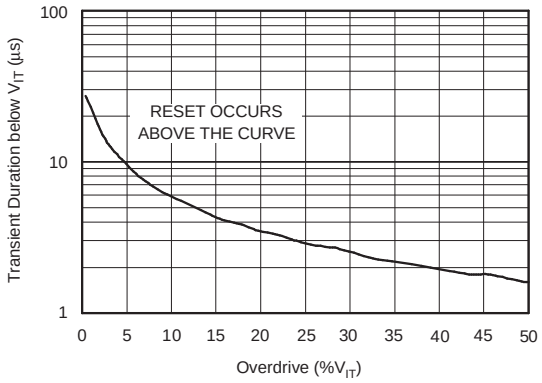


Figure 14. Maximum Transient Duration at SENSE vs SENSE Threshold Overdrive Voltage

10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.7 V and 6.5 V. Use a low-impedance power supply to eliminate inaccuracies caused by current changes during the voltage reference refresh.

11 Layout

11.1 Layout Guidelines

Make sure the connection to the V_{DD} pin is low impedance. Place a 0.1-µF ceramic capacitor near the V_{DD} pin. If no capacitor is connected to the C_T pin, parasitic capacitance on this pin should be minimized so the $\overline{\text{RESET}}$ delay time is not adversely affected.

11.2 Layout Example

The layout example in Figure 15 shows how the TPS3808 is laid out on a printed circuit board (PCB) for a 20-ms delay.

Layout Example (continued)

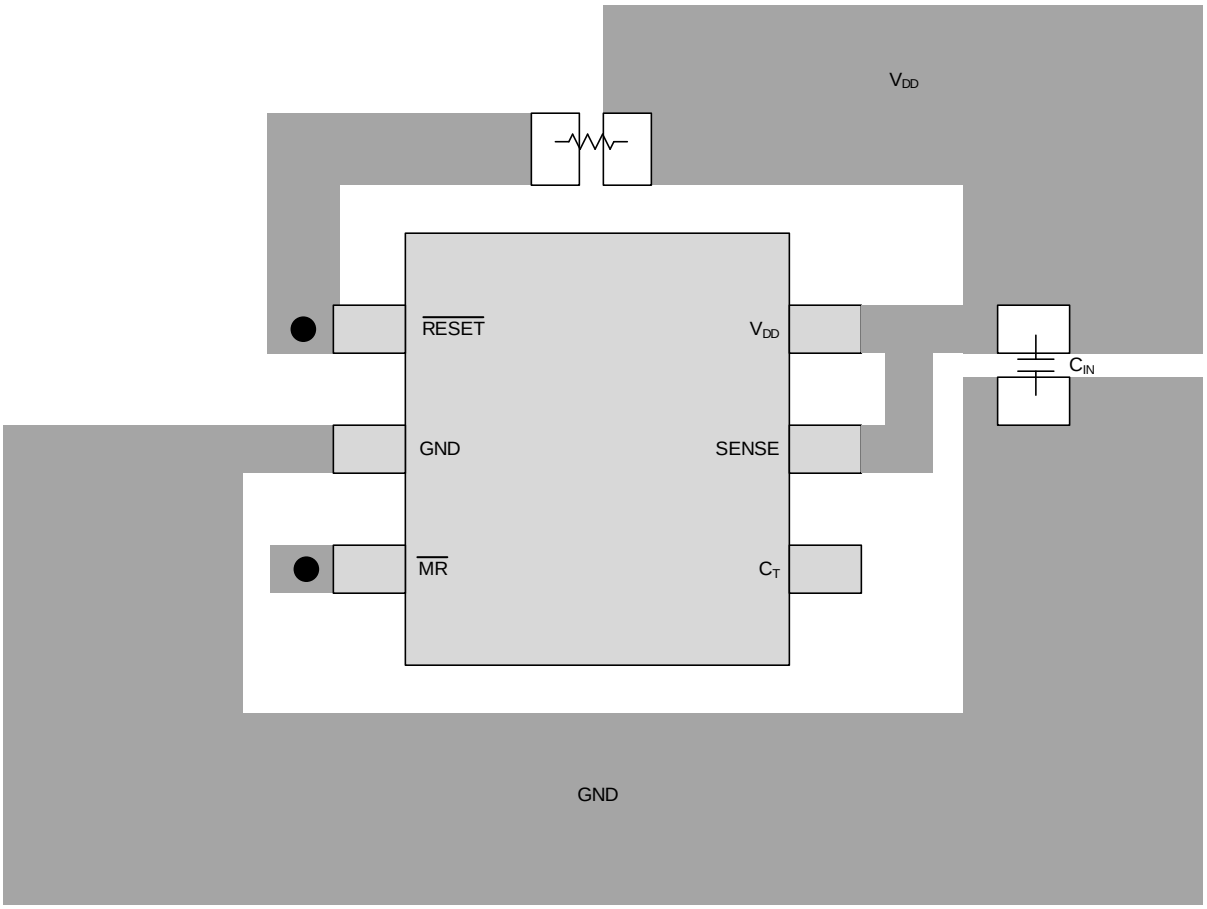


Figure 15. Layout Example for a 20-ms Delay

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS3808. The TPS3808G01DBVEVM evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

12.2 Documentation Support

12.2.1 Related Documentation

The following related documents are available for download at www.ti.com:

- Application note. *Optimizing Resistor Dividers at a Comparator Input*. Literature number SLVA450.
- Application note. *Sensitivity Analysis for Power Supply Design*. Literature number SLVA481.
- TPS3808G01DBVEVM Evaluation Module User Guide. Literature number SBVU015.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
900-0380801	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVW	Samples
TPS3808G01DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVW	Samples
TPS3808G01DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVW	Samples
TPS3808G01DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVW	Samples
TPS3808G01DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVW	Samples
TPS3808G01DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVW	Samples
TPS3808G01DRVRG4	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVW	Samples
TPS3808G01DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVW	Samples
TPS3808G01DRVTG4	ACTIVE	WSON	DRV	6		TBD	Call TI	Call TI	-40 to 125		Samples
TPS3808G09DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVV	Samples
TPS3808G09DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVV	Samples
TPS3808G09DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVV	Samples
TPS3808G09DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVV	Samples
TPS3808G125DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CAC	Samples
TPS3808G125DBVRG4	ACTIVE	SOT-23	DBV	6		TBD	Call TI	Call TI	-40 to 125		Samples
TPS3808G125DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CAC	Samples
TPS3808G125DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CAC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3808G12DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVY	Samples
TPS3808G12DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVY	Samples
TPS3808G12DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVY	Samples
TPS3808G12DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVY	Samples
TPS3808G12DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVY	Samples
TPS3808G12DRVRG4	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVY	Samples
TPS3808G12DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVY	Samples
TPS3808G12DRVTG4	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVY	Samples
TPS3808G15DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVS	Samples
TPS3808G15DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVS	Samples
TPS3808G15DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVS	Samples
TPS3808G15DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVS	Samples
TPS3808G15DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVS	Samples
TPS3808G15DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVS	Samples
TPS3808G18DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVR	Samples
TPS3808G18DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVR	Samples
TPS3808G18DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVR	Samples
TPS3808G18DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVR	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3808G18DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVR	Samples
TPS3808G18DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVR	Samples
TPS3808G19DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CHP	Samples
TPS3808G19DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CHP	Samples
TPS3808G25DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVQ	Samples
TPS3808G25DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVQ	Samples
TPS3808G25DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVQ	Samples
TPS3808G25DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVQ	Samples
TPS3808G25DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVQ	Samples
TPS3808G25DRVRG4	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVQ	Samples
TPS3808G25DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVQ	Samples
TPS3808G25DRVTG4	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVQ	Samples
TPS3808G30DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVP	Samples
TPS3808G30DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVP	Samples
TPS3808G30DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVP	Samples
TPS3808G30DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVP	Samples
TPS3808G30DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVP	Samples
TPS3808G30DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3808G30DRVTG4	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVP	Samples
TPS3808G33DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVO	Samples
TPS3808G33DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVO	Samples
TPS3808G33DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVO	Samples
TPS3808G33DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVO	Samples
TPS3808G33DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SEC	Samples
TPS3808G33DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SEC	Samples
TPS3808G50DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVN	Samples
TPS3808G50DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVN	Samples
TPS3808G50DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVN	Samples
TPS3808G50DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS3808G01, TPS3808G12, TPS3808G125, TPS3808G15, TPS3808G18, TPS3808G30, TPS3808G33, TPS3808G50 :

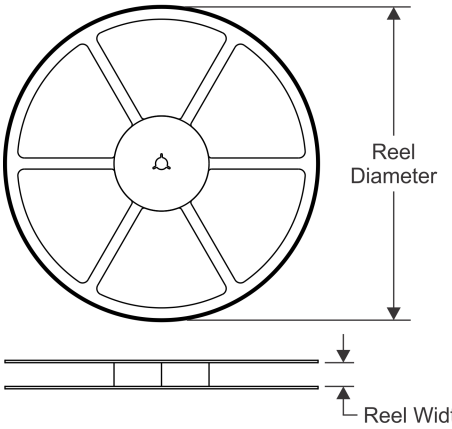
- Automotive: TPS3808G01-Q1, TPS3808G12-Q1, TPS3808G125-Q1, TPS3808G15-Q1, TPS3808G18-Q1, TPS3808G30-Q1, TPS3808G33-Q1, TPS3808G50-Q1

NOTE: Qualified Version Definitions:

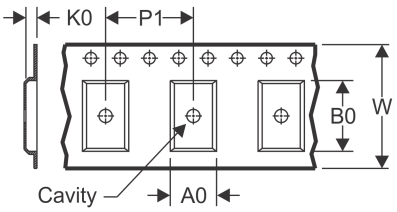
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

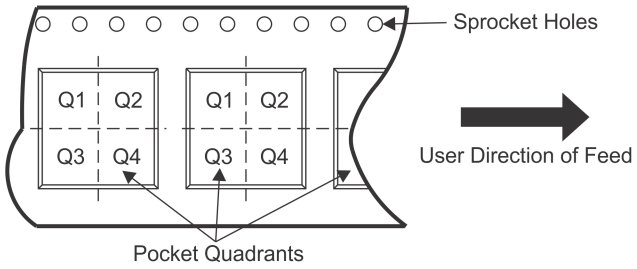


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

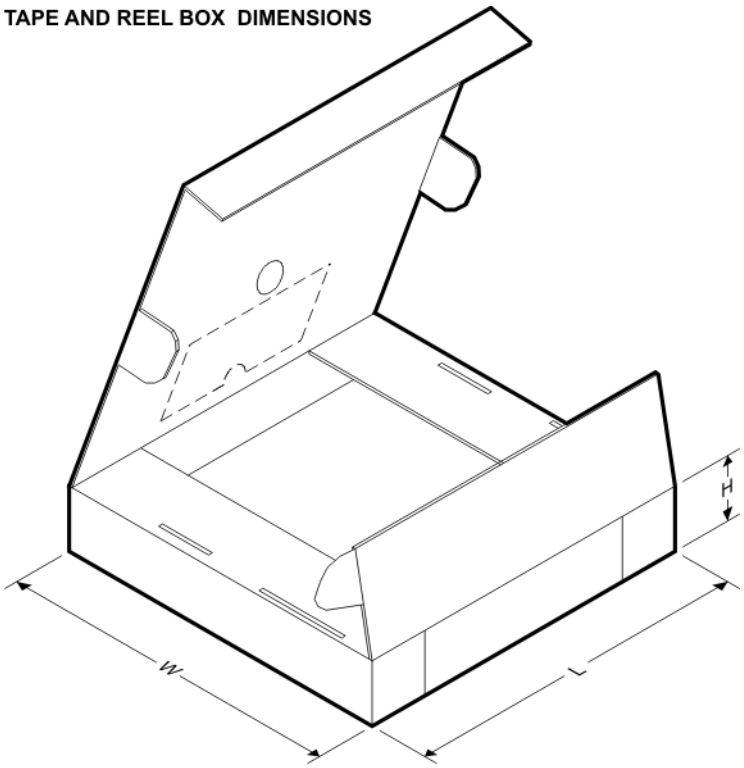


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3808G01DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G01DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G01DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS3808G01DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G01DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS3808G01DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G125DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G125DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G12DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G12DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G12DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G12DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS3808G12DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS3808G12DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G15DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G15DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G15DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G15DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3808G18DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G18DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G18DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G18DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G19DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G19DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G25DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G25DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G25DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G25DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G30DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G30DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G30DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS3808G30DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G30DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS3808G30DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G33DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G33DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G33DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G33DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G50DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3808G50DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

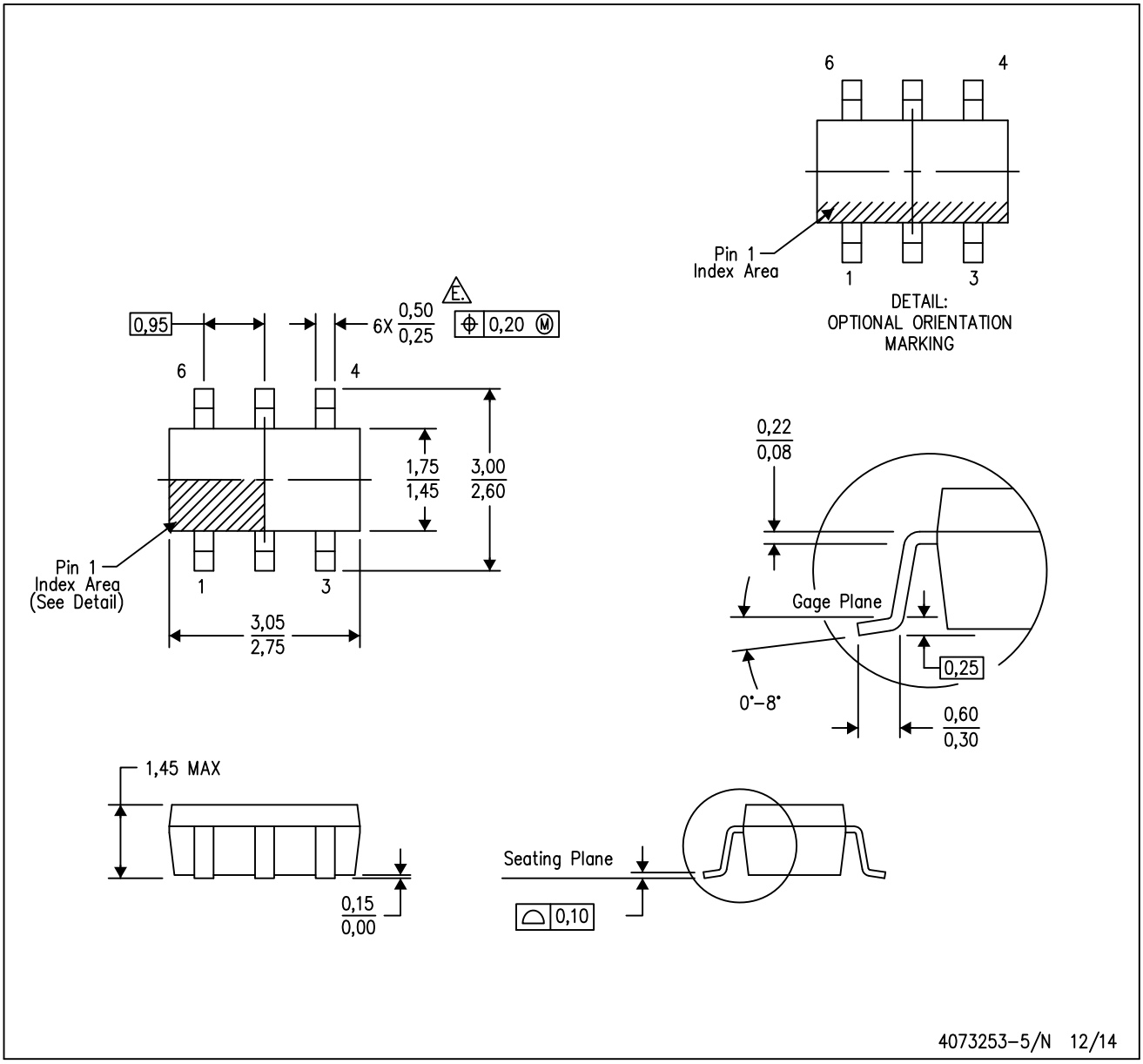


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3808G01DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G01DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G01DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS3808G01DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS3808G01DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS3808G01DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS3808G125DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3808G125DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0
TPS3808G12DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G12DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G12DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS3808G12DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS3808G12DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS3808G12DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS3808G15DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G15DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G15DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS3808G15DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS3808G18DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G18DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

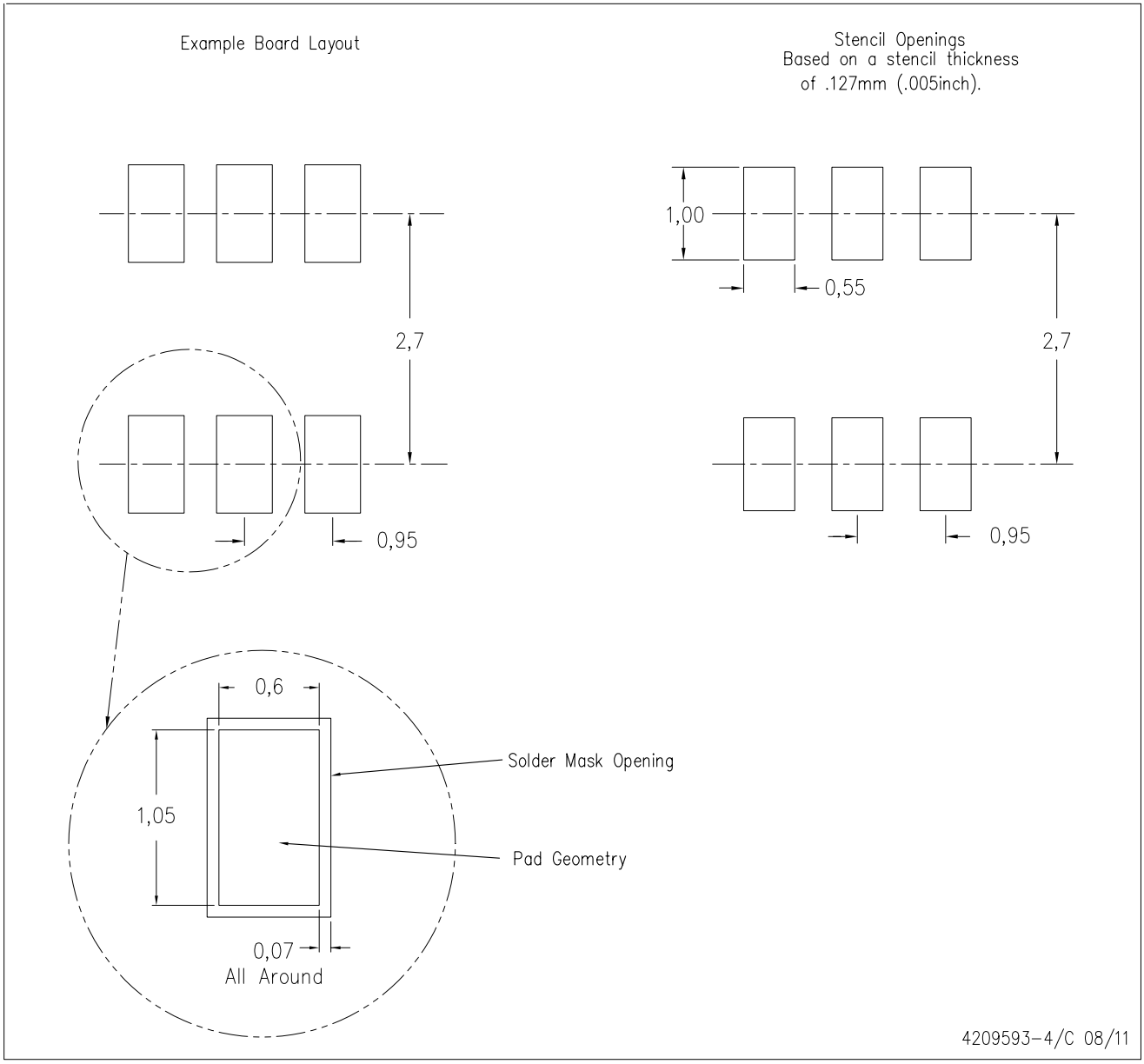
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3808G18DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS3808G18DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS3808G19DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G19DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G25DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G25DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G25DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS3808G25DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS3808G30DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G30DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G30DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS3808G30DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS3808G30DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS3808G30DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS3808G33DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G33DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3808G33DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS3808G33DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS3808G50DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3808G50DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



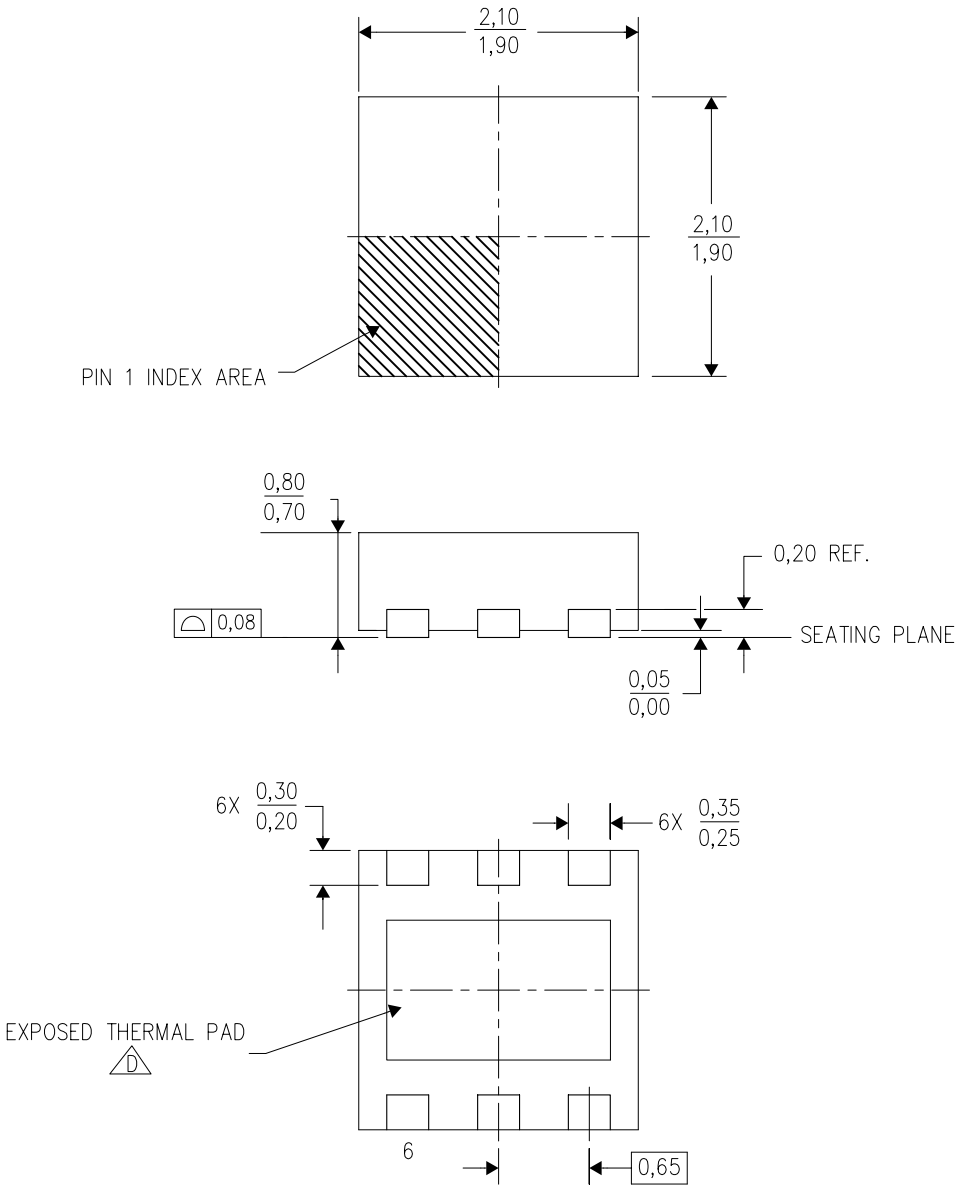
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

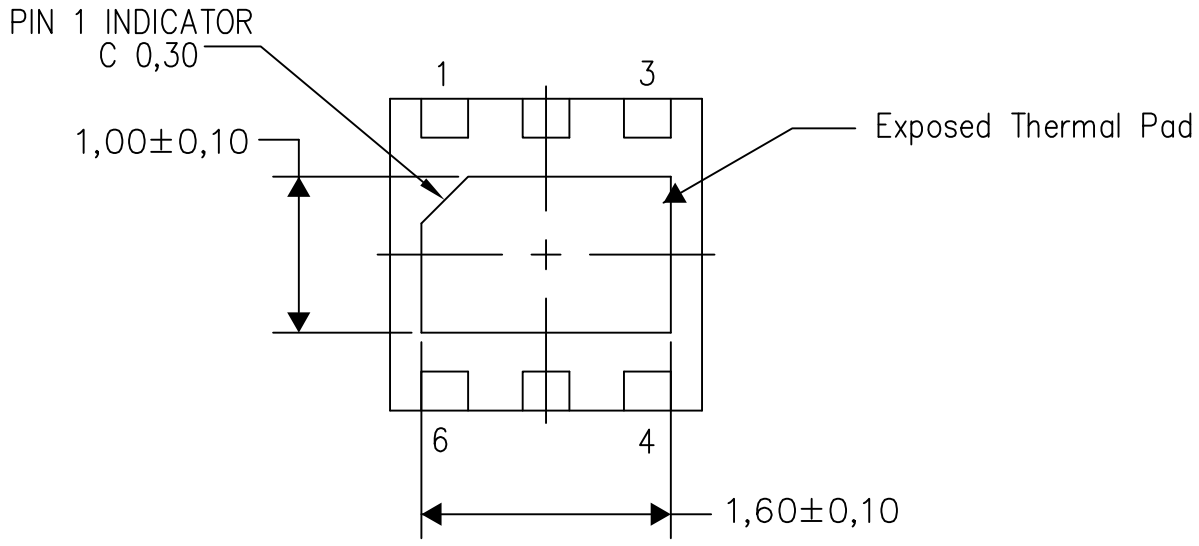
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



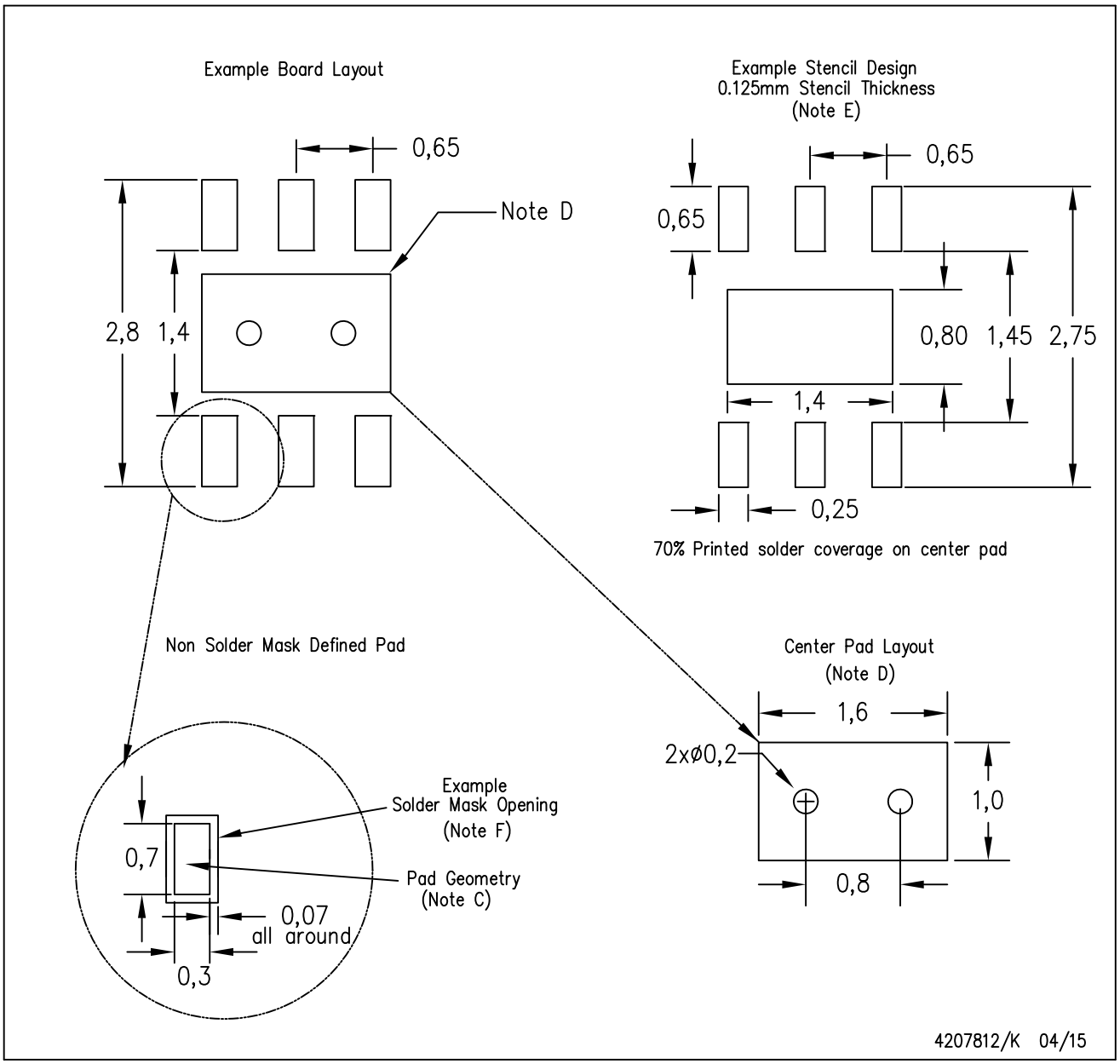
Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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