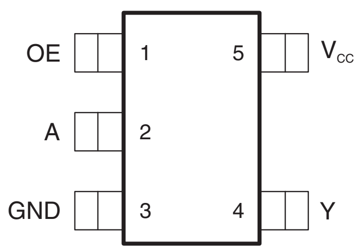
LOW-POWER SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

Check for Samples: SN74AUP1G126

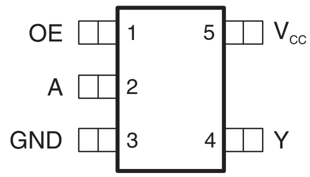
FEATURES

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption (I_{CC} = 0.9 μA Max)
- Low Dynamic-Power Consumption (C_{pd} = 4 pF Typ at 3.3 V)
- Low Input Capacitance (C_i = 1.5 pF Typ)
- Low Noise – Overshoot and Undershoot <10% of V_{CC}
- Input-Disable Feature Allows Floating Input Conditions
- I_{off} Supports Partial-Power-Down Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- t_{pd} = 4.6 ns Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22–
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

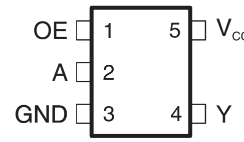
DBV PACKAGE (TOP VIEW)



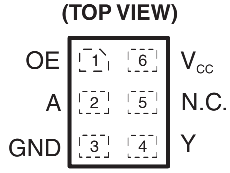
DCK PACKAGE (TOP VIEW)



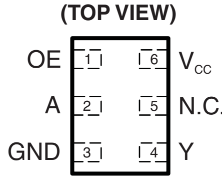
DRL PACKAGE (TOP VIEW)



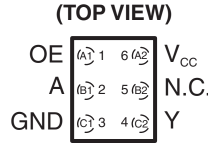
DRY PACKAGE (TOP VIEW)



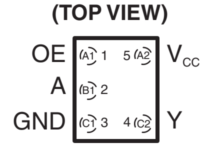
DSF PACKAGE (TOP VIEW)



YFP PACKAGE (TOP VIEW)



YZP PACKAGE (TOP VIEW)



N.C. – No internal connection.

See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figure 1 and Figure 2).

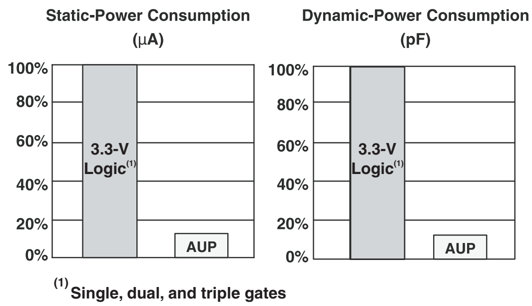


Figure 1. AUP – The Lowest-Power Family

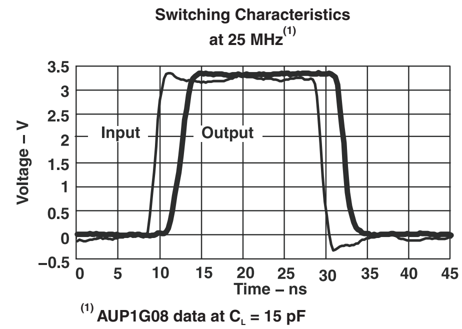


Figure 2. Excellent Signal Integrity

This bus buffer gate is a single line driver with a 3-state output. The output is disabled when the output-enable (OE) input is low. This device has the input-disable feature, which allows floating input signals.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP	Reel of 3000	SN74AUP1G126YFPR	_ _ _ HN _
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1G126YZPR	_ _ _ HN _
	QFN – DRY	Reel of 5000	SN74AUP1G126DRYR	HN
	µQFN – DSF	Reel of 5000	SN74AUP1G126DSFR	HN
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G126DBVR	H26_
		Reel of 250	SN74AUP1G126DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G126DCKR	HN_
		Reel of 250	SN74AUP1G126DCKT	
	SOT (SOT-553) – DRL	Reel of 4000	SN74AUP1G126DRLR	HN_

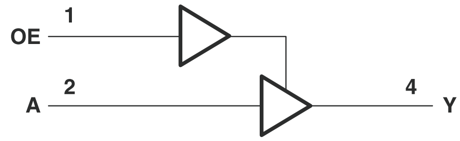
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YZP/YZT: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X(1)	Z

(1) Floating inputs allowed

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range[2]		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	4.6	V
V_O	Output voltage range in the high or low state[2]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance[3]	DBV package		206	°C/W
		DCK package		252	
		DRL package		142	
		DSF package		TBD	
		DRY package		234	
		YFP/YZP/YZT package		132	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}	3.6	V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}	3.6	
		V_{CC} = 2.3 V to 2.7 V	1.6	3.6	
		V_{CC} = 3 V to 3.6 V	2	3.6	
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V	0	0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V	0	0.7	
		V_{CC} = 3 V to 3.6 V	0	0.9	
V_O	Output voltage	Active state	0	V_{CC}	V
		3-state	0	3.6	
I_{OH}	High-level output current	V_{CC} = 0.8 V		–20	μA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65 V		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		–4	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	μA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow of Floating CMOS Inputs, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OL}		I_{OH} = –20 μA	0.8 V to 3.6 V	V_{CC} – 0.1			V_{CC} – 0.1		V
		I_{OH} = –1.1 mA	1.1 V	0.75 × V_{CC}			0.7 × V_{CC}		
		I_{OH} = –1.7 mA	1.4 V	1.11			1.03		
		I_{OH} = –1.9 mA	1.65 V	1.32			1.3		
		I_{OH} = –2.3 mA	2.3 V	2.05			1.97		
		I_{OH} = –3.1 mA		1.9			1.85		
		I_{OH} = –2.7 mA	3 V	2.72			2.67		
		I_{OH} = –4 mA		2.6			2.55		
V_{OL}		I_{OL} = 20 μA	0.8 V to 3.6 V			0.1		0.1	V
		I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
		I_{OL} = 1.7 mA	1.4 V			0.31		0.37	
		I_{OL} = 1.9 mA	1.65 V			0.31		0.35	
		I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
		I_{OL} = 3.1 mA				0.44		0.45	
		I_{OL} = 2.7 mA	3 V			0.31		0.33	
		I_{OL} = 4 mA				0.44		0.45	
I_I	A or OE input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1		0.5	μA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.2		0.6	μA
ΔI_{off}		V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.6	μA
I_{OZ}		V_O = V_{CC} or GND	3.6 V					0.5	μA
I_{CC}		V_I = GND or (V_{CC} to 3.6 V), OE = GND, I_O = 0	0.8 V to 3.6 V			0.5		0.9	μA
ΔI_{CC}	A input	V_I = V_{CC} – 0.6 V (1), I_O = 0	3.3 V			40		50	μA
	OE input					110		120	
	All inputs	V_I = GND to 3.6 V, OE = V_{CC} (2)	0.8 V to 3.6 V			0		0	
C_i		V_I = V_{CC} or GND	0 V		1.5				pF
			3.6 V		1.5				
C_o		V_O = V_{CC} or GND	3.6 V		3				pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND
(2) To show I_{CC} is very low when the input-disable feature is enabled

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		18.1				ns
			1.2 V ± 0.1 V	4.3	7.4	12.6	2.7	15.3	
			1.5 V ± 0.1 V	3.3	5.2	8.5	1	10.2	
			1.8 V ± 0.15 V	2.6	4.1	6.8	1.3	8.3	
			2.5 V ± 0.2 V	2	2.9	4.7	1.1	5.8	
			3.3 V ± 0.3 V	1.7	2.4	3.8	1	4.6	
t_{en}	OE	Y	0.8 V		19.1				ns
			1.2 V ± 0.1 V	5.1	9.3	15.9	3.6	19.2	
			1.5 V ± 0.1 V	4.1	6.6	10.5	2.5	12.7	
			1.8 V ± 0.15 V	3.2	5.3	8.7	2.1	10.3	
			2.5 V ± 0.2 V	2.5	3.8	6	1.6	7.2	
			3.3 V ± 0.3 V	2.1	3.2	4.9	1.4	5.9	
t_{dis}	OE	Y	0.8 V		12.1				ns
			1.2 V ± 0.1 V	2.4	4.1	6.9	2.2	7.7	
			1.5 V ± 0.1 V	1.8	2.9	4.5	1.7	5.1	
			1.8 V ± 0.15 V	1	2.9	4.3	1.5	4.7	
			2.5 V ± 0.2 V	1	1.8	2.7	1	3.3	
			3.3 V ± 0.3 V	1.2	2.2	3.2	1.1	4	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		20.5	13.7			ns
			1.2 V ± 0.1 V	4.6	8.4	9.3	3.6	16.6	
			1.5 V ± 0.1 V	3.5	5.9	7.5	2.4	11.1	
			1.8 V ± 0.15 V	3.9	4.7	5.3	1.3	9.1	
			2.5 V ± 0.2 V	2.3	3.4	4.3	1.6	6.4	
			3.3 V ± 0.3 V	2.1	2.8		1.4	5.2	
t_{en}	OE	Y	0.8 V		21.8	16.8			ns
			1.2 V ± 0.1 V	4.9	10.2	11.2	4.4	20.2	
			1.5 V ± 0.1 V	3.9	7.3	9.2	3.3	13.5	
			1.8 V ± 0.15 V	3.4	5.8	6.4	2.7	11	
			2.5 V ± 0.2 V	2.5	4.3	5.4	2.1	7.8	
			3.3 V ± 0.3 V	2.1	3.7		1.9	6.4	
t_{dis}	OE	Y	0.8 V		13				ns
			1.2 V ± 0.1 V	3.8	6.6	11.7	1.2	14	
			1.5 V ± 0.1 V	2.2	4.7	7.9	1.3	9.3	
			1.8 V ± 0.15 V	2.4	4.4	6.4	2.2	7.5	
			2.5 V ± 0.2 V	1.3	3.1	4.9	1.2	5.4	
			3.3 V ± 0.3 V	1.9	3.4	5	1.9	5.6	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		22.5				ns
			1.2 V ± 0.1 V	5.8	9.3	15.1	4.3	17.9	
			1.5 V ± 0.1 V	4.4	6.6	10.2	3	12.1	
			1.8 V ± 0.15 V	3.5	5.3	8.3	2.3	9.9	
			2.5 V ± 0.2 V	2.7	3.9	5.8	1.9	7	
			3.3 V ± 0.3 V	2.4	3.2	4.7	1.8	5.7	
t_{en}	OE	Y	0.8 V		25.2				ns
			1.2 V ± 0.1 V	7	11.3	18.1	5.4	21.4	
			1.5 V ± 0.1 V	5.5	8.1	12.2	4.1	14.5	
			1.8 V ± 0.15 V	4.3	6.5	10.1	3.3	12	
			2.5 V ± 0.2 V	3.4	4.8	7.1	2.6	8.4	
			3.3 V ± 0.3 V	2.9	4.1	5.9	2.3	6.9	
t_{dis}	OE	Y	0.8 V		14				ns
			1.2 V ± 0.1 V	3.7	5.8	8.2	3.3	11	
			1.5 V ± 0.1 V	5.5	3.9	5.9	2.1	8	
			1.8 V ± 0.15 V	3.3	4.5	6.6	2.9	7.4	
			2.5 V ± 0.2 V	2.3	3.2	4.3	1.8	5.1	
			3.3 V ± 0.3 V	2.4	4.8	6.2	3.1	6.7	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C MIN	TYP	MAX	T_A = –40°C to 85°C MIN	MAX	UNIT
t_{pd}	A or B	Y	0.8 V		29				ns
			1.2 V ± 0.1 V	7.4	12	18.7	6.6	21.4	
			1.5 V ± 0.1 V	5.7	8.6	12.5	4.9	14.7	
			1.8 V ± 0.15 V	4.8	6.9	10.1	3.1	12	
			2.5 V ± 0.2 V	3.9	5.1	7.2	3.3	8.7	
			3.3 V ± 0.3 V	3.5	4.8	6	3	7	
t_{en}	OE	Y	0.8 V		33.4				ns
			1.2 V ± 0.1 V	8.8	14.1	21.8	7.4	25.5	
			1.5 V ± 0.1 V	6.9	10.1	14.6	5.6	17.4	
			1.8 V ± 0.15 V	5.6	8.1	12	4.7	14.1	
			2.5 V ± 0.2 V	4.3	6.1	8.5	3.8	10	
			3.3 V ± 0.3 V	3.7	5.2	7.1	3.4	8.3	
t_{dis}	OE	Y	0.8 V		17.7				ns
			1.2 V ± 0.1 V	5.8	10	16	3.7	16	
			1.5 V ± 0.1 V	5.7	7.7	10.9	1	10.7	
			1.8 V ± 0.15 V	4.5	7.7	9.8	4.4	12.5	
			2.5 V ± 0.2 V	3.9	5.6	7.4	3.2	9	
			3.3 V ± 0.3 V	3.3	8.4	10.7	6.6	10.8	

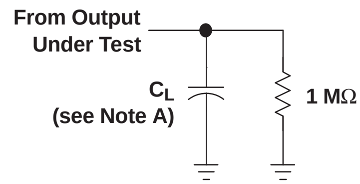
OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	0.8 V	3.8	pF
				1.2 V ± 0.1 V	3.7	
				1.5 V ±0.1 V	3.7	
				1.8 V ± 0.15 V	3.7	
				2.5 V ± 0.2 V	3.9	
				3.3 V ± 0.3 V	4	
		Outputs disable	f = 10 MHz	0.8 V	0	
				1.2 V ± 0.1 V	0	
				1.5 V ±0.1 V	0	
				1.8 V ± 0.15 V	0	
				2.5 V ± 0.2 V	0	
				2.5 V ± 0.2 V	0	
				3.3 V ± 0.3 V	0	

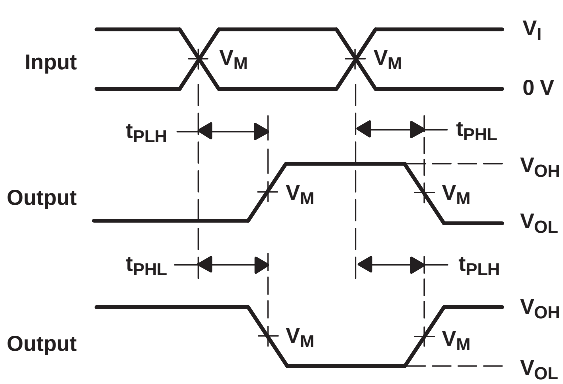
PARAMETER MEASUREMENT INFORMATION

(Propagation Delays, Setup and Hold Times, and Pulse Width)

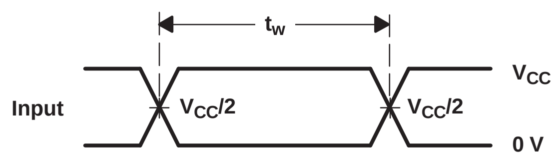


LOAD CIRCUIT

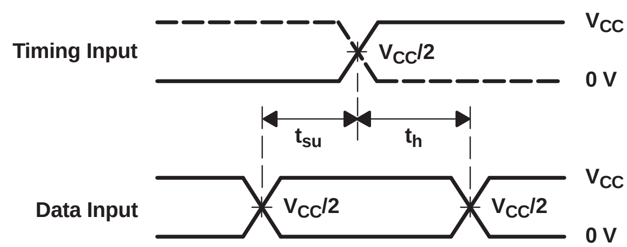
	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION



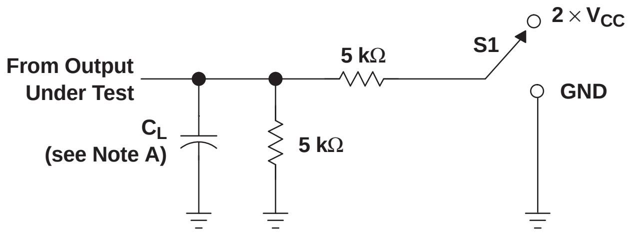
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

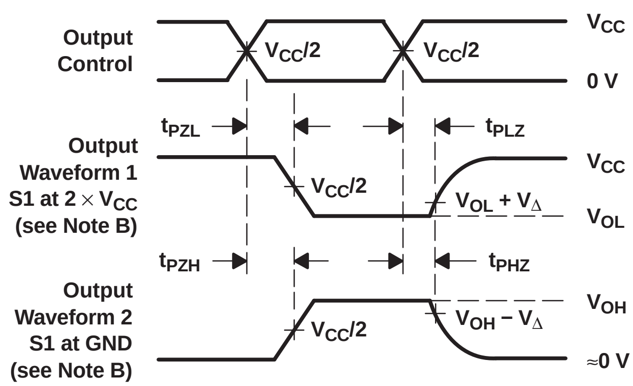
(Enable and Disable Times)



LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AUP1G126DRLRG4	ACTIVE	SOT-OTHER	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HN7 ~ HNR)	Samples
SN74AUP1G126DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H26R	Samples
SN74AUP1G126DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H26R	Samples
SN74AUP1G126DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HN5 ~ HNF ~ HNK ~ HNR)	Samples
SN74AUP1G126DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HN5 ~ HNR)	Samples
SN74AUP1G126DRLR	ACTIVE	SOT-OTHER	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HN7 ~ HNR)	Samples
SN74AUP1G126DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HN	Samples
SN74AUP1G126DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HN	Samples
SN74AUP1G126YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		HNN	Samples
SN74AUP1G126YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(HN7 ~ HNN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

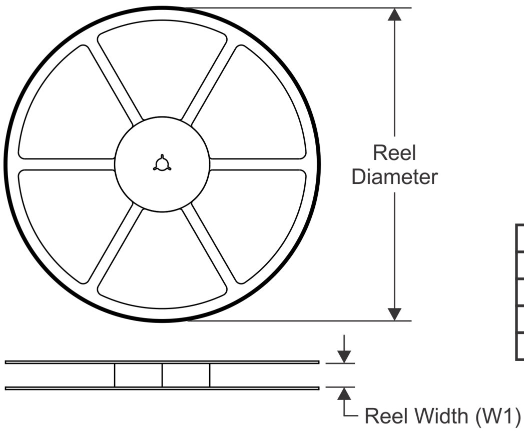
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

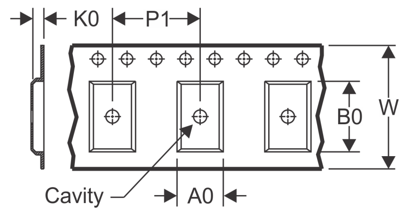
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

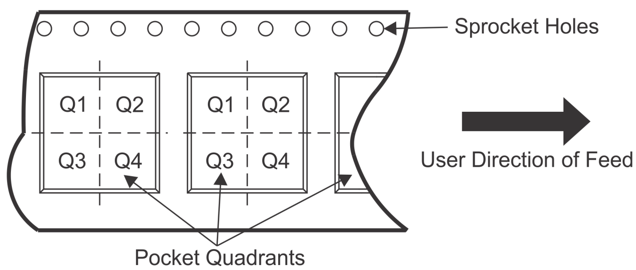


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

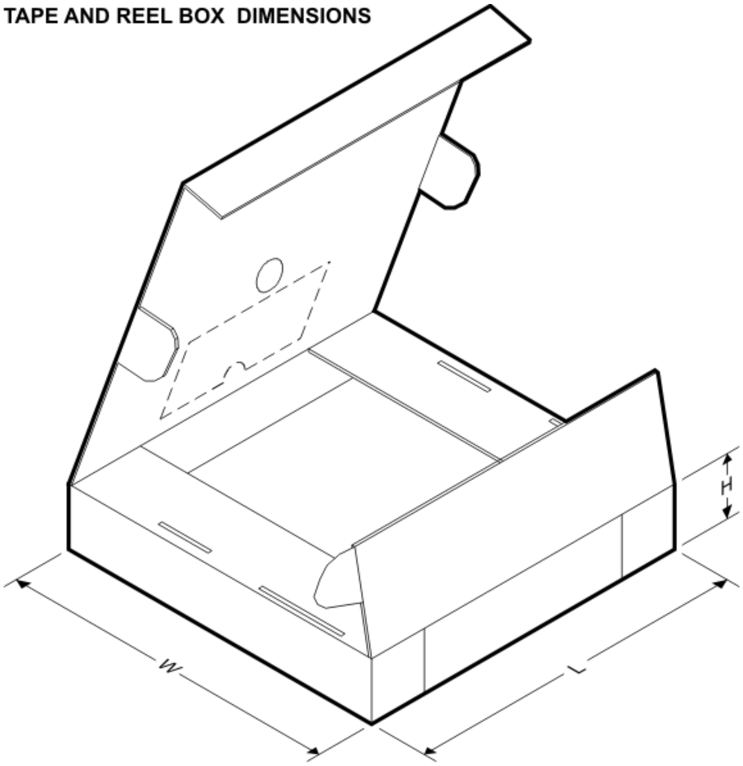
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G126DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G126DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G126DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G126DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G126DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G126DRLR	SOT-OTHER	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G126DRLR	SOT-OTHER	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G126DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G126DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP1G126DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G126YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G126YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

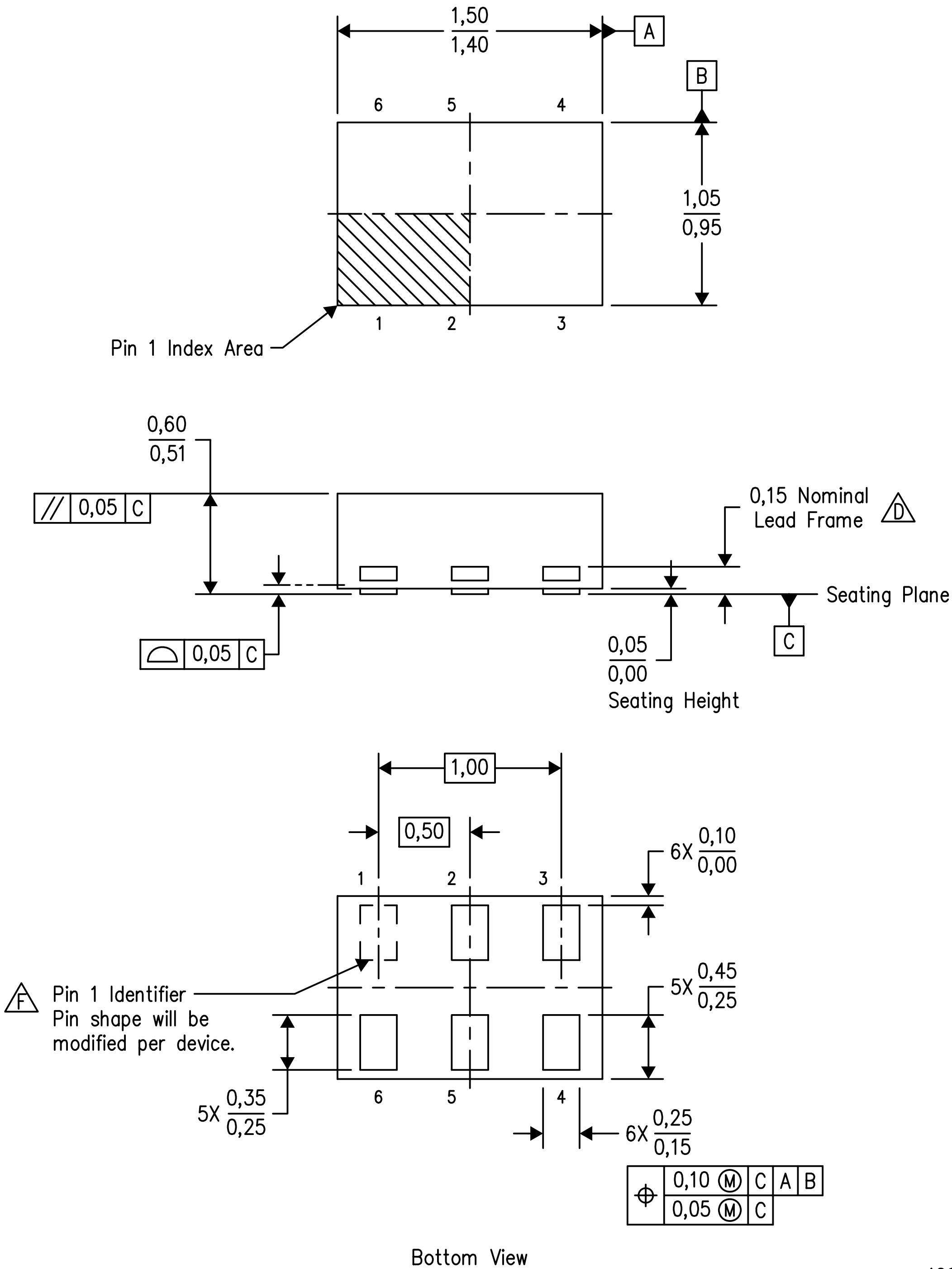
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G126DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G126DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G126DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G126DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AUP1G126DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G126DRLR	SOT-OTHER	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G126DRLR	SOT-OTHER	DRL	5	4000	184.0	184.0	19.0
SN74AUP1G126DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G126DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP1G126DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G126YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G126YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

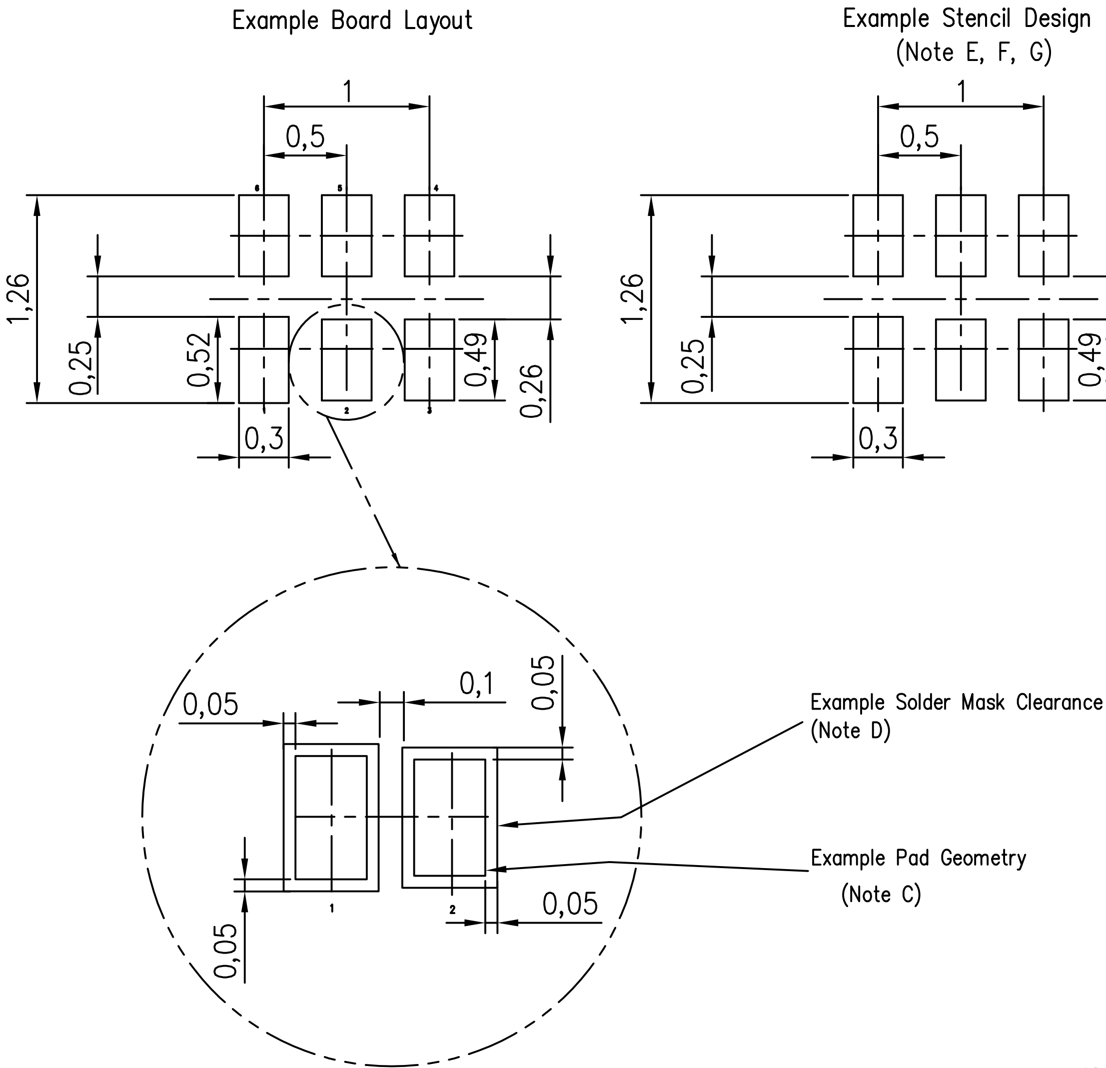
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4207181/F 12/11

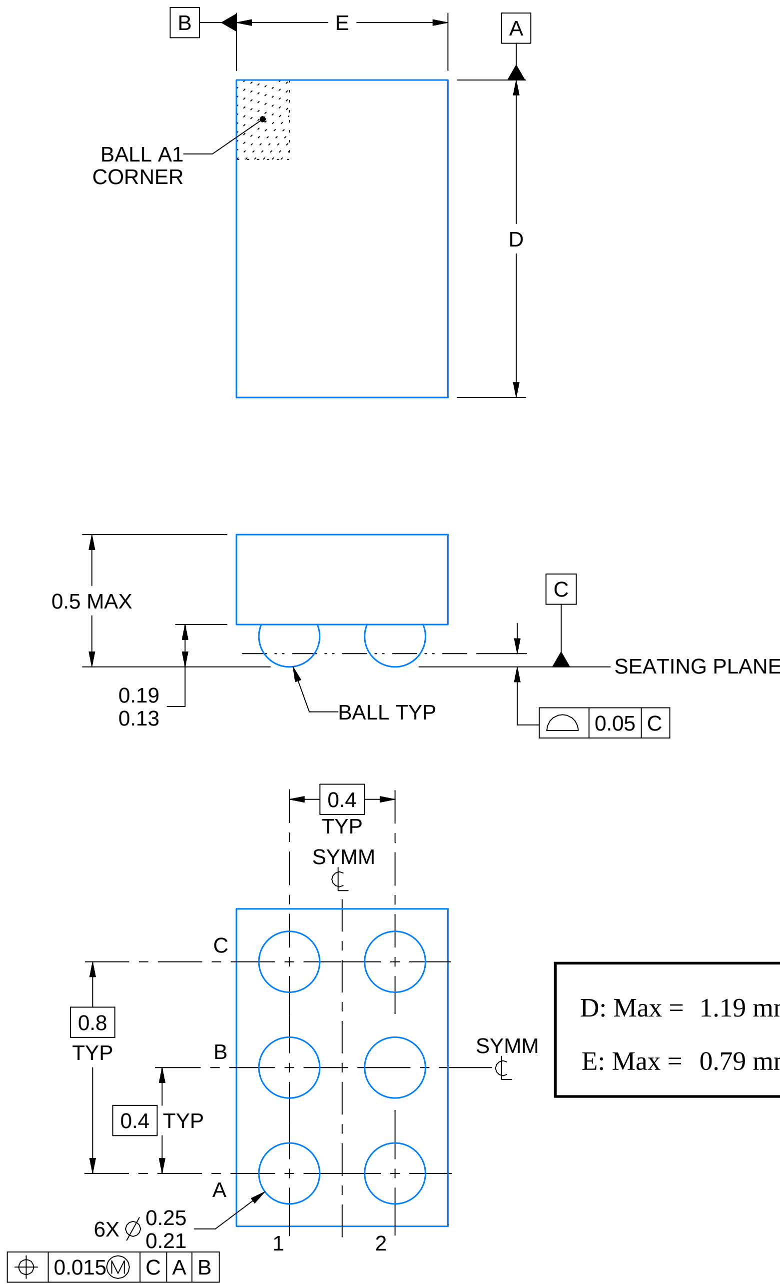
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4208310/E 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

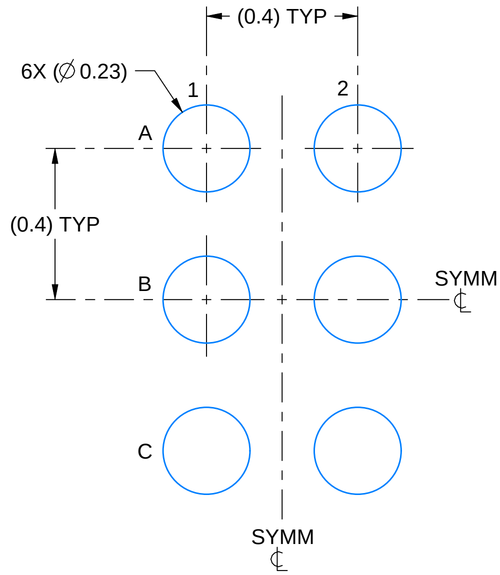


D: Max = 1.19 mm, Min = 1.13 mm	
E: Max = 0.79 mm, Min = 0.73 mm	

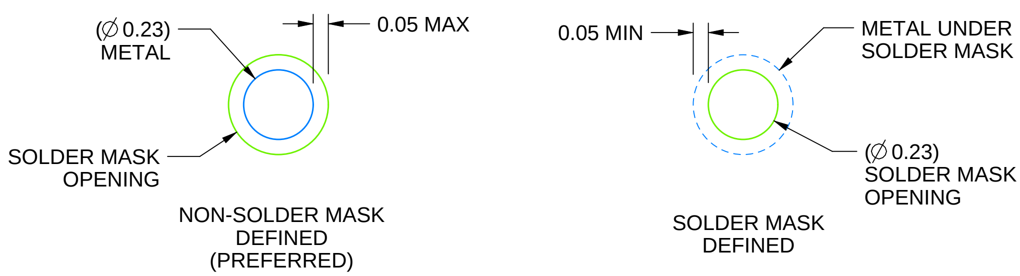
4223410/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:50X

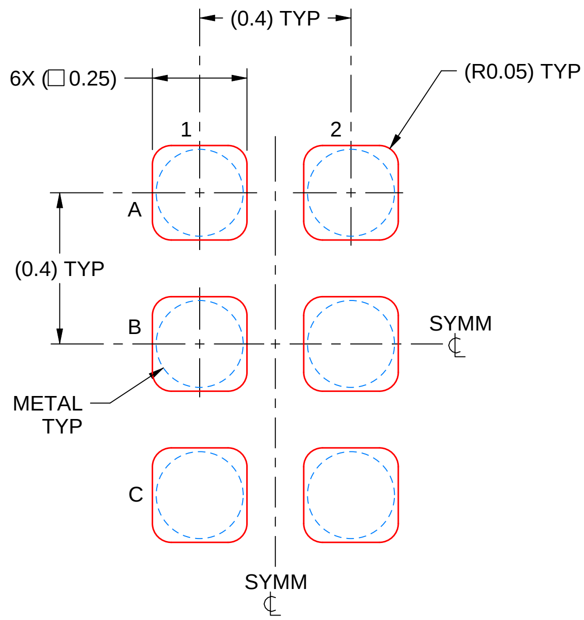


SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

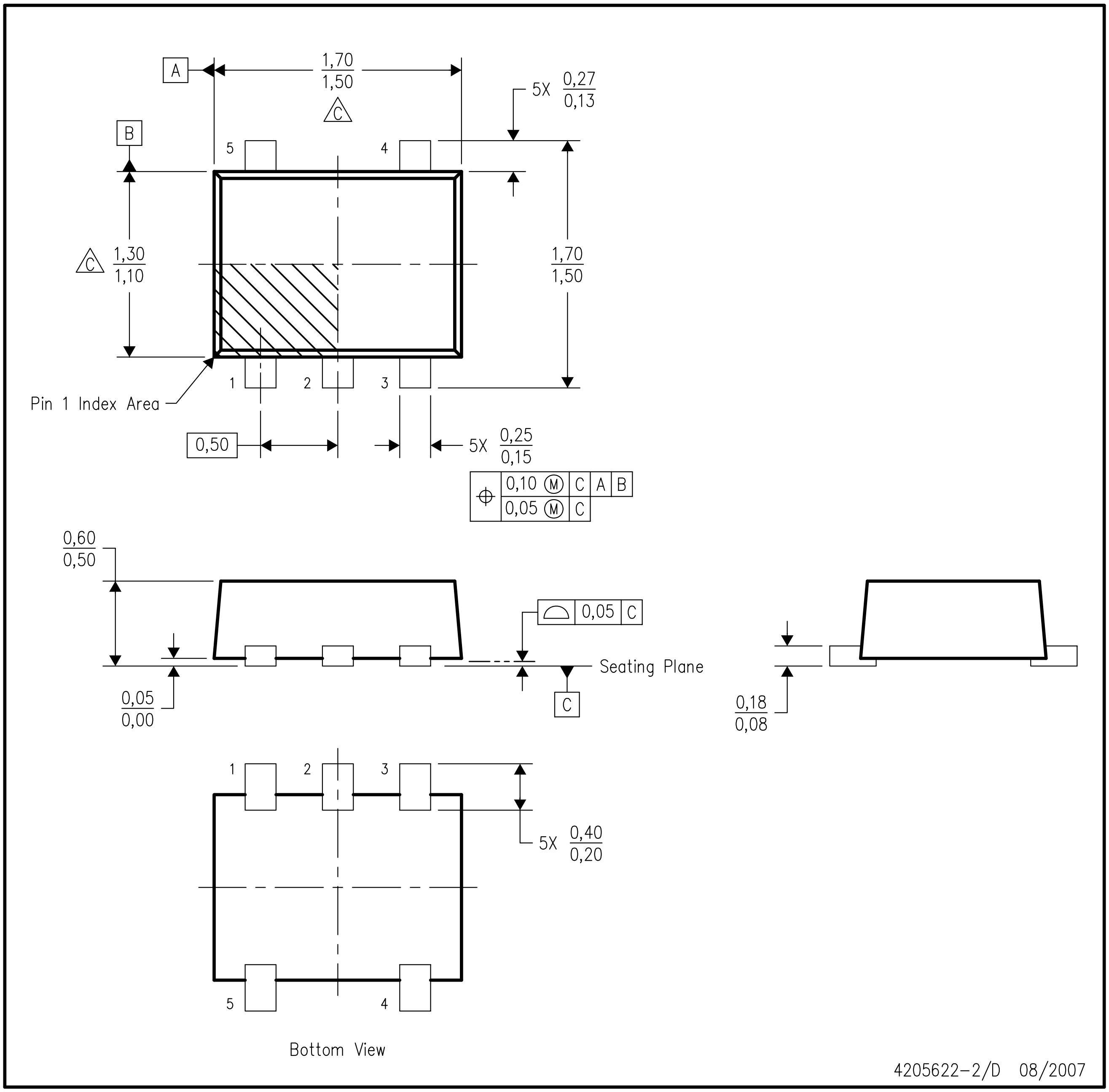


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

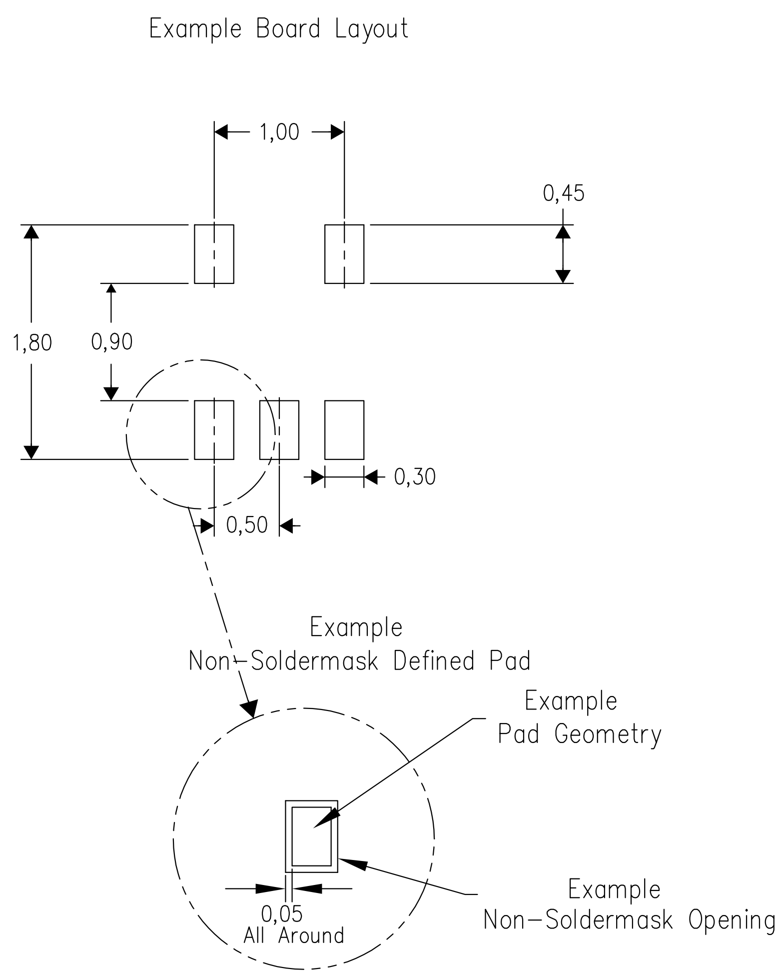
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

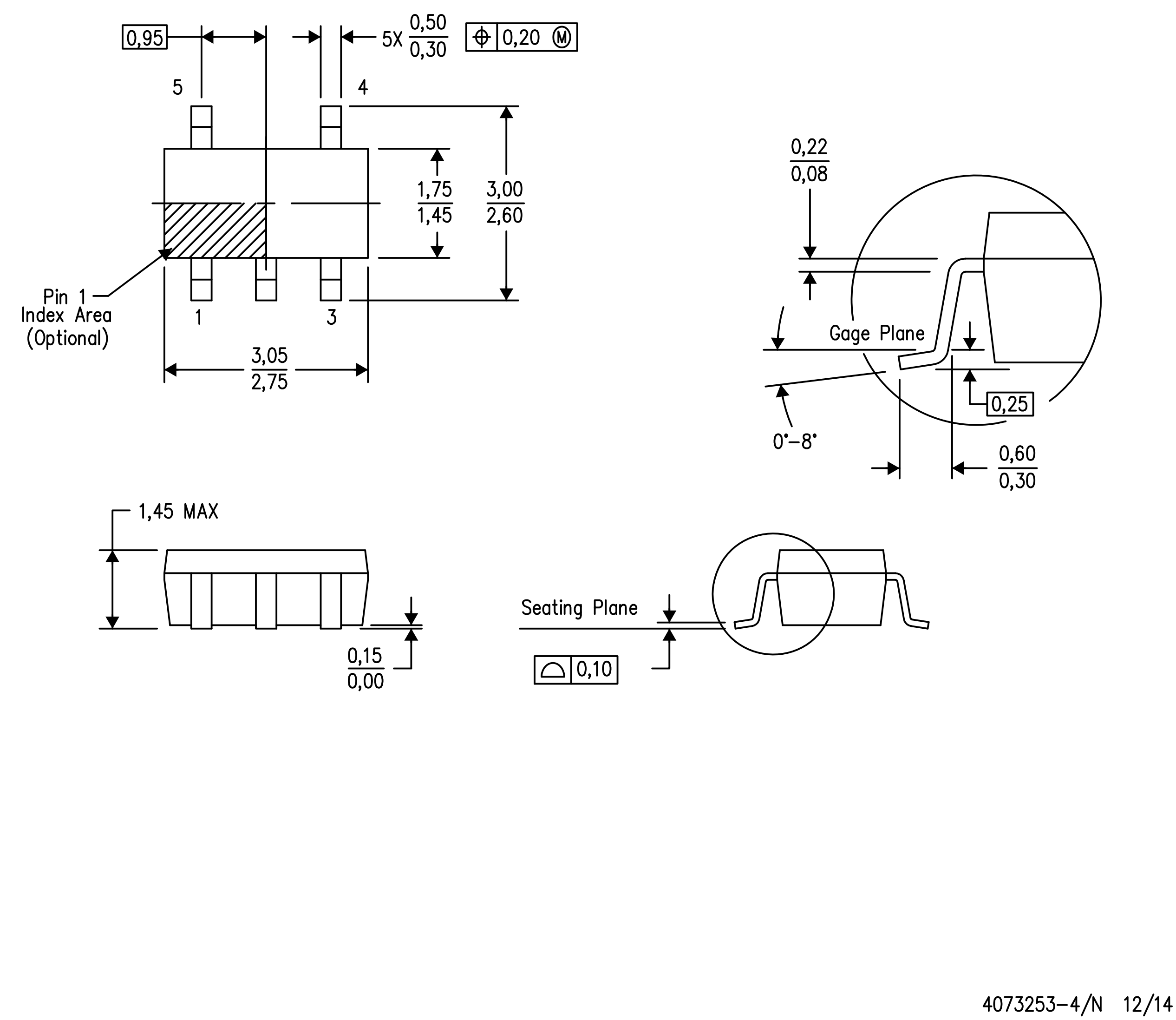
DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE



4208207–2/E 06/12

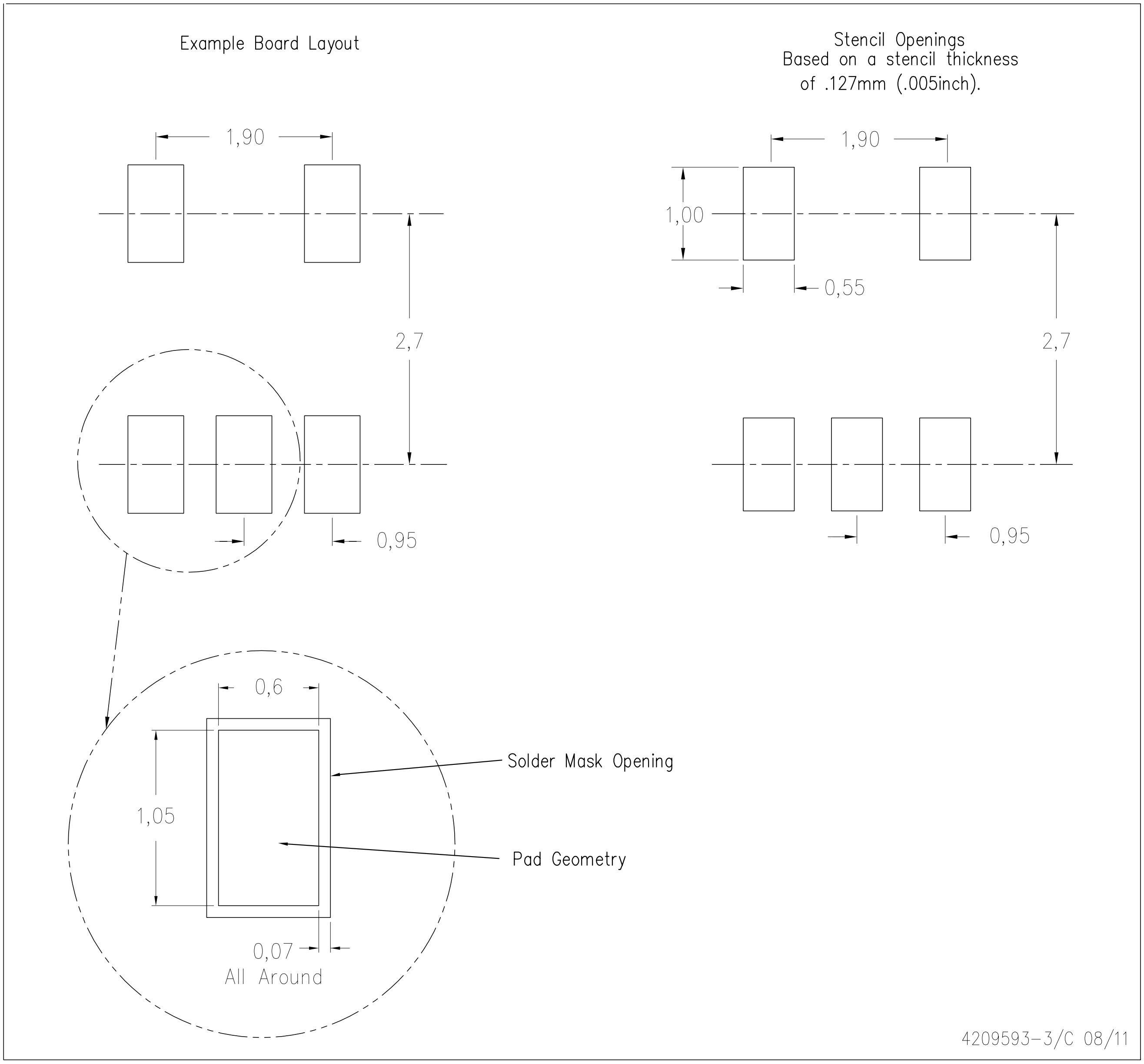
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



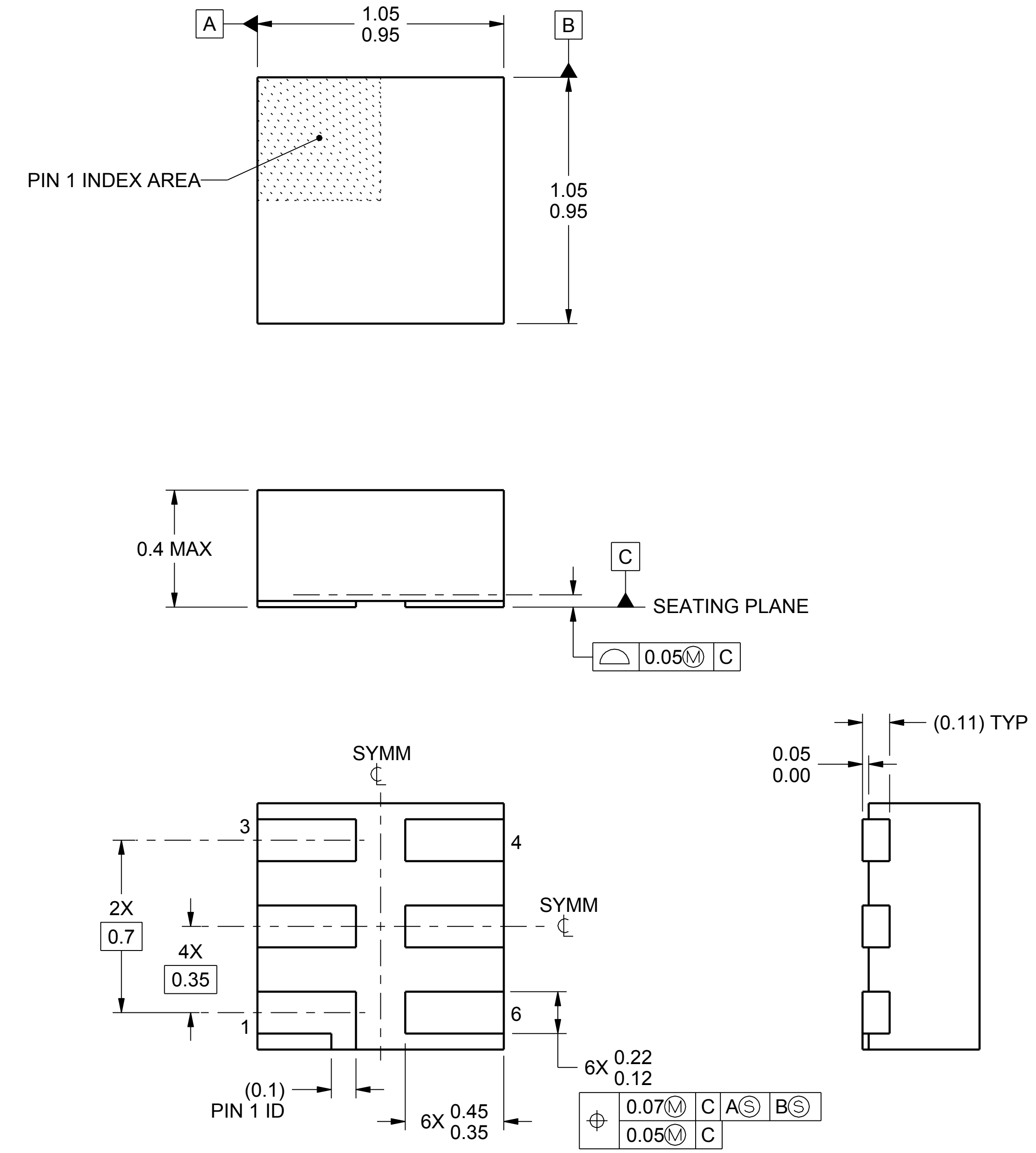
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DSF (S-PX2SON-N6) PLASTIC SMALL OUTLINE NO-LEAD

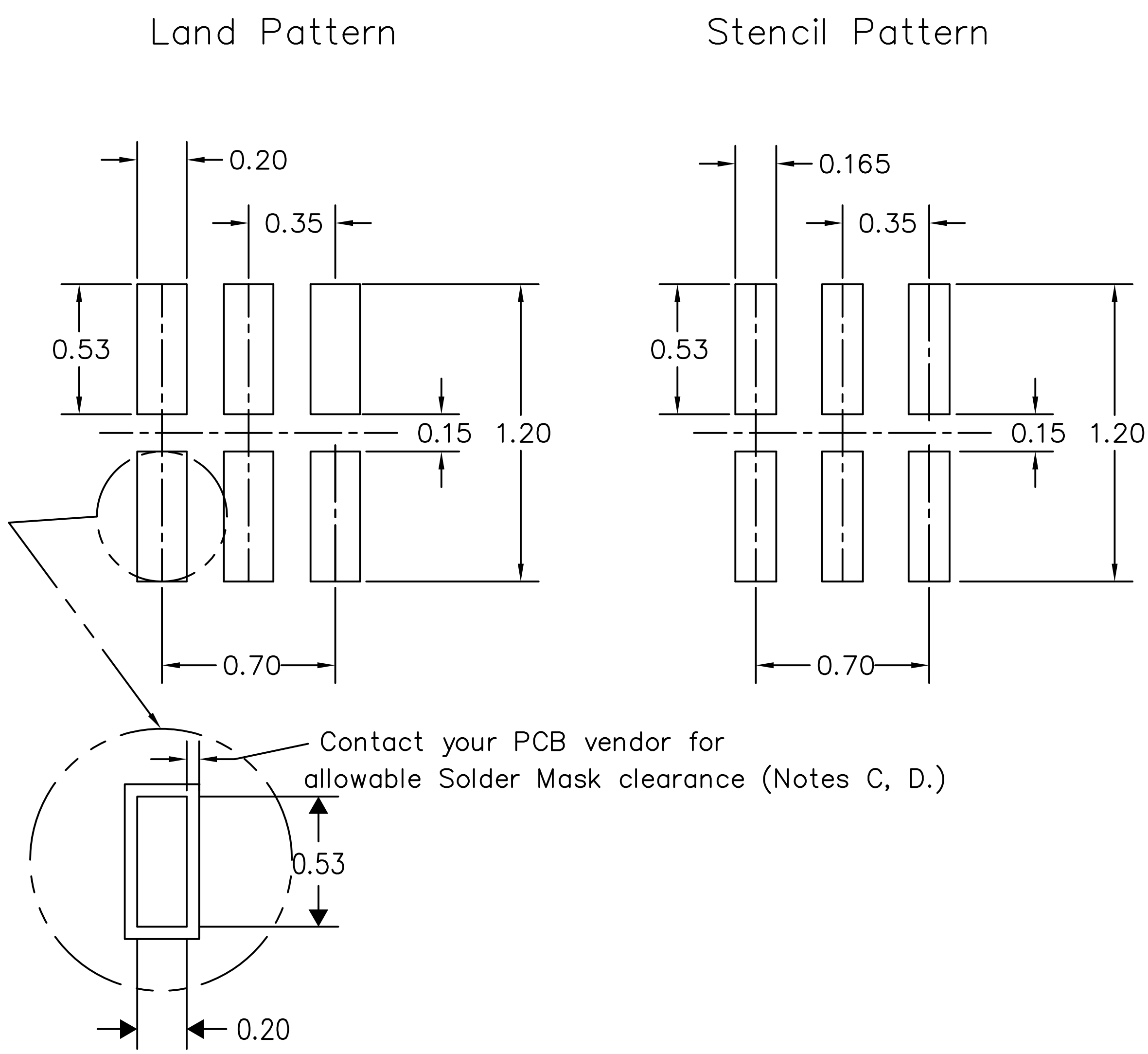


4208186/F 10/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

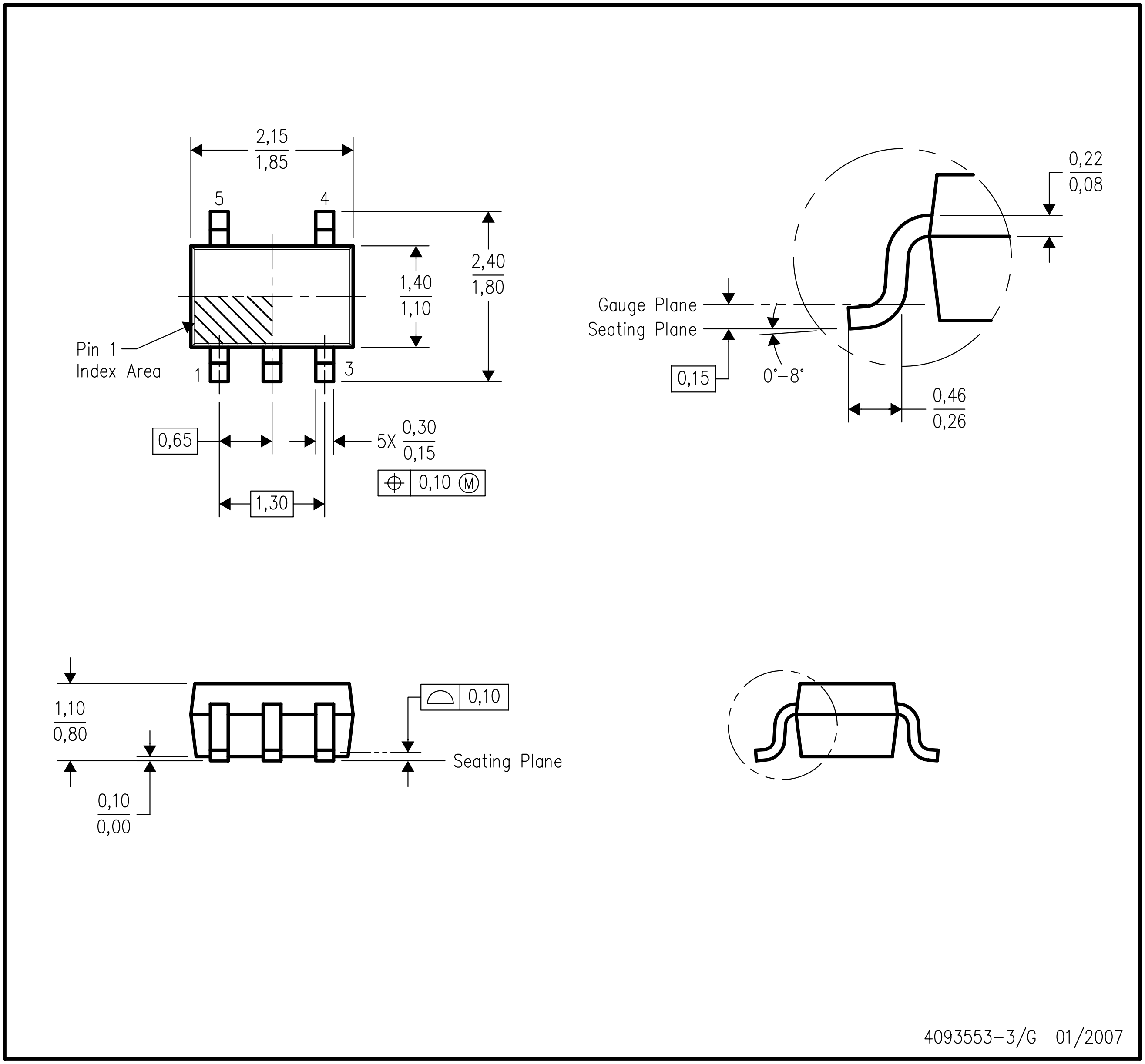
DSF (S-PX2SON-N6) PLASTIC SMALL OUTLINE NO-LEAD



4210277/D 05/12

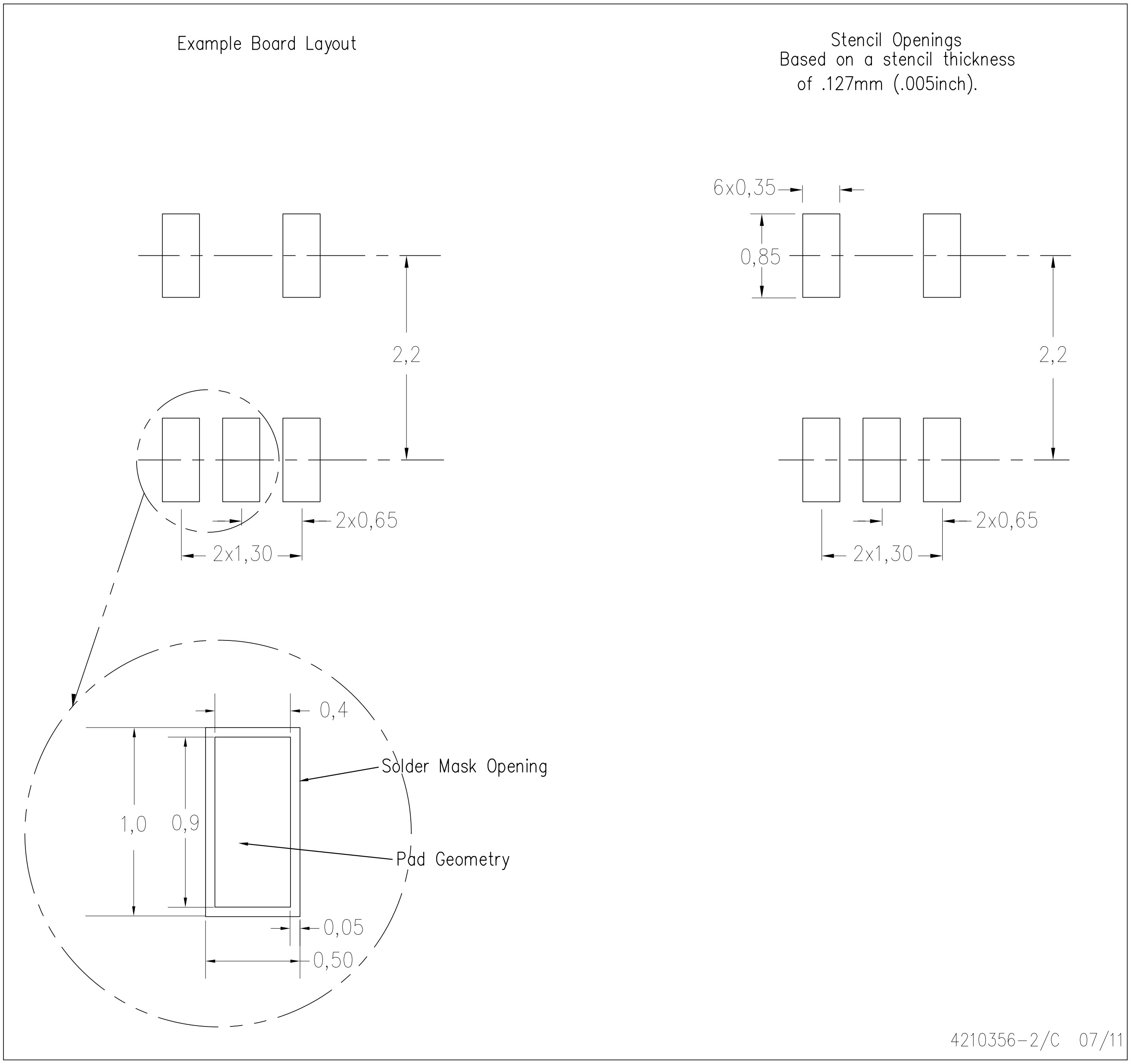
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- H. Component placement force should be minimized to prevent excessive paste block deformation.

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



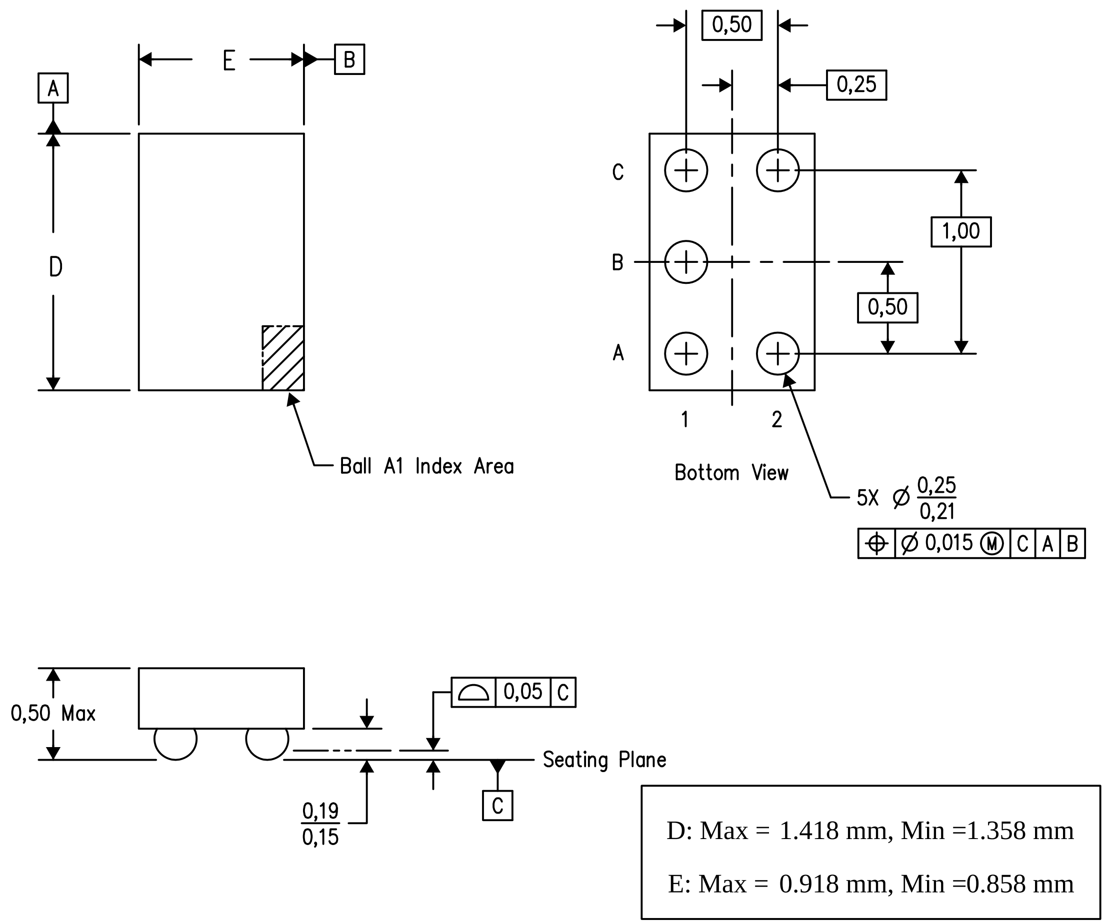
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

YZP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



4204741–3/M 11/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265