

## TPS51200 Sink and Source DDR Termination Regulator

### 1 Features

- Input Voltage: Supports 2.5-V Rail and 3.3-V Rail
- VLDOIN Voltage Range: 1.1 V to 3.5 V
- Sink and Source Termination Regulator Includes Droop Compensation
- Requires Minimum Output Capacitance of 20- $\mu$ F (Typically 3  $\times$  10- $\mu$ F MLCCs) for Memory Termination Applications (DDR)
- PGOOD to Monitor Output Regulation
- EN Input
- REFIN Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider
- Remote Sensing (VOSNS)
- $\pm$ 10-mA Buffered Reference (REFOUT)
- Built-in Soft Start, UVLO, and OCL
- Thermal Shutdown
- Supports DDR, DDR2, DDR3, DDR3L, Low-Power DDR3, and DDR4 VTT Applications
- 10-Pin VSON Package With Thermal Pad

### 2 Applications

- Memory Termination Regulator for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4
- Notebooks, Desktops, and Servers
- Telecom and Datacom
- Base Stations
- LCD-TVs and PDP-TVs
- Copiers and Printers
- Set-Top Boxes

### 3 Description

The TPS51200 device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration.

The TPS51200 maintains a fast transient response and requires a minimum output capacitance of only 20  $\mu$ F. The TPS51200 supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4 VTT bus termination.

In addition, the TPS51200 provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications.

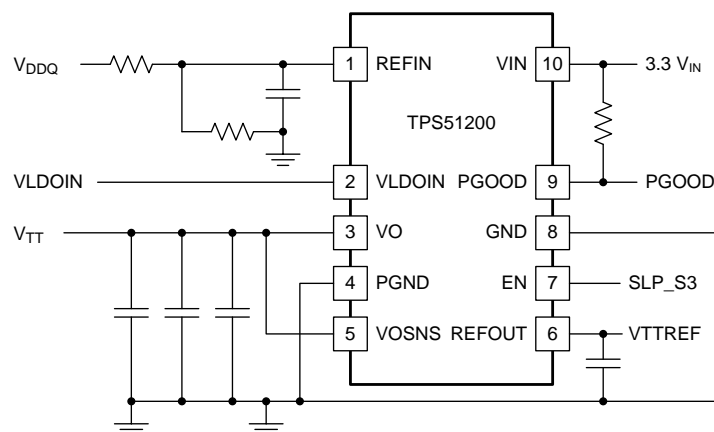
The is available in the thermally efficient 10-pin VSON thermal pad package, and is rated both Green and Pb-free. It is specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS51200	VSON (10)	3.00 mm $\times$ 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified DDR Application



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (September 2016) to Revision C</b>	<b>Page</b>
• Added references to DDR3L DRAM technology throughout.....	<b>1</b>

<b>Changes from Revision A (September 2015) to Revision B</b>	<b>Page</b>

<b>Changes from Original (February 2008) to Revision A</b>	<b>Page</b>
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes, Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....	<b>1</b>

## 5 Device and Documentation Support

### 5.1 Device Support

#### 5.1.1 Third-Party Products Disclaimer

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#### 5.1.2 Development Support

##### 5.1.2.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS51200 device. The [TPS51200EVM](#) evaluation module and related user's guide ([SLUU323](#)) can be requested at the Texas Instruments website through the product folders or purchased directly from the [TI eStore](#).

##### 5.1.2.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS51200 device is available [here](#).

### 5.2 Documentation Support

#### 5.2.1 Related Documentation

- *Using New Thermal Metrics*, [SBVA025](#)
- *Semiconductor and IC Package Thermal Metrics*, [SPRA953](#)
- *Using the TPS51200 EVM Sink/Source DDR Termination Regulator*, [SLUU323](#)
- For more information on the TPS51100 device, see the product folder on [ti.com](#).

### 5.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 5.4 Trademarks

E2E is a trademark of Texas Instruments.  
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### 5.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 5.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51200DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1200	<a href="#">Samples</a>
TPS51200DRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1200	<a href="#">Samples</a>
TPS51200DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1200	<a href="#">Samples</a>
TPS51200DRCTG4	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1200	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPS51200 :**

- Automotive: [TPS51200-Q1](#)
- Enhanced Product: [TPS51200-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51200DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51200DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**

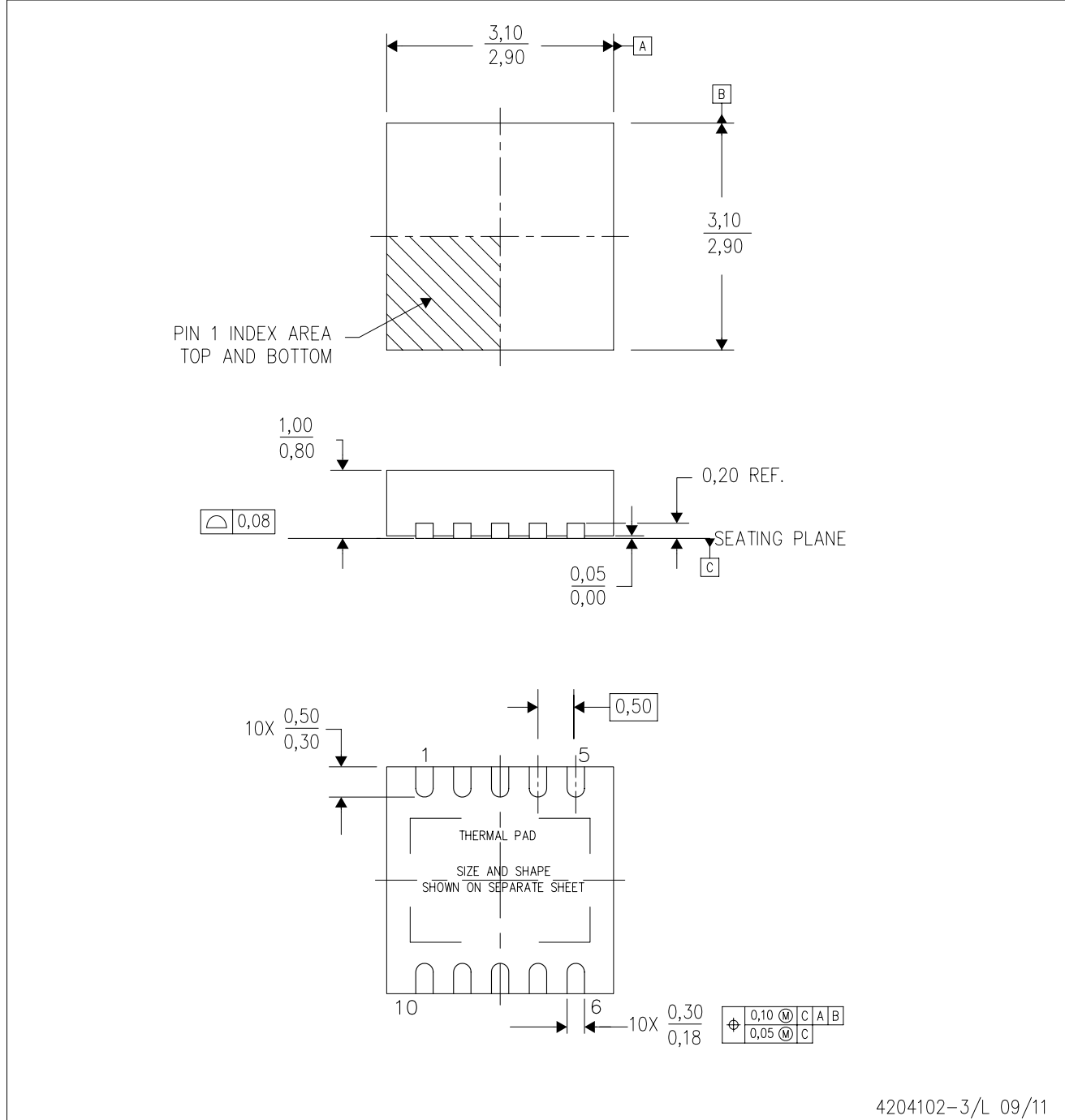

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51200DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS51200DRCT	VSON	DRC	10	250	210.0	185.0	35.0



DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



4204102-3/L 09/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

# THERMAL PAD MECHANICAL DATA

DRC (S-PVSON-N10)

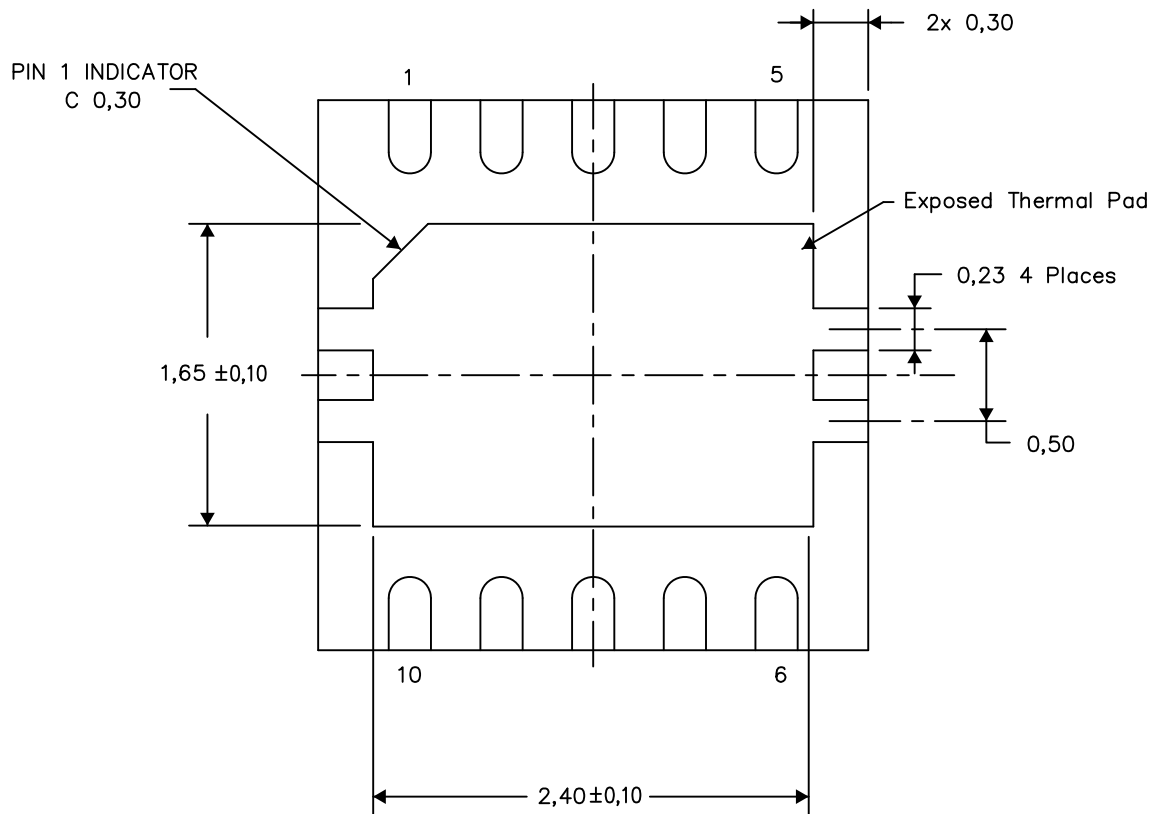
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206565-3/Y 08/15

NOTE: A. All linear dimensions are in millimeters



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