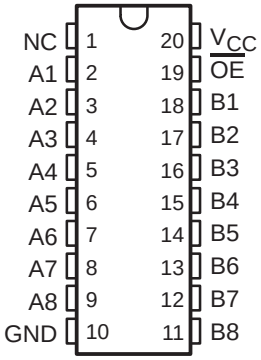
SCDS034F – JULY 1997 – REVISED MAY 1998

- **Standard ’245-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **Isolation Under Power-Off Conditions**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN74CBTLV3245 provides eight bits of high-speed bus switching in a standard ’245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 8-bit switch. When output enable ($\overline{OE}$) is low, the 8-bit bus switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

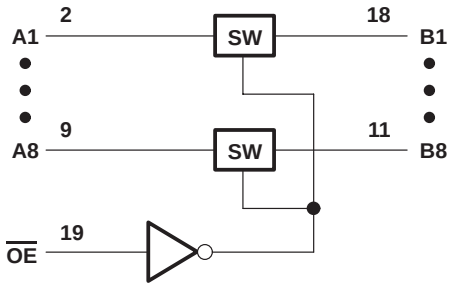
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV3245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

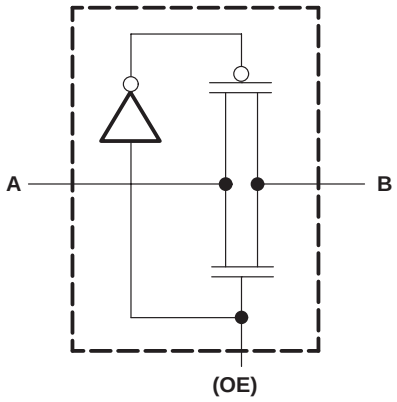
INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 4.6 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 115°C/W
DGV package . . . . . 146°C/W
DW package . . . . . 97°C/W
PW package . . . . . 128°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = –18 mA				–0.8	V
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±50	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				30	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			20	µA
ΔI_{CC}‡	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			750	µA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			8		pF
r_{on}§		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		¶	¶	Ω
				I_I = 24 mA		¶	¶	
			V_I = 1.7 V,	I_I = 15 mA		¶	¶	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

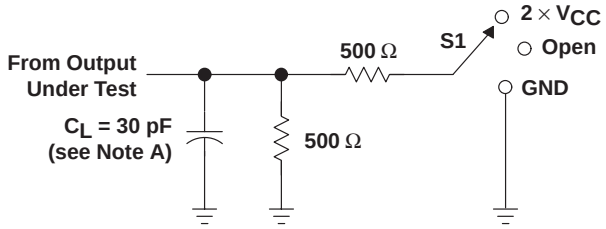
† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.
¶ This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}#	A or B	B or A		¶		0.25	ns
t_{en}	$\overline{OE}$	A or B	¶	¶	1	5.6	ns
t_{dis}	$\overline{OE}$	A or B	¶	¶	1	6.5	ns

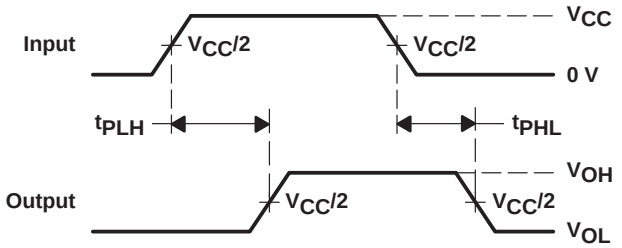
¶ This information was not available at the time of publication.
# The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

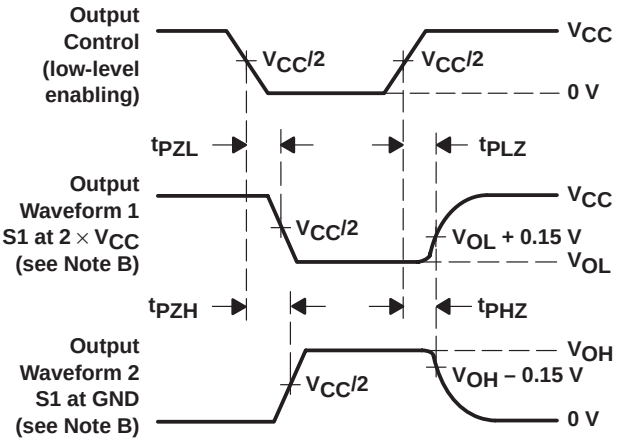


LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

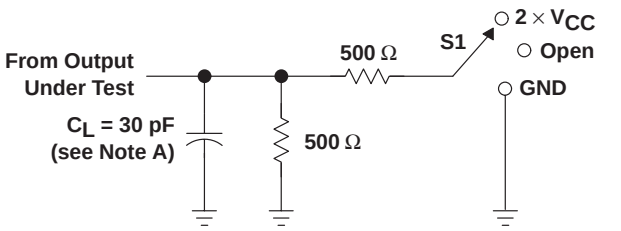


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3 V ± 0.3 V



LOAD CIRCUIT

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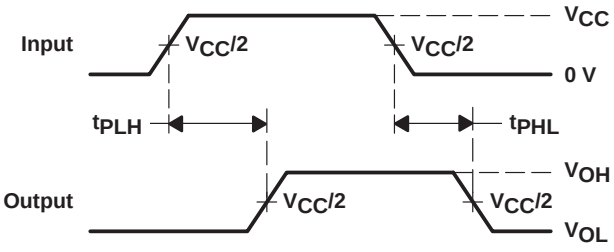
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND



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PROPAGATION DELAY TIMES

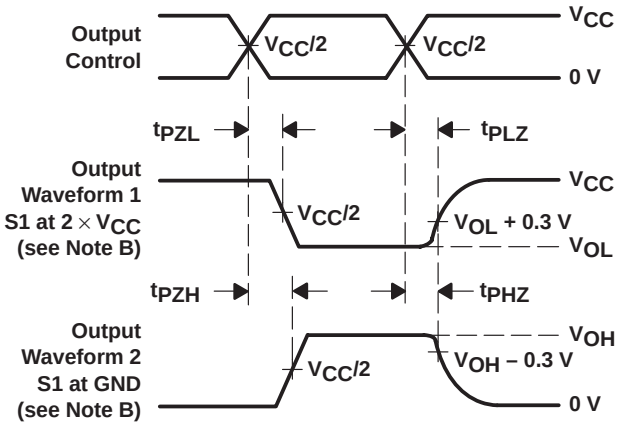

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Figure 2. Load Circuit and Voltage Waveforms

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PRODUCT FOLDER | PRODUCT INFO: FEATURES | DESCRIPTION | DATASHEETS | PRICING/AVAILABILITY | SAMPLES | APPLICATION NOTES | RELATED DOCUMENTS

PRODUCT SUPPORT: TRAINING

SN74CBTLV3245, Low-Voltage Octal FET Bus Switch

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74CBTLV3245
Voltage Nodes (V)	3.3
Vcc range (V)	2.3 to 3.6
No. of Bits	8
ron(max) (ohms)	7
tpd(max) (ns)	0.25

FEATURES

Back to Top

- Standard '245-Type Pinout
- 5- Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

DESCRIPTION

Back to Top

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The device is organized as one 8-bit switch. When output enable (OE\) is low, the 8-bit bus switch is on and
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To ensure the high-impedance state during power up or power down, OE\ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-

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The SN74CBTLV3245 is characterized for operation from -40°C to 85°C.

TECHNICAL DOCUMENTS

Back to Top

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To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Back to Top

Full datasheet in Acrobat PDF: scds034f.pdf (79 KB) (Updated: 05/19/1998)
Full datasheet in Zipped PostScript: scds034f.psz (83 KB)

APPLICATION NOTES

Back to Top

View Application Reports for Digital Logic

- 5-V To 3.3-V Translation With The SN74CBTD3384 (SCDA003B - Updated: 03/01/1997)
- Low-Voltage Bus-Switch Technology And Applications (SCDA005 - Updated: 12/01/1997)
- SN74CBTS3384 Bus Switches Provide Fast Connection And Ensure Isolation (SCDA002A - Updated: 08/01/1996)
- TI Logic Solutions for Memory Interleaving With the Intel440BX Chipset (SCCA001 - Updated: 04/08/1999)
- Texas Instruments Crossbar Switches (SCDA001A - Updated: 06/01/1995)
- Texas Instruments Solution for Undershoot Protection for Bus Switches (SCDA007 - Updated: 04/13/2000)

RELATED DOCUMENTS

Back to Top

- Documentation Rules (SAP) And Ordering Information (SZZU001B, 4 KB - Updated: 05/06/1999)
- Logic Selection Guide Second Half 2000 (SDYU001N, 5035 KB - Updated: 04/17/2000)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- More Power In Less Space - Technical Article (SCAU001A, 850 KB - Updated: 03/01/1996)

SAMPLES

Back to Top

ORDERABLE DEVICE	PACKAGE	PINS	TEMP (°C)	STATUS	SAMPLES
SN74CBTLV3245PWLE	PW	20	-40 TO 85	OBSOLETE	
SN74CBTLV3245PWR	PW	20	-40 TO 85	ACTIVE	Request Samples

PRICING/AVAILABILITY

Back to Top

ORDERABLE DEVICE	PACKAGE	PINS	TEMP (°C)	STATUS	BUDGETARY PRICE US$/UNIT QTY=1000+	PACK QTY	PRICING/AVAILABILITY
SN74CBTLV3245DBLE	DB	20	-40 TO 85	OBSOLETE			
SN74CBTLV3245DBR	DB	20	-40 TO 85	ACTIVE	1.00	2000	Check stock or order
SN74CBTLV3245DGVR	DGV	20	-40 TO 85	ACTIVE	1.17	2000	Check stock or order

SN74CBTLV3245PWLE	PW	20	-40 TO 85	OBSOLETE			
SN74CBTLV3245PWR	PW	20	-40 TO 85	ACTIVE	1.00	2000	Check stock or order

Table Data Updated on: 11/15/2000