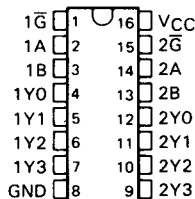


SN54LS139A, SN54S139, SN74LS139A, SN74S139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

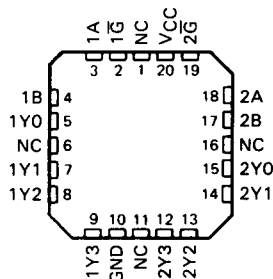
DECEMBER 1972 - REVISED MARCH 1988

- Designed Specifically for High-Speed: Memory Decoders Data Transmission Systems
- Two Fully Independent 2- to 4-Line Decoders/Demultiplexers
- Schottky Clamped for High Performance

SN54LS139A, SN54S139 . . . J OR W PACKAGE
SN74LS139A, SN74S139A . . . D OR N PACKAGE
(TOP VIEW)



SN54LS139A, SN54S139 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The circuit comprises two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

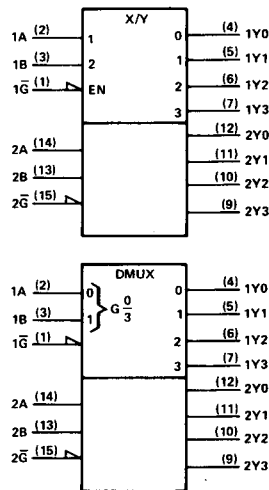
All of these decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design. The SN54LS139A and SN54S139 are characterized for operation range of -55°C to 125°C . The SN74LS139A and SN74S139A are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

| INPUTS | | | OUTPUTS | | | |
|-----------|--------|---|---------|----|----|----|
| ENABLE | SELECT | | Y0 | Y1 | Y2 | Y3 |
| \bar{G} | B | A | | | | |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

H = high level, L = low level, X = irrelevant

logic symbols (alternatives)[†]



[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

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TTL Devices

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TEXAS
INSTRUMENTS

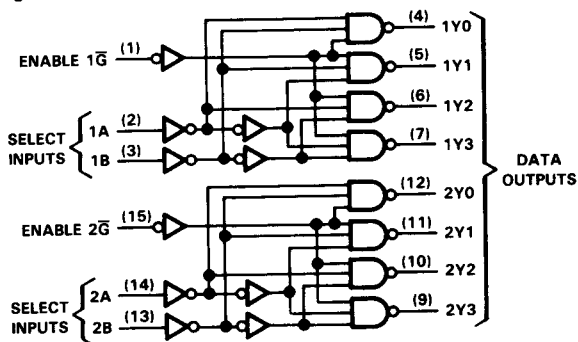
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SN54LS139A, SN54S139, SN74LS139A, SN74S139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

logic diagram (positive logic)

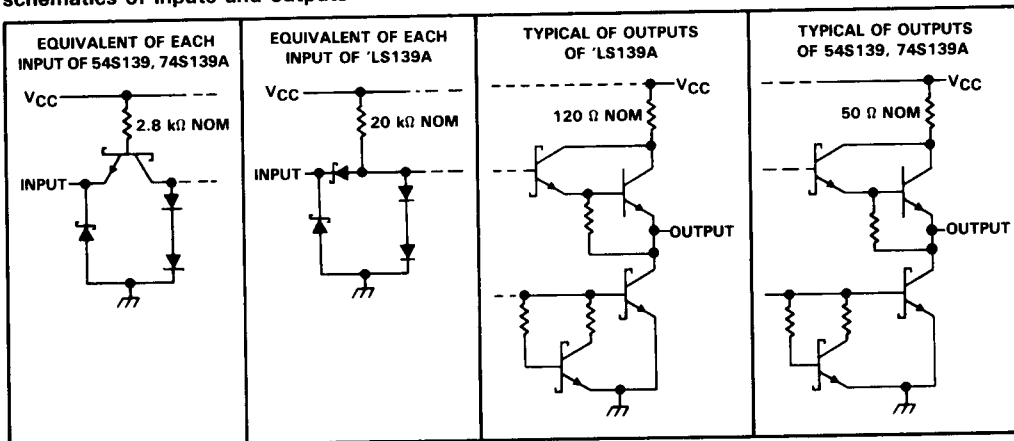


Pin numbers shown are for D, J, N, and W packages.

2

schematics of inputs and outputs

TTL Devices



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--|----------------|
| Supply voltage, V_{CC} (See Note 1) | 7 V |
| Input voltage: 'LS139A | 7 V |
| 54S139, 74S139A | 5.5 V |
| Operating free-air temperature range: SN54LS139A, SN54S139 | -55°C to 125°C |
| SN74LS139A, SN74S139A | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

SN54LS139A, SN74LS139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

recommended operating conditions

| | | SN54LS139A | | | SN74LS139A | | | UNIT | | |
|-----------------|--------------------------------|------------|-----|-----|------------|-----|------|------|----|----|
| | | MIN | NOM | MAX | MIN | NOM | MAX | | | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V | | |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V | | |
| V _{IL} | Low-level input voltage | | | | | | | 0.8 | | |
| I _{OH} | High-level output current | -0.4 | | | -0.4 | | | mA | | |
| I _{OL} | Low-level output current | 4 | | | 8 | | | mA | | |
| T _A | Operating free-air temperature | -55 | | | 125 | | | 0 | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS [†] | | SN54LS139A | | | SN74LS139A | | | UNIT |
|------------------------------|--|--|------------------------|------------------|------|------------|------------------------|-----|------|
| | | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | |
| V _{IK} | V _{CC} = MIN, I _I = -18 mA | | -1.5 | | | -1.5 | | | V |
| V _{OH} | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA | | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V _{OL} | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX | | I _{OL} = 4 mA | | 0.25 | 0.4 | I _{OL} = 8 mA | | V |
| I _I | V _{CC} = MAX, V _I = 7 V | | 0.1 | | | 0.1 | | | mA |
| I _{IH} | V _{CC} = MAX, V _I = 2.7 V | | 20 | | | 20 | | | μA |
| I _{IL} | V _{CC} = MAX, V _I = 0.4 V | | -0.4 | | | -0.4 | | | mA |
| I _{OS} [§] | V _{CC} = MAX | | -20 | -100 | | -20 | -100 | | mA |
| I _{CC} | V _{CC} = MAX, Outputs enabled and open | | 6.8 | | 11 | 6.8 | | 11 | mA |

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 2)

| PARAMETER [†] | FROM (INPUT) | TO (OUTPUT) | LEVELS OF DELAY | TEST CONDITIONS | SN54LS139A SN74LS139A | | | UNIT |
|------------------------|---------------|-------------|-----------------|---|--------------------------|-----|-----|------|
| | | | | | MIN | TYP | MAX | |
| t _{PLH} | Binary Select | Any | 2 | R _L = 2 kΩ, C _L = 15 pF | 13 | | 20 | ns |
| t _{PHL} | | | | | 22 | | 33 | ns |
| t _{PLH} | | | 18 | | 29 | ns | | |
| t _{PHL} | | | 25 | | 38 | ns | | |
| t _{PLH} | Enable | Any | 2 | | 16 | | 24 | ns |
| t _{PHL} | | | | | 21 | | 32 | ns |

[†] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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TTL Devices

SN54S139, SN74S139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLIERS

recommended operating conditions

| | | SN54S139 | | | SN74S139A | | | UNIT |
|-----------------|--------------------------------|----------|-----|-----|-----------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | | 0.8 | | | V |
| I _{OH} | High-level output current | | | | -1 | | | mA |
| I _{OL} | Low-level output current | | | | 20 | | | mA |
| T _A | Operating free-air temperature | -55 | | | 125 | | | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | | SN54S139 SN74S139A | | | UNIT |
|-------------------|--|--------|-----------------------|------|------|------|
| | | | MIN | TYP‡ | MAX | |
| V _{IK} | V _{CC} = MIN, I _I = -18 mA | | -1.2 | | | V |
| V _{OH} | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA | SN54S' | 2.5 | 3.4 | | V |
| | | SN74S' | 2.7 | 3.4 | | |
| V _{OL} | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA | | | 0.5 | | V |
| I _I | V _{CC} = MAX, V _I = 5.5 V | | | 1 | | mA |
| I _{IH} | V _{CC} = MAX, V _I = 2.7 V | | | 50 | | μA |
| I _{IL} | V _{CC} = MAX, V _I = 0.5 V | | | -2 | | mA |
| I _{OS} ‡ | V _{CC} = MAX | | | -40 | -100 | mA |
| I _{CC} | V _{CC} = MAX, Outputs enabled and open | | | 60 | 90 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 2)

| PARAMETER† | FROM (INPUT) | TO (OUTPUT) | LEVELS OF DELAY | TEST CONDITIONS | SN54S139 SN74S139A | | | UNIT |
|------------------|---------------|-------------|-----------------|--|-----------------------|-----|-----|------|
| | | | | | MIN | TYP | MAX | |
| t _{PLH} | Binary Select | Any | 2 | R _L = 280 Ω, C _L = 15 pF | 5 7.5 ns | | | |
| t _{PHL} | | | | | 6.5 10 ns | | | |
| t _{PLH} | | | | | 7 12 ns | | | |
| t _{PHL} | | | | | 8 12 ns | | | |
| t _{PLH} | Enable | Any | 2 | | 5 8 ns | | | |
| t _{PHL} | | | | | 6.5 10 ns | | | |

† t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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