National Semiconductor

Programmable Array Logic (PAL®)

Description

The PAL® family utilizes National Semiconductor's Schottky TTL process and bipolar PROM fusible-link technology to provide user-programmable logic to replace conventional SSI/MSI gates and flip-flops. Typical chip count reduction gained by using PALs is greater than 4:1.

The family lets the systems engineer customize his chip by opening fusible links to configure AND and OR gates to perform his desired logic functions. Complex interconnections that previously required timeconsuming layout are thus transferred from PC board to silicon where they can be easily modified during prototype checkout or production.

The PAL transfer function is the familiar sum of products with a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array. (The PROM is a fixed AND array driving a programmable OR array.) In addition, the PAL family offers these options:

- Variable input/output in ratio.
- Programmable TRISTATE® outputs.
- Registers and feedback.

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops that are loaded on the low-to-high transition of the clock. PAL logic diagrams are shown with all fuses blown, enabling the designer to use the diagrams as coding sheets.

The entire PAL family is programmed on conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to make verification difficult. This feature gives the user a proprietary circuit that is very difficult to copy.

Features

- Programmable replacement for conventional TTL logic.
- Simplifies prototyping and board layout.
- Skinny DIP packages.
- Reliable titanium-tungsten fuses.
- Available in standard, low power, and high speed versions.

Table 2-1. Part Types

Part Number	Description
PAL10H8	OCTAL 10 INPUT AND-OR GATE ARRAY
PAL 12H6	HEX 12 INPUT AND-OR GATE ARRAY
PAL 14H4	QUAD 14 INPUT AND-OR GATE ARRAY
PAL 16H2	DUAL 16 INPUT AND-OR GATE ARRAY
PAL 16C1	16 INPUT AND-OR/AND-OR-INVERT GATE ARRAY
PAL 10L8	OCTAL 10 INPUT AND-OR-INVERT GATE ARRAY
PAL 12L6	HEX 12 INPUT AND-OR-INVERT GATE ARRAY
PAL 14L4	QUAD 14 INPUT AND-OR-INVERT GATE ARRAY
PAL 16L2	DUAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL 16L8	OCTAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL 16R8	OCTAL 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL 16R6	HEX 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL 16R4	QUAD 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL 16X4	QUAD 16 INPUT REGISTERED AND-OR-XOR GATE ARRAY
PAL 16A4	QUAD 16 INPUT REGISTERED AND-CARRY-OR-XOR GATE ARRAY

Absolute Maximum Ratings

	Operating		Programming
Supply voltage V_{CC}	7 V		12 V
Input voltage	5.5 V		12 V
Off-state output voltage	5.5 V		12 V
Storage temperature range	-65 C	to	150 C

Table 2-2. Electrical Characteristics

Over Recommended Operating Temperature Range
10H8, 12H6, 14H4, 16H2, 16C1, 10L8, 12L6, 14L4, 16L2

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC} = MIN I_I = *−18* mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX V_I = 5.5 V			1.0	mA
I_{IH}	High-level input current	V_{CC} = MAX V_I = 2.4V			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX V_I = 0.4V			−250	μA
I_{OS}	Short-circuit output current	V_{CC} = 5.0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX		55	90	mA

Table 2-3. Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Unit
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			−2.0			−3.2	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free air temperature	−55		125	0		75	°C

Table 2-4. Switching Characteristics

Over Recommended Ranges of Temperature and V_{CC}

Symbol	Parameter	Test Conditions†† R_L = 2.0 K Ω	Military T_A = −55° to +125°C V_{CC} = 5.0V ±10%			Commercial T_A = 0° to 75°C V_{CC} = 5.0V ± 5%			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{PD}	From any input to any output	C_L = 15pF		25	45		25	40	ns

Table 2-5. Electrical Characteristics

Over Recommended Operating Temperature Range
16L8, 16R8, 16R6, 16R4, 16X4, 16A4

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage		V_{CC} = MIN I_I = -18 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OL} = MAX			0.5	V
I_{OZH}	Off-state output current high-level voltage applied		V_{CC} = MAX, V_{IH} = 2V, V_O = 2.4V, VIL = 0.8V			100	μA
I_{OZL}	Off-state output current low-level voltage applied		V_{CC} = MAX, V_{IH} = 2V V_O = 0.4V, VIL = 0.8V			−100	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX V_I = 5.5 V			1.0	mA
I_{IH}	High-level input current		V_{CC} MAX V_I = 2.4V			25	μA
I_{IL}	Low-level input current		V_{CC} MAX V_I = 0.4V			−250	μA
I_{OS}	Short-circuit output current		V_{CC} = 5.0V	−30		−130	mA
I_{CC}	Supply Current	16L8	V_{CC} = MAX		140	210†	mA
		16R4,16R6,16R8			150	225†	
		16X4,16A4			160		

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Table 2-6. Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Unit
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			−2.0			−3.2	mA
I_{OL}	Low-level output current			12			24†††	mA
T_A	Operating free air temperature	−55		125*	0		75	°C

Table 2-7. Switching Characteristics

Over Recommended Ranges of Temperature and V_{CC}

Symbol	Parameter		Test Conditions†† R_L = 667 Ω	Military T_A = −55° to +125°C V_{CC} = 5.0V ±10%			Commercial T_A = 0° to 75°C V_{CC} = 5.0V ± 5%			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input to output		C_L = 45pF		25	45		25	40	ns
t_{PD}	Clock to output				15	25		15	25	ns
t_{PZX}	Pin 11 to output enable				15	25		15	25	ns
t_{PXZ}	Pin 11 to output disable		CL = 5pF		15	25		15	25	ns
t_{PZX}	Input to output enable		C_L = 45pF		25	45		25	40	ns
t_{PXZ}	Input to output disable		C_L = 5pF		25	45		25	40	ns
t_w	Width of clock	High		25			25			ns
		Low		25			25			
t_{su}	Setup time	16R8,16R6,16R4		45			40			ns
		16X4,16A4								
t_h	Hold time			0	−15		0	−15		ns

*Operating Case Temperature only, T_C = 125°C

†I_{CC} = MAX at minimum temperature

††See Standard Test Load and Definition of Waveforms

†††One output at a time; otherwise, 16mA

Table 2-8. T_A = 25 C

Symbol	Parameter		Limits Min	Typ	Max	Units
V_{IHH}	Program-level input voltage		11.0	11.5	12.0	V
I_{IHH}	Program-level input current	Output Program Pulse			50	mA
		OD,L/R			25	
		All Other Inputs			5	
I_{CCH}	Program Supply Current				400	mA
T_P	Program Pulse Width		10		50	µs
t_d	Delay time		100			ns
	Program Pulse duty cycle				25	%
V_P	Program/Verify-Protect-input voltage			20		V
I_P	Program/Verify-Protect-input current				400	mA
t_{dv}	Delay Time to Verify		100			µs
V_{PH}	Programming Pulse		11.0	11.5	12.0	V

Truth Table Explanations

H = high level (steady-state)

L = low level (steady-state).

| = transition from low to high level.

| = transition from high to low level.

X = irrelevant (any input, including transitions).

Z = off (high-impedance) state of a 3-state output.

a...h = the level of steady-state inputs at A through H respectively.

Q_0 = the level of Q before the indicated steady-state input conditions were established.

$/Q_0$ = complement of Q_0, or level of /Q before the indicated steady-state input conditions were established.

Q_n = level of Q before the most recent active transition, indicated by |or|.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with | and/or |, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_O, or $/Q_O$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output.

Programming

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all 15 PAL types. The array is divided into two groups, products 0 through 31 and products 32 through 63, for which pin identifications are shown in Figure 2-2. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

1. Raise Output Disable, OD, to V_{IHH}.
2. Select an input line by specifying I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7, and L/R as shown in Table 12.
3. Select a product line by specifying A_0, A_1, and A_2 one-of-eight select as shown in Table 2-10.
4. Raise V_{CC} (pin 20) to V_{IHH}.
5. Program the fuse by pulsing the output pins O_n of the selected product group to V_{PH} as shown in Table 13.
6. Lower V_{CC} (pin 20) to 6.0 V.
7. Pulse the CLOCK pin and verify output pins O_n to be Low for active Low PAL types or High for active High PAL types.
8. Lower V_{CC}(pin 20) to 4.5 V and repeat step 7.
9. Should the output not verify, repeat steps 1 through 8 up to five (5) times.

Repeat this procedure for all fuses to be blown. (See Figure 2-3.)

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to V_D for 10 ms. V_{CC} is not required during this operation.

Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
R = 10 k Ohms to 5.0 V.
V_{PH} = Programming Pulse

Table 2-9. Input Line Select

Input Line Number	Pin Identification								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	R
1	HH	HH	HH	HH	HH	HH	HH	H	R
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	R
5	HH	HH	HH	HH	HH	HH	H	HH	R
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	R
9	HH	HH	HH	HH	HH	H	HH	HH	R
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	R
13	HH	HH	HH	HH	H	HH	HH	HH	R
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	R
17	HH	HH	HH	H	HH	HH	HH	HH	R
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	R
21	HH	HH	H	HH	HH	HH	HH	HH	R
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	R
25	HH	H	HH	HH	HH	HH	HH	HH	R
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	R
29	H	HH	HH	HH	HH	HH	HH	HH	R
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

Table 2-10. Product Line Select

Product Line Number	Pin Identification						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0,32	R	R	R	V_{PH}	R	R	R
1,33	R	R	R	V_{PH}	R	R	HH
2,34	R	R	R	V_{PH}	R	HH	R
3,35	R	R	R	V_{PH}	R	HH	HH
4,36	R	R	R	V_{PH}	HH	R	R
5,37	R	R	R	V_{PH}	HH	R	HH
6,38	R	R	R	V_{PH}	HH	HH	R
7,39	R	R	R	V_{PH}	HH	HH	HH
8,40	R	R	V_{PH}	R	R	R	R
9,41	R	R	V_{PH}	R	R	R	HH
10,42	R	R	V_{PH}	R	R	HH	R
11,43	R	R	V_{PH}	R	R	HH	HH
12,44	R	R	V_{PH}	R	HH	R	R
13,45	R	R	V_{PH}	R	HH	R	HH
14,46	R	R	V_{PH}	R	HH	HH	R
15,47	R	R	V_{PH}	R	HH	HH	HH
16,48	R	V_{PH}	R	R	R	R	R
17,49	R	V_{PH}	R	R	R	R	HH
18,50	R	V_{PH}	R	R	R	HH	R
19,51	R	V_{PH}	R	R	R	HH	HH
20,52	R	V_{PH}	R	R	HH	R	R
21,53	R	V_{PH}	R	R	HH	R	HH
22,54	R	V_{PH}	R	R	HH	HH	R
23,55	R	V_{PH}	R	R	HH	HH	HH
24,56	V_{PH}	R	R	R	R	R	R
25,57	V_{PH}	R	R	R	R	R	HH
26,58	V_{PH}	R	R	R	R	HH	R
27,59	V_{PH}	R	R	R	R	HH	HH
28,60	V_{PH}	R	R	R	HH	R	R
29,61	V_{PH}	R	R	R	HH	R	HH
30,62	V_{PH}	R	R	R	HH	HH	R
31,63	V_{PH}	R	R	R	HH	HH	HH

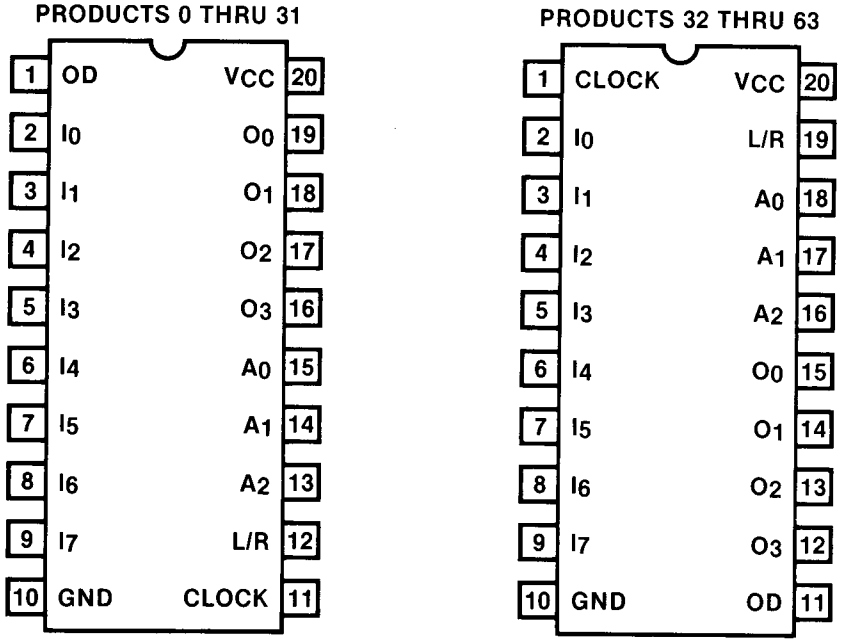

FIGURE 2-2. Pin Identification

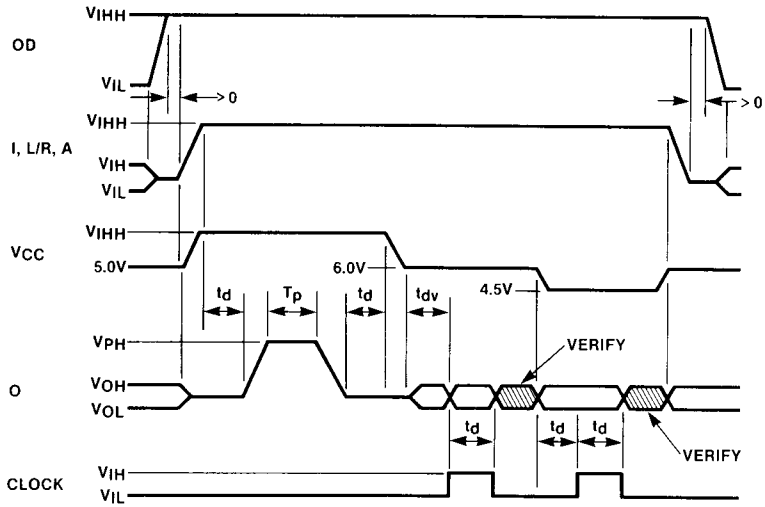

FIGURE 2-3. Programming Waveforms

Absolute Maximum Ratings

	Operating		Programming
Supply voltage V_{CC}	7 V		12 V
Input voltage	5.5 V		12 V
Off-state output voltage	5.5 V		12 V
Storage temperature range	-65 C	to	150 C

Table 2-11. Electrical Characteristics

Over Recommended Operating Temperature Range
10H8A, 12H6A, 14H4S, 16H2A, 16C1A,
10L8A, 12L6A, 14L4A, 16L2A

typo S/B 'A'

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC} = MIN I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX V_I = 5.5 V			1.0	mA
I_{IH}	High-level input current	V_{CC} = MAX V_I = 2.4V			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX V_I = 0.4V			−250	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX		55	90	mA

Table 2-12. Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Unit
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			−2.0			−3.2	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free air temperature	−55		125	0		75	°C

Table 2-13. Switching Characteristics

Over Recommended Ranges of Temperature and V_{CC}

Symbol	Parameter	Test Conditions†† R_L = 2.0 K Ω	Military T_A = −55° to +125°C V_{CC} = 5.0V ±10% Min	Typ	Max	Commercial T_A = 0° to 75°C V_{CC} = 5.0V ± 5% Min	Typ	Max	Unit
t_{PD}	From any input to any output	C_L = 15pF		8	25		18	25	ns

Table 2-14. Electrical Characteristics

Over Recommended Operating Temperature Range
16L8A, 16R8A, 16R6A, 16R4A

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC} = MIN I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OL} = MAX			0.5	V
I_{OZH}	Off-state output current high-level voltage applied	V_{CC} = MAX, V_{IH} = 2V, V_O = 2.4V, VIL = 0.8V			100	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC} = MAX, V_{IH} = 2V V_O = 0.4V, VIL = 0.8V			−100	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX V_I = 5.5 V			1.0	mA
I_{IH}	High-level input current	V_{CC} MAX V_I = 2.4V			25	μA
I_{IL}	Low-level input current	V_{CC} MAX V_I = 0.4V			−250	μA
I_{OS}	Short-circuit output current	V_{CC} MAX	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = MAX			150	mA

MIL CC*
-55 35

Table 2-15. Recommended Operating Conditions

Symbol	Parameter	Military Min	Nom	Max	Commercial Min	Nom	Max	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			−2.0			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free air temperature	−55		125*	0		75	°C

Table 2-16. Switching Characteristics

Over Recommended Ranges of Temperature and V_{CC}

Symbol	Parameter		Test Conditions†† R_L = 667 Ω	Military T_A = −55° to +125°C V_{CC} = 5.0V ±10% Min	Typ	Max	Commercial T_A = 0° to 75°C V_{CC} = 5.0V ± 5% Min	Typ	Max	Unit
t_{PD}	Input to output		C_L = 45pF		18	30		18	35	ns
t_{PD}	Clock to output				15	20		15	25	ns
t_{PZX}	Pin 11 to output enable				12			12		ns
t_{PXZ}	Pin 11 to output disable		CL = 5pF		12			12		ns
t_{PZX}	Input to output enable		C_L = 45pF		18			18		ns
t_{PXZ}	Input to output disable		C_L = 5pF		18			18		ns
t_w	Width of clock	High		17			17			ns
		Low		17			17			
t_{su}	Setup time			40			35			ns
		16X4,16A4								
t_h	Hold time			0	−15		0	−15		ns

*Operating Case Temperature only, T_C = 125°C

†I_{CC} = MAX at minimum temperature

††See Standard Test Load and Definition of Waveforms

†††One output at a time; otherwise, 16mA

Absolute Maximum Ratings

	Operating		Programming
Supply voltage V_{CC}	7 V		12 V
Input voltage	5.5 V		12 V
Off-state output voltage	5.5 V		12 V
Storage temperature	-65 C	to	150 C

Table 2-17. Electrical Characteristics

Over Recommended Operating Temperature Range
16L8A-1, 16R8A-1, 16R6A-1, 16R4A-1

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage		V_{CC} = MIN I_I = -18 mA			1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OL} = MAX			0.5	V
I_{OZH}	Off-state output current high-level voltage applied		V_{CC} = MAX, V_{IH} = 2V, V_O = 2.4V, VIL = 0.8V			100	μA
I_{OZL}	Off-state output current low-level voltage applied		V_{CC} = MAX, V_{IH} = 2V V_O = 0.4V, VIL = 0.8V			-100	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX V_I = 5.5 V			1.0	mA
I_{IH}	High-level input current		V_{CC} MAX V_I = 2.4V			25	μA
I_{IL}	Low-level input current		V_{CC} MAX V_I = 0.4V			-250	μA
I_{OS}	Short-circuit output current		V_{CC} MAX	-30		-130	mA
I_{CC}	Supply Current	16L8	V_{CC} = MAX		140	180†	mA
		16R4,16R6,16R8			140	180†	

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Table 2-18. Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Unit
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			-2.0			-3.2	mA
I_{OL}	Low-level output current			12			24†††	mA
T_A	Operating free air temperature	-55		125*	0		75	°C

Table 2-19. Switching Characteristics

Over Recommended Ranges of Temperature and V_{CC}

Symbol	Parameter		Test Conditions†† R_L = 667 Ω	Military T_A = −55° to +125°C V_{CC} = 5.0V ±10% Min	Typ	Max	Commercial T_A = 0° to 75°C V_{CC} = 5.0V ± 5% Min	Typ	Max	Unit
t_{PD}	Input to output				15	30		15	25	ns
t_{PD}	Clock to output		C_L = 45pF		12	17		12	17	ns
t_{PZX}	Pin 11 to output enable				15	25		15	25	ns
t_{PXZ}	Pin 11 to output disable		CL = 5pF		15	25		15	25	ns
t_{PZX}	Input to output enable		C_L = 45pF		18	40		18	35	ns
t_{PXZ}	Input to output disable		C_L = 5pF		18	40		18	35	ns
t_w	Width of clock	High		17			17			ns
		Low		17			17			
t_{su}	Setup time	16R8,16R6,16R4		30			25			ns
t_h	Hold time			0		−15	0		−15	ns

*Operating Case Temperature only, T_C = 125°C

†I_{CC} = MAX at minimum temperature

††See Standard Test Load and Definition of Waveforms

†††One output at a time; otherwise, 16mA

DMPALXXXXA/A-1 Programming Algorithm

The PALXXXXA/A-1 may be programmed, using the same data file as the PALXXXX DEVICES, as a 512x4 PROM or, with a byte wide data file, as a 256x8 PROM. To program a particular fuse, both an input line and a product line are selected according to the following procedure.

1. After the selected inputs, I_0 through I_7 (Figure 2-5), and V_{CC} at 4.5 to 5.0 V, have been stable for T_1, raise the "Enable" (pin 11) to V_{EP}. (See Table 2-20.)
2. After T_2, raise V_{CC}(pin 20) to V_{CP}.
3. After T_3, pulse the selected output (pins 16 through 19 for the 512x4 data format and Products 0 through 31 or pins 12 through 15 for Products 32 through 63) with V_{OP}.
4. After the programming pulse (V_{OP}) and T_1, lower V_{CC} to V_{VH}.
5. After T_4 at V_{VH} (high voltage verify V_{CC}), pulse the CLOCK pin.
6. After T_1, verify the output and lower the V_{CC} pin to V_{VL}.
7. After T_1 at V_{VL} (low voltage verity V_{CC}), pulse the CLOCK pin.
8. After T_1, verify the output.
9. Should the output not verify, repeat steps 2 through 8 up to five (5) times.
10. Remove V_{EP} (the voltage on pin 11).
11. After T_5, change the inputs as required.
12. Repeat steps 1 through 11 as required.

Programming Duty Cycle

The maximum allowable programming duty cycle is 10 percent. If V_{CC} (pin 1) is removed completely following each programming cycle, 30 percent duty cycle is permitted.

Register Test Algorithm

The registers contained within applicable DMPALXXXXA/A-1 devices may be "Cleared" or "Preset" to facilitate functional testing of the device and/or provide a register test mechanism. Selected input lines are utilized to perform this function according to the following procedure.

1. With I_2, I_5, and I_6(pins 4, 7, and 8) at logic "0" (V_{IL}) and V_{CC} at 4.5 to 5.0 V (pin 20), set I_7 (pin 9) to logic "1" (level high) to CLEAR the registers. The remaining inputs, I_0, I_1, I_3, I_4 (pins 2, 3, 5 and 6) may be either logic "0" or "1".
2. After T_1, raise CE (the "Enable" input, pin 11) to V_{EP}.
3. After T_2, raise I_0 and I_1 (pins 2 and 3) to the same voltage as V_{EP}, observing the same T_r (slew rate).
4. After T_3, provide a CLOCK pulse to pin 1.
5. After T_1, remove the elevated voltage from pins 2 and 3 and verify the register status at the outputs (whichever is applicable of pins 12 through 19).
6. After T_1, remove V_{EP} (the elevated voltage on pin 11).
7. After T_1, the functional test may begin with the newly defined register status.

DMPALXXXXA/A-1

Programming Timing

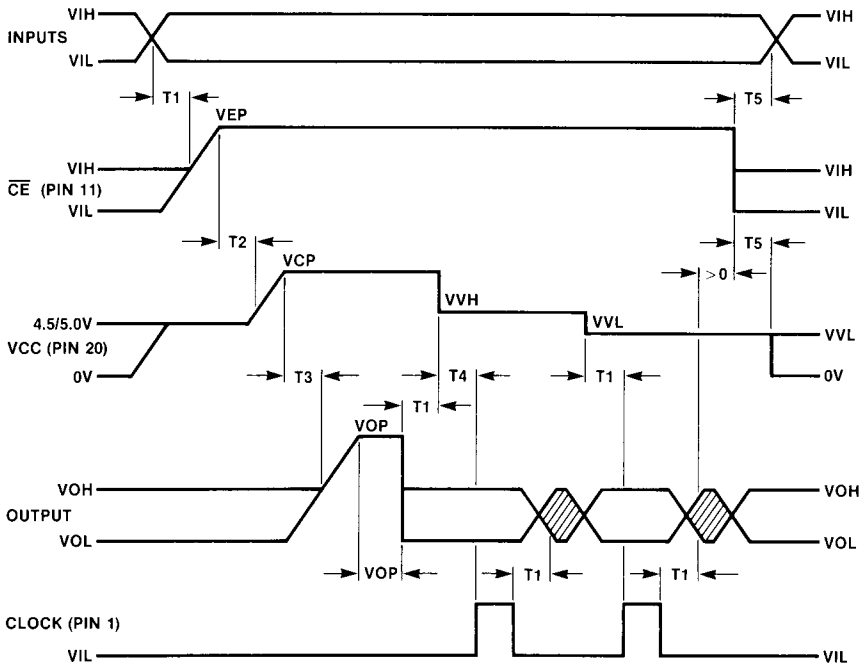

FIGURE 2-4. Programming Timing Diagram.

Table 2-20. Programming Parameters (TA = 25° C)

Symbol	Parameter	Min	Typ	Max	Units
V_{EP}	CE (enable) programming voltage	9.5	10.0	10.5	V
V_{CP}	Elevated V_{CC} (while programming)	9.5	10.0	10.5	V
V_{OP}	Output pin programming voltage	9.5	10.0	10.5	V
V_{OP}	Output pin programming pulse	9.0	10.0	11.0	us
V_{VH}	High verify (V_{CC}) voltage		6.0	6.0	V
V_{VL}	Low verify (V_{CC}) voltage	4.5	4.5		V
T_r	Slew rate; V_{EP}, V_{CP}, and V_{OP}	0.4	5.0	10.0	V/us
T_1	Input, V_{VH}, output set-up time	100			ns
T_2	Enable set-up to V_{CP} time	500			ns
T_3	V_{CP} set-up to programming pulse	200			ns
T_4	V_{VH} set-up to CLOCK	10			ns
T_5	Input hold time (from V_{EP})	50			ns
CLOCK	PAL Register CLOCK	25			ns

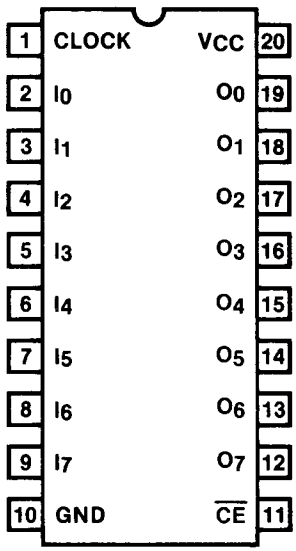

Figure 2-5. Pin Identification

Table 2-21. Input Line Select

Input Line Number	Pin Identification				
	I4	I3	I2	I1	I0
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	L	H	H	H	H
16	H	L	L	L	L
17	H	L	L	L	H
18	H	L	L	H	L
19	H	L	L	H	H
20	H	L	H	L	L
21	H	L	H	L	H
22	H	L	H	H	L
23	H	L	H	H	H
24	H	H	L	L	L
25	H	H	L	L	H
26	H	H	L	H	L
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

Table 2-22. Product Line Select

Product Line Number	Pin Identification		
	I7	I6	I5
0,8,16,24,32,40,48,56	L	L	L
1,9,17,25,33,41,49,57	L	L	H
2,10,18,26,34,42,50,58	L	H	L
3,11,19,27,35,43,51,59	L	H	H
4,12,20,28,36,44,52,60	H	L	L
5,13,21,29,37,45,53,61	H	L	L
6,14,22,30,38,46,54,62	H	H	L
7,15,23,31,39,47,55,63	H	H	H

Table 2-23. Product Group Select

Product Line Group	Pin Identification							
	O7	O6	O5	O4	O3	O2	O1	O0
0-7	Z	Z	Z	Z	Z	Z	Z	V_{OP}
8-15	Z	Z	Z	Z	Z	Z	V_{OP}	Z
16-23	Z	Z	Z	Z	Z	V_{OP}	Z	Z
24-31	Z	Z	Z	Z	V_{OP}	Z	Z	Z
32-39	Z	Z	Z	V_{OP}	Z	Z	Z	Z
40-47	Z	Z	V_{OP}	Z	Z	Z	Z	Z
48-55	Z	V_{OP}	Z	Z	Z	Z	Z	Z
56-63	V_{OP}	Z	Z	Z	Z	Z	Z	Z

Voltage Legend

L = Low-level input voltage, V_{IL}

H = High-level input voltage, V_{IH}

V_{OP} = Programming pulse

Z = 10k Ohm minimum to 5.0 V

A Programming Variance

Although the DMPALXXXA/A-1 series most easily programs as a 256x8 PROM, the programming data may be formatted to be compatible with the DMPALXXX series. Programming the first "half," products 0 through 31, requires that device pins O_0 through O_3 be utilized to limit the programming to those product groups while the device pins designated O_4through O_7 remain in the "Z" state (terminated to 5.0 V through an impedance of 10K Ohms minimum). For programming the remaining products, 32 through 63, O_4 through O_7 are utilized for the programming pulses (V_{OP}), while O_0 through O_3 remain in the "Z" state. While this variance will allow a certain compatibility in data formatting to be achieved, no variance in the programming algorithm is suggested.