NOVEMBER 1985—REVISED APRIL 1988

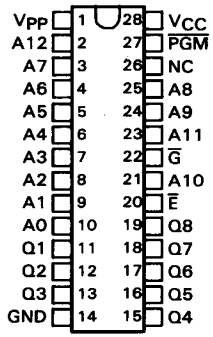
This Data Sheet is Applicable to All TMS27C64s and TMS27PC64s Symbolized with Code "A" as Described on Page 12.

- **Organization . . . 8K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible with Existing 64K MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**

V_{CC} ±5%	V_{CC} ±10%	
'27C64-100		100 ns
'27C/PC64-120	'27C/PC64-12	120 ns
'27C/PC64-1	'27C/PC64-15	150 ns
'27C/PC64-2	'27C/PC64-20	200 ns
'27C/PC64	'27C/PC64-25	250 ns

- **Power Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming or Fast Programming Algorithms**
- **3-State Output Buffers**
- **400 mV Guaranteed DC Noise Immunity with Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.25 V)**
  - **Active . . . 158 mW Worst Case**
  - **Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**
- **PEP4 Version Available with 168 Hour Burn-In, and also Extended Guaranteed Operating Temperature Ranges**

J & N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Address Inputs
$\overline{E}$	Chip Enable Power Down
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
NU	Make No External Connection
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12-13 V Programming Power Supply

description

The TMS27C64 series are 65,536-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC64 series are 65,536-bit, one-time, electrically programmable read-only memories.

These devices are fabricated using power saving CMOS technology for high-speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C64 and the TMS27PC64 are pin compatible with 28-pin 64K MOS ROMs, PROMs, and EPROMs.

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The TMS27C64 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C64 is available with two guaranteed temperature ranges of 0°C to 70°C and −40°C to 85°C (TMS27C64-_ _JL and TMS27C64-_ _JE, respectively). The TMS27C64 is also offered with 168-hour burn-in on both temperature ranges (TMS27C64-_ _JL4 and TMS27C64-_ _JE4, respectively). (See table below).

The TMS27PC64 PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC64 is guaranteed for operation from 0°C to 70°C.

All package styles conform to JEDEC standards.

EPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	−40°C to 85°C	0°C to 70°C	−40°C to 85°C
TMS27C64-XXX	JL	JE	JL4	JE4

These EPROMs and PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 12-13 V supply is needed for programming. All programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. Fast programming uses a V_{PP} of 12.5 V and a V_{CC} of 6.0 V for a nominal programming time of two minutes. SNAP! Pulse programming uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of one second. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation listed in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V for Fast, or 13.0 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X	V_{IH}	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	CODE	
							MFG	DEVICE
							97	07

†X Can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C64s or TMS27PC64s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 through Q8.

latchup immunity

Latchup immunity on the TMS27C64 and TMS27PC64 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001; *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family,"* available through TI Field Sales Offices.

power down

Active I_{CC} current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C64)

Before programming, the TMS27C64 EPROM is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic 0s are programmed into the desired locations. A programmed logic 0 can be erased only by ultraviolet light. The recommended minimum ultraviolet light exposure dose (UV intensity × exposure time) is 15 watt-seconds per square centimeter.

A typical 12-milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C64, the window should be covered with an opaque label.

initializing (TMS27PC64)

The one-time programmable TMS27PC64 PROM is provided with all bits in the logic 1 state, then logic 0s are programmed into the desired locations. Logic 0s programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 64K EPROM and PROM can be programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart of Figure 1, which can reduce programming time to a nominal of one second. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q1 through Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100 μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13.0 V, V_{CC} = 6.5 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

Fast programming

The 64K EPROM and PROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming, data is presented in parallel (eight bits) on pins Q1 through Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, V_{CC} = 6.0 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Fast programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6.0 V and V_{PP} = 12.5 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code, which is output on Q1-Q8; A0 = V_{IH} accesses the device code, which is output on Q1-Q8. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for these devices is 97, and the device code is 07.

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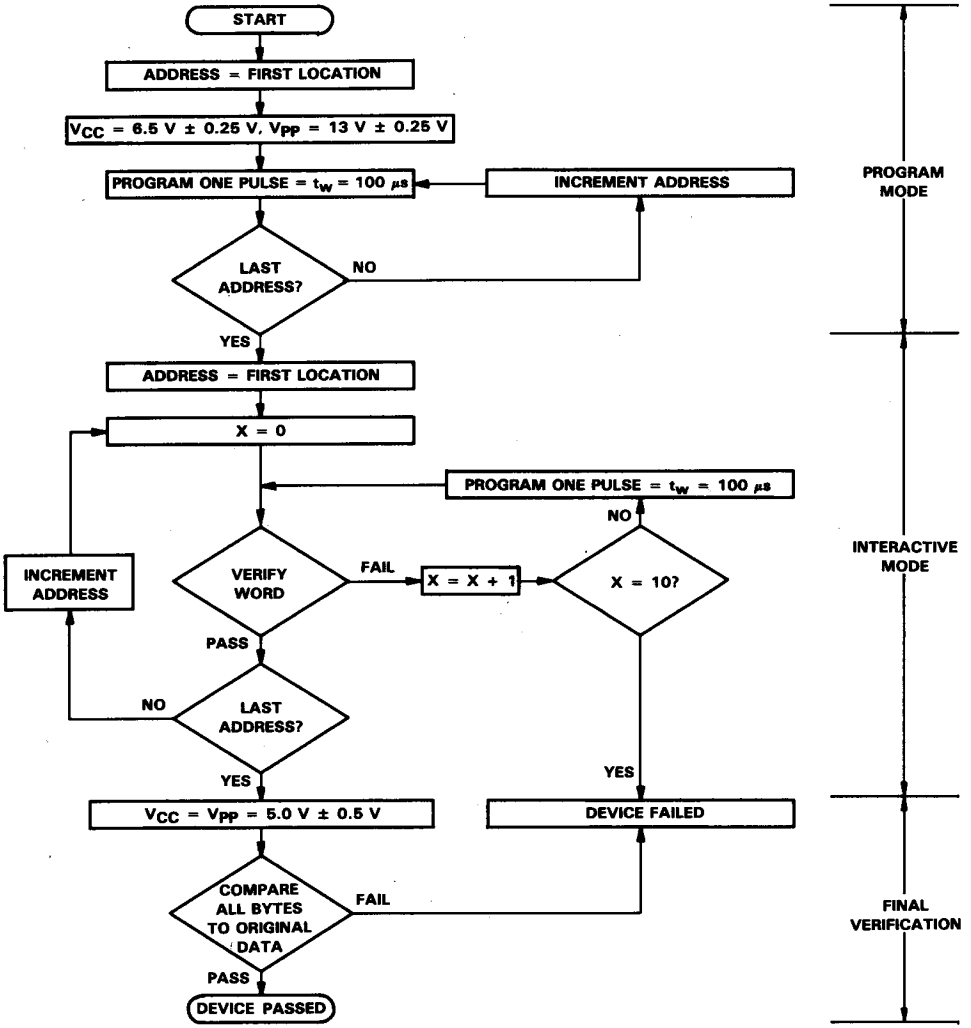

FIGURE 1. SNAP! PULSE PROGRAMMING FLOWCHART

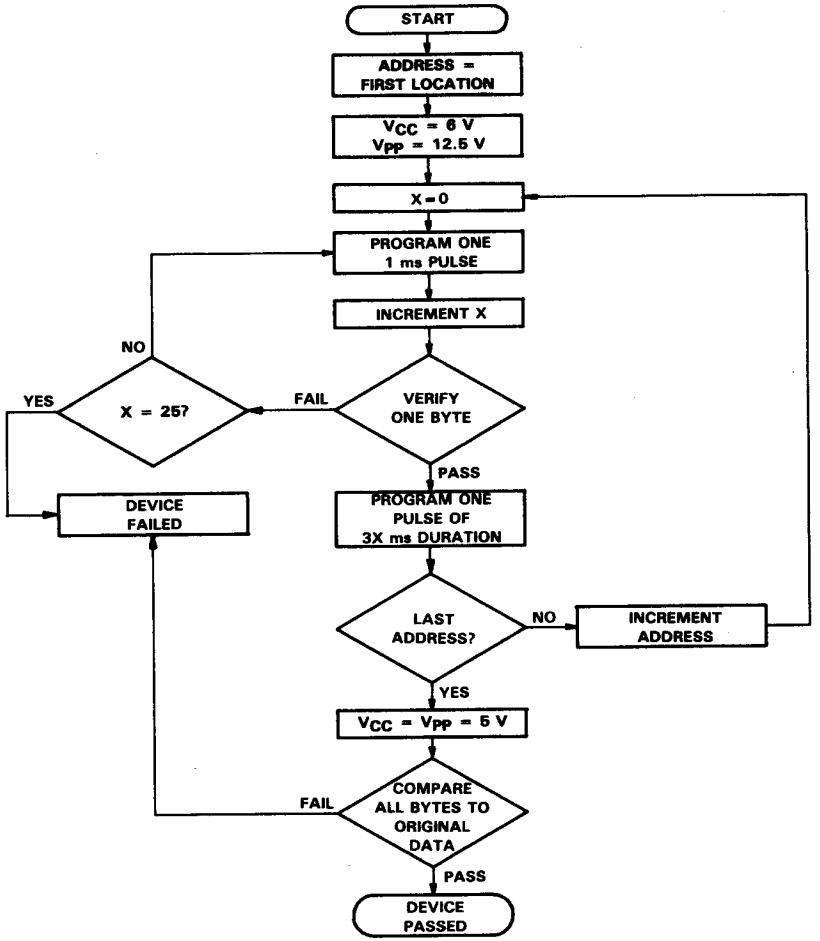

FIGURE 2. FAST PROGRAMMING FLOWCHART

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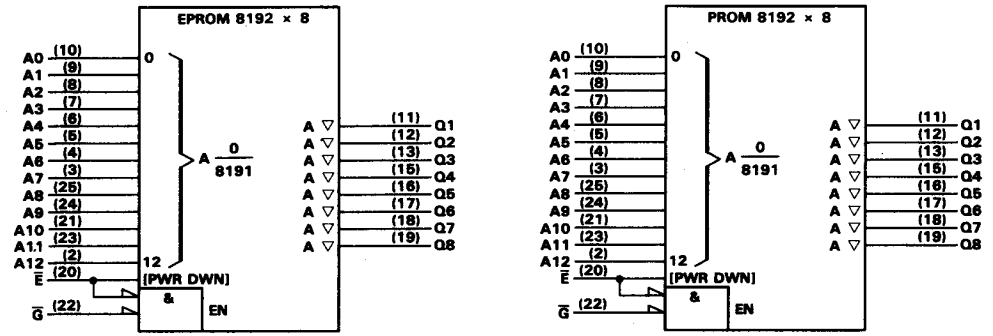
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
J and N packages illustrated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . −0.6 V to 6.5 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C64-_ _JL and JL4; '27PC64-_ _NL) . . . . . 0°C to 70°C
Operating free-air temperature range ('27C64-_ _JE and JE4) . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			'27C64-100, '27C/PC64-120, '27C/PC64-1, '27C/PC64-2, '27C/PC64			'27C/PC64-12, '27C/PC64-15, '27C/PC64-20, '27C/PC64-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	4.5	5	5.5	V
		Fast programming algorithm	5.75	6	6.25	5.75	6	6.25	V
		SNAP! Pulse programming algorithm	6.25	6.50	6.75	6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)	$V_{CC}-0.6$		$V_{CC}+0.6$	$V_{CC}-0.6$		$V_{CC}+0.6$	V
		Fast programming algorithm	12	12.5	13	12	12.5	13	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	12.75	13	13.25	V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		0.2	−0.5		0.2	V
T_A	Operating free-air temperature (see table, page 2)		(see table, page 2)			(see table, page 2)			°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −2.5 mA	3.5			V
			I_{OH} = −20 μA	$V_{CC}-0.1$			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
			I_{OL} = 20 μA			0.1	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±1	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±1	μA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC}$ = 5.5 V		1	10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E} = V_{IH}$		250	500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E} = V_{CC}$		100	250	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		15	30	mA

†Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		10	14	pF

†Typical values are at T_A = 25°C and nominal voltages.
‡Capacitance measurements are made on sample basis only.

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switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C64-100		'27C/PC64-120 '27C/PC64-12		'27C/PC64-1 '27C/PC64-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		55		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	40	0	45	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C/PC64-2 '27C/PC64-20		'27C/PC64 '27C/PC64-25		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		200		250	ns
$t_{a(E)}$	Access time from chip enable			200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

†Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.50 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

NOTES: 4. For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0. (Reference page 10.)
5. Common test conditions apply for t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.5 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 4)

			MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	μs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			μs
$t_{su(E)}$	$\overline{E}$ setup time		2			μs
$t_{su(G)}$	$\overline{G}$ setup time		2			μs
$t_{su(D)}$	Data setup time		2			μs
$t_{su(VPP)}$	V_{PP} setup time		2			μs
$t_{su(VCC)}$	V_{CC} setup time		2			μs
$t_{h(A)}$	Address hold time		0			μs
$t_{h(D)}$	Data hold time		2			μs

NOTE 4: For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 (reference below).

PARAMETER MEASUREMENT INFORMATION

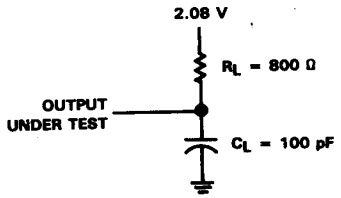
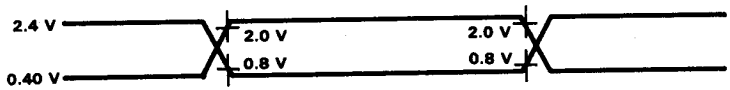


FIGURE 3. OUTPUT LOAD CIRCUIT

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 for both outputs.

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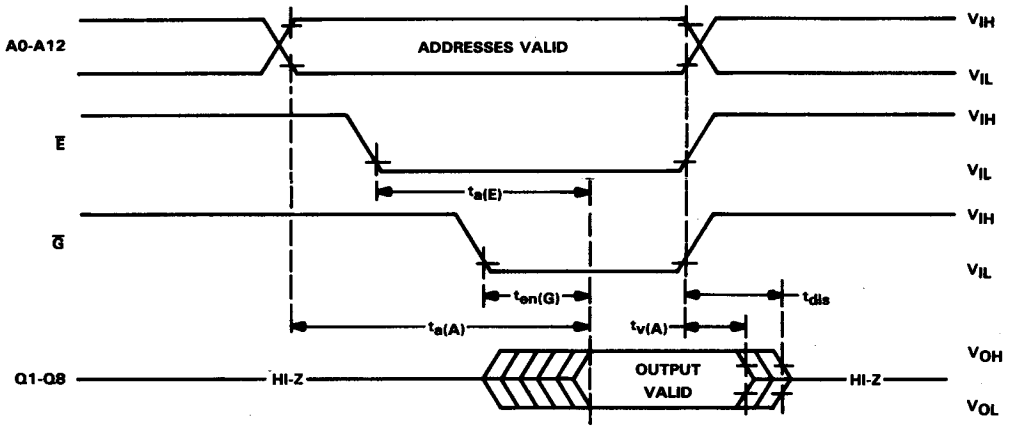
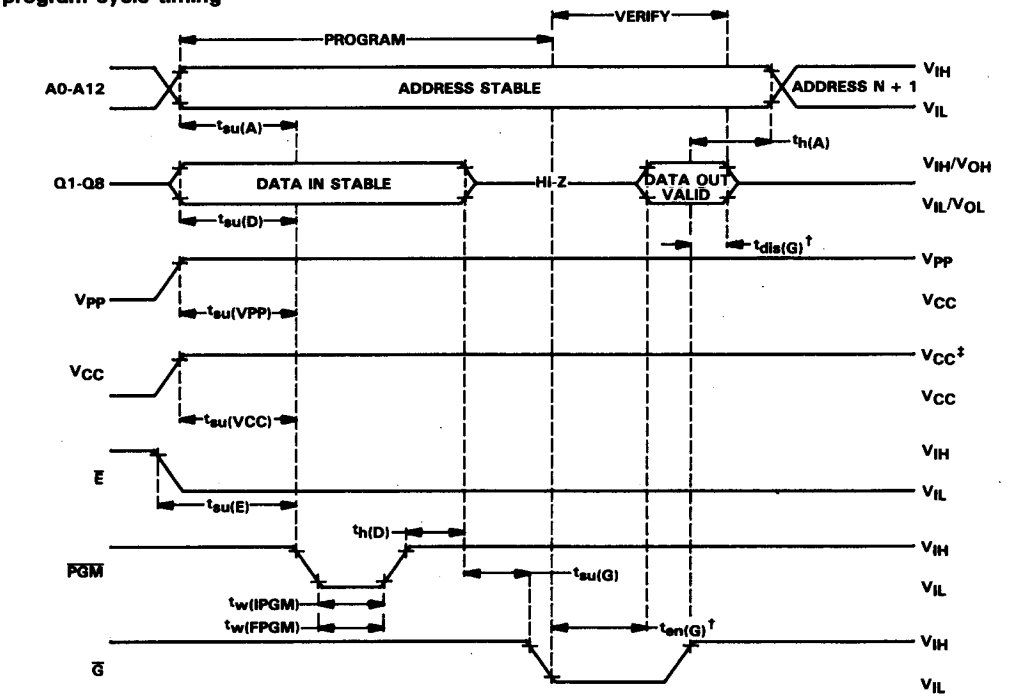
read cycle timing



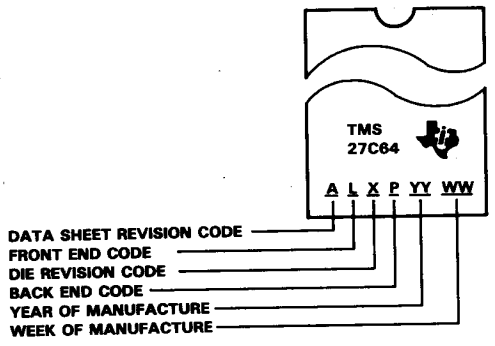
program cycle timing



†$t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡12.5 V V_{PP} and 6.0 V V_{CC} for Fast programming; 13.0 V V_{PP} and 6.5 V V_{CC} for SNAP! Pulse programming.

device symbolization

This data sheet is applicable to all TI TMS27C64 CMOS EPROMs and TMS27PC64 PROMs with the data sheet revision code "A" as shown below.



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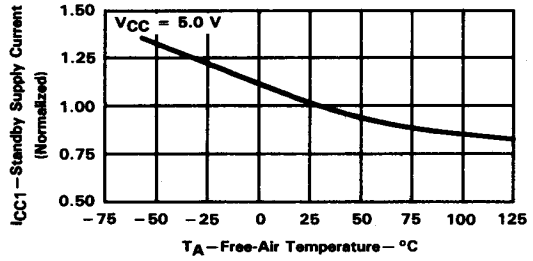
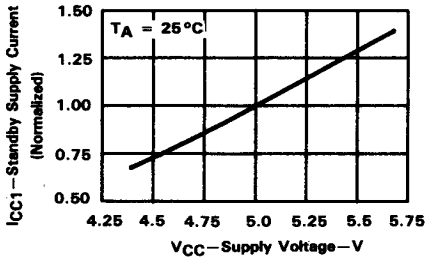
TYPICAL TMS27C/PC64 CHARACTERISTICS

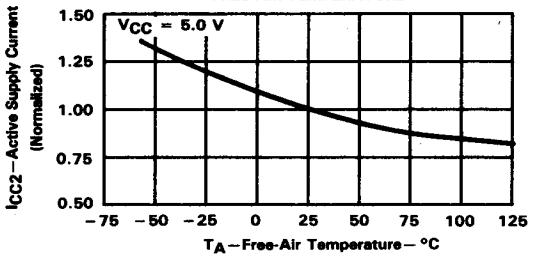
STANDBY SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



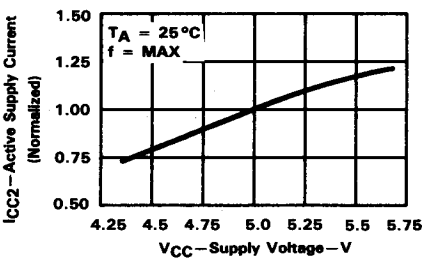
STANDBY SUPPLY CURRENT
vs
SUPPLY VOLTAGE



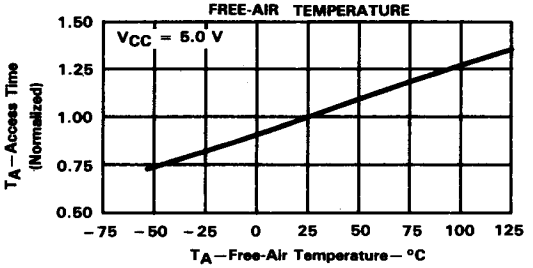
ACTIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



ACTIVE SUPPLY CURRENT
vs
SUPPLY VOLTAGE



ACCESS TIME
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
SUPPLY VOLTAGE