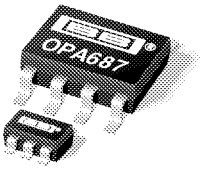
BURR-BROWN®



OPA687

SpeedPlus™ Wideband, Ultra-Low Noise, Voltage Feedback OPERATIONAL AMPLIFIER With Power Down

FEATURES

- HIGH GAIN BANDWIDTH: 3.8GHz
- LOW INPUT VOLTAGE NOISE: 0.95nV/√Hz
- VERY LOW DISTORTION: –95dBc (5MHz)
- LOW DISABLED POWER: 2mW
- VERY HIGH SLEW RATE: 900V/µs
- STABLE FOR G ≥ 12

APPLICATIONS

- LOW DISTORTION ADC DRIVER
- OC-3 FIBER OPTIC RECEIVER
- LOW NOISE DIFFERENTIAL AMPLIFIERS
- EQUALIZING RECEIVERS
- ULTRASOUND CHANNEL AMPLIFIERS
- IMPROVED REPLACEMENT FOR THE CLC425

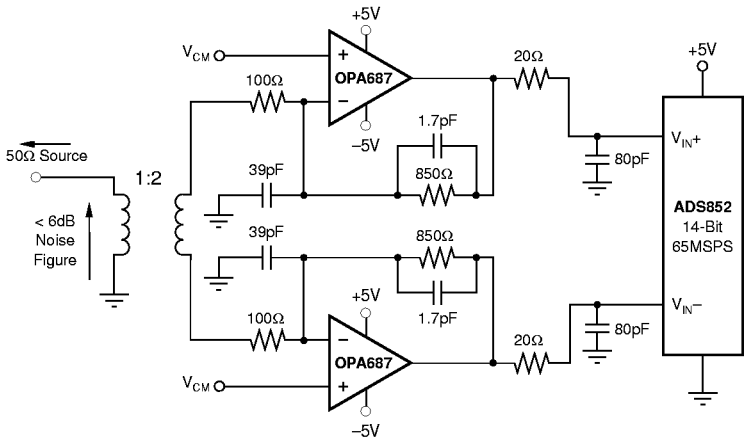
DESCRIPTION

The OPA687 combines a very high gain bandwidth and large signal performance with an ultra-low input noise voltage (0.95nV/√Hz) while dissipating only 18mA supply current. Where power savings is paramount, the OPA687 also includes an optional power down pin that, when pulled low, will disable the amplifier and decrease the quiescent current to only 1% of its powered up value. This optional feature may be left disconnected to insure normal amplifier operation when no power-down is required.

The combination of low input voltage and current noise, along with a 3.8GHz gain bandwidth product, make the OPA687 an ideal amplifier for wideband transimpedance stages. As a voltage gain stage, the OPA687 is optimized for a flat frequency response at a gain of +20 and is guaranteed stable down to gains of +12. New external compensation techniques allows the OPA687 to be used at any inverting gain with excellent frequency response control. Using this compensation can give an extremely high dynamic range ADC driver to support > 40MSPS 12- and 14-bit converters.

OPA687 RELATED PRODUCTS

SINGLES	DUAL	INPUT NOISE VOLTAGE (nV/√Hz)	GAIN BANDWIDTH PRODUCT (MHz)
OPA642		2.7	210
OPA643		2.3	800
OPA686	OPA2686	1.3	1600



Ultra-High Dynamic Range Digitizer, > 90dB SFDR Through 30MHz

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

Printed in U.S.A. September, 1998

SPECIFICATIONS: V_S = ±5V

R_L = 100Ω, R_F = 750Ω, and R_G = 39.2Ω, G = +20 (Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA687U, N TYP +25°C	OPA687U, N GUARANTEED +25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
AC PERFORMANCE (Figure 1)								
Closed-Loop Bandwidth	G = +12, R_G = 39.2Ω, V_O = 200mVp-p	600				MHz	typ	C
	G = +20, R_G = 39.2Ω, V_O = 200mVp-p	290	180	160	140	MHz	min	B
	G = +50, R_G = 39.2Ω, V_O = 200mVp-p	75	60	54	48	MHz	min	B
Gain Bandwidth Product	G ≥ +50	3800	3000	2700	2400	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +20, R_L = 100Ω	35	24	20	18	MHz	min	B
Peaking at a Gain of +12		3	8	10	14	dB	max	B
Harmonic Distortion	G = +20, f = 5MHz, V_O = 2Vp-p							
2nd Harmonic	R_L = 100Ω	–74	–70	–68	–65	dBc	max	B
	R_L = 500Ω	–94	–90	–88	–85	dBc	max	B
3rd Harmonic	R_L = 100Ω	–108	–95	–90	–85	dBc	max	B
	R_L = 500Ω	–110	–105	–100	–95	dBc	max	B
Two-Tone, 3rd-Order Intercept	G = +20, f = 20MHz	43	40	39	37	dBm	min	B
Input Voltage Noise Density	f > 1MHz	0.95	1.1	1.15	1.3	nV/√Hz	max	B
Input Current Noise Density	f > 1MHz	2.5	3.2	3.3	3.5	pA/√Hz	max	B
Pulse Response								
Rise/Fall Time	0.2V Step	1.2	2.0	2.2	2.5	ns	max	B
Slew Rate	2V Step	900	675	550	450	V/µs	min	B
Settling Time to 0.01%	2V Step	17				ns	typ	C
0.1%	2V Step	15	18	20	25	ns	max	B
1%	2V Step	8	11	13	17	ns	max	B
DC PERFORMANCE[4]								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V	85	**78**	75	70	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±0.1	**±1**	±1.2	±1.6	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			5	10	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	–20	**–33**	–36	–40	µA	max	A
Input Bias Current Drift (magnitude)	V_{CM} = 0V			–50	–100	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±0.2	**±1.0**	±1.5	±1.8	µA	max	A
Input Offset Current Drift	V_{CM} = 0V			±12	±15	nA/°C	max	B
INPUT								
Common-Mode Input Range (CMIR)[5]		±3.7	**±3.2**	±3.1	±3.0	V	min	A
Common-Mode Rejection (CMR)	V_{CM} = ±0.5V, Input Referred	100	**88**	83	78	dB	min	A
Input Impedance								
Differential-Mode	V_{CM} = 0V	2.5 || 2.5				kΩ || pF	typ	C
Common-Mode	V_{CM} = 0V	1.0 || 1.2				MΩ || pF	typ	C
OUTPUT								
Output Voltage Swing	≥ 400Ω Load	±3.6	**±3.3**	±3.1	±3.0	V	min	A
	100Ω Load	±3.5	**±3.2**	±2.9	±2.8	V	min	A
Current Output, Sourcing	V_O = 0V	80	**60**	50	40	mA	min	A
Current Output, Sinking	V_O = 0V	–80	**–60**	–50	–40	mA	min	A
Closed-Loop Output Impedance	G = +20, f = < 100kHz	0.006				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage		±6	**±6**	±6	±6	V	max	A
Quiescent Current, max	V_S = ±5V	18.5	**19**	19.5	20.5	mA	max	A
Quiescent Current, min	V_S = ±5V	18.5	**18**	17.5	16	mA	min	A
Power Supply Rejection Ratio								
+PSR, –PSR	|V_S| = 4.5V to 5.5V, Input Referred	85	**80**	78	75	dB	min	A
POWER-DOWN (Disabled Low)	(Pin 8 SO-8; Pin 5 on SOT23-6)							
Power-Down Quiescent Current (+V_S)		–225	**–300**	–350	–400	µA	max	A
On Voltage (Enabled High or Floated)		> 2.8				V	typ	C
Off Voltage (Disabled Asserted Low)		< 2.2				V	typ	C
Power-Down Pin Input Bias Current	($V_{\overline{DIS}}$ = 0)	100	**125**	140	160	µA	max	A
Power-Down Time		200				ns	typ	C
Power-Up Time		60				ns	typ	C
Off Isolation	5MHz, Input to Output	70				dB	typ	C
THERMAL								
Specification U, N		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction to Ambient							
U	8-Pin, SO-8		125			°C/W	typ	C
N	6-Pin, SOT23		150			°C/W	typ	C

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction temperature = ambient for +25°C guaranteed specifications. (3) Junction temperature = ambient at low temperature limit: junction temperature = ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive out of node. V_{CM} is the input common-mode voltage. (5) Tested <3dB below minimum specified CMR at ±CMIR limits.

ABSOLUTE MAXIMUM RATINGS

Power Supply	±6.5V_{DC}
Internal Power Dissipation	See Thermal Analysis
Differential Input Voltage	±1.2V
Input Voltage Range	±V_S
Storage Temperature Range: U, N	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+175°C

ELECTROSTATIC DISCHARGE SENSITIVITY

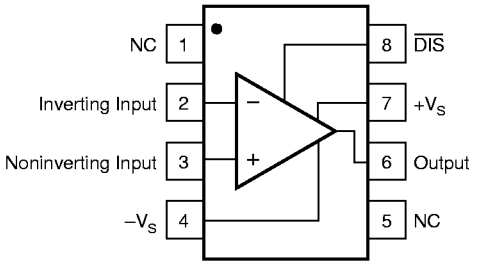
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

Top View **SO-8**

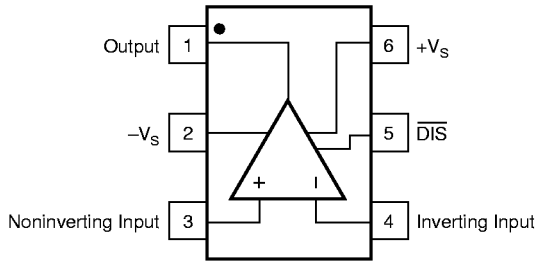
OPA687



NC: No Connection

SOT23-6

OPA687



PACKAGE/ORDERING INFORMATION

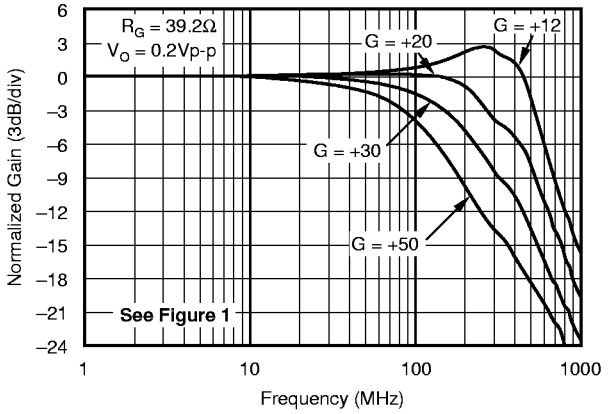
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[2]	TRANSPORT MEDIA
OPA687U	SO-8 Surface-Mount	182	–40°C to +85°C	OPA687U	OPA687U	Rails
"	"	"	"	"	OPA687U/2K5	Tape and Reel
OPA687N	6-Lead SOT23	332	–40°C to +85°C	A87	Contact Factory	Tape and Reel
"	"	"	"	"	Contact Factory	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "OPA687U/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

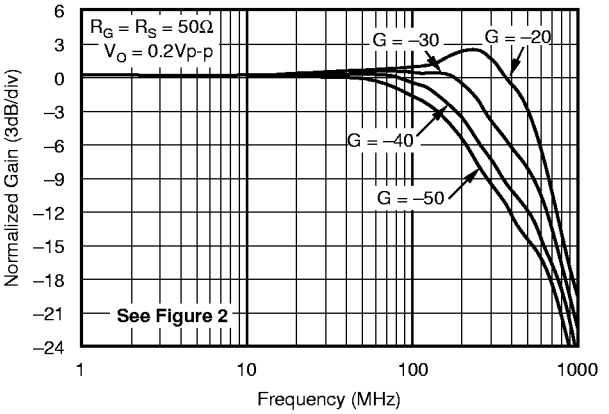
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$

$R_F = 750\Omega$, $R_G = 39.2\Omega$, G = +20 and $R_L = 100\Omega$, unless otherwise noted.

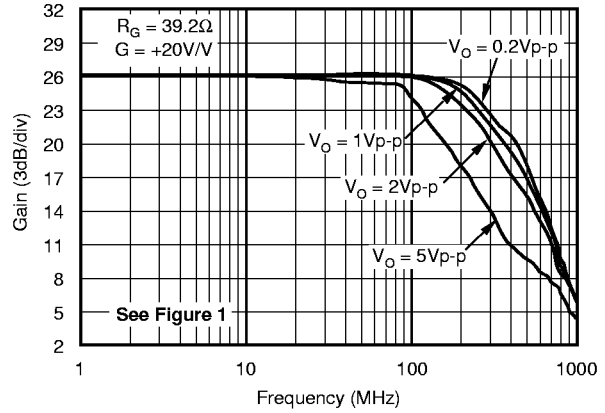
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



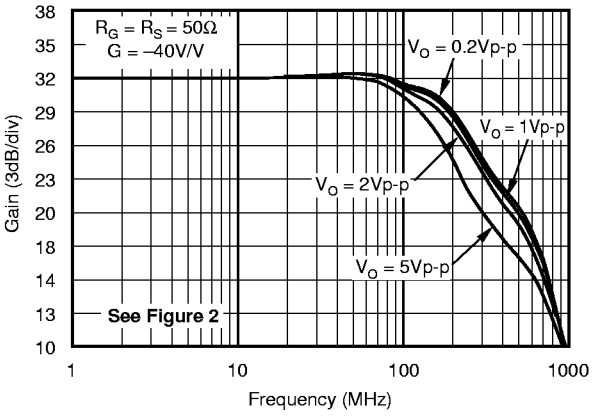
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



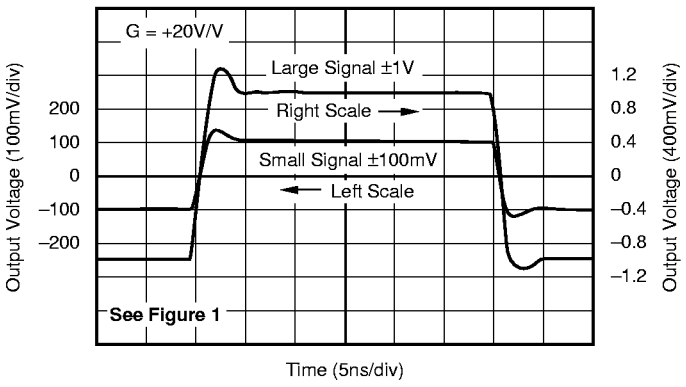
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



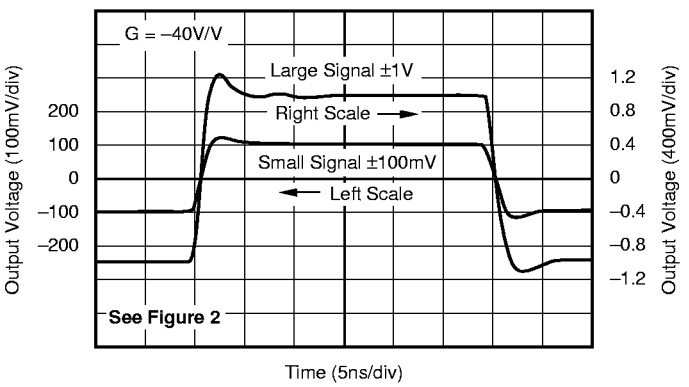
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



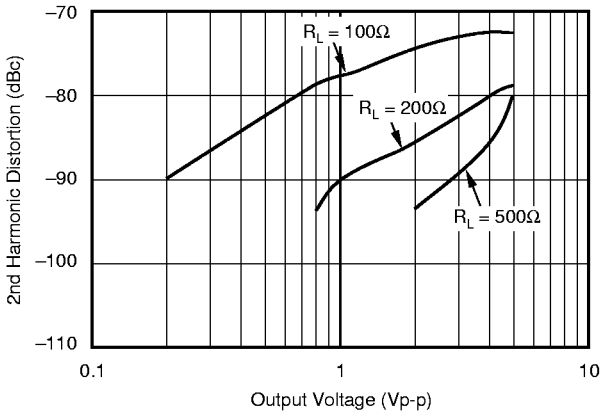
INVERTING PULSE RESPONSE



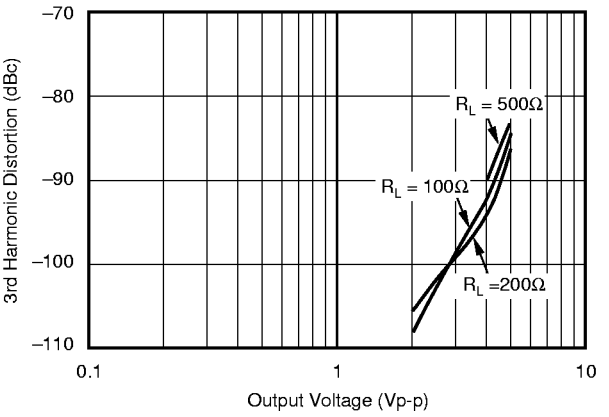
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (CONT)

$R_F = 750\Omega$, $R_G = 39.2\Omega$, G = +20 and $R_L = 100\Omega$, unless otherwise noted (Figure 1).

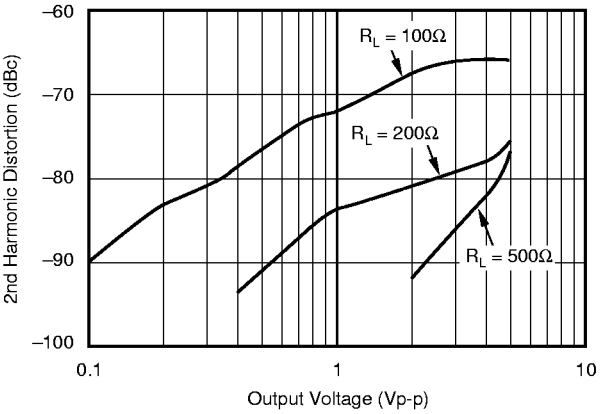
5MHz 2nd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



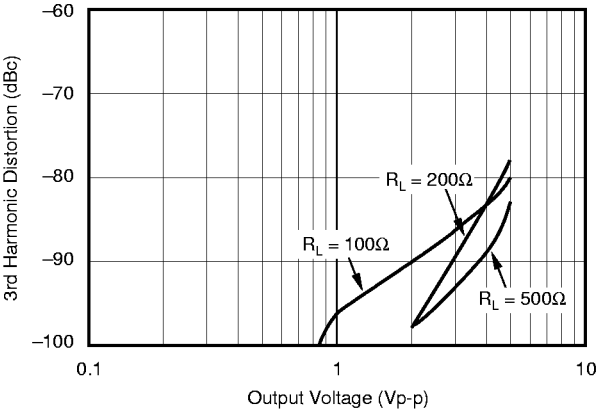
5MHz 3rd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



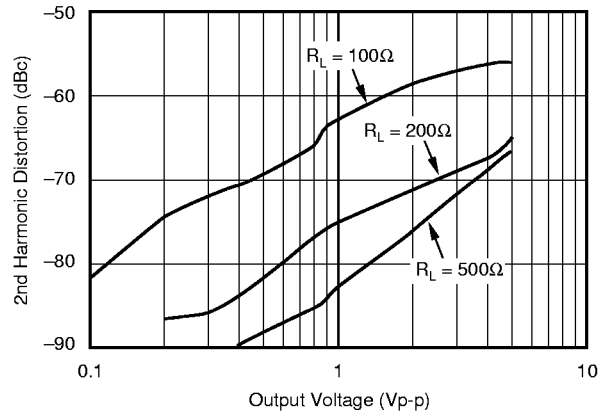
10MHz 2nd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



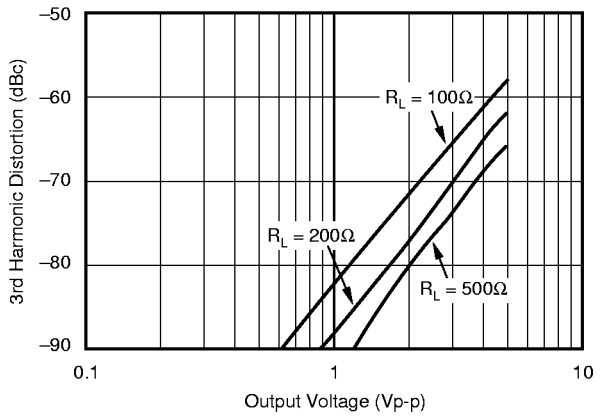
10MHz 3rd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



20MHz 2nd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



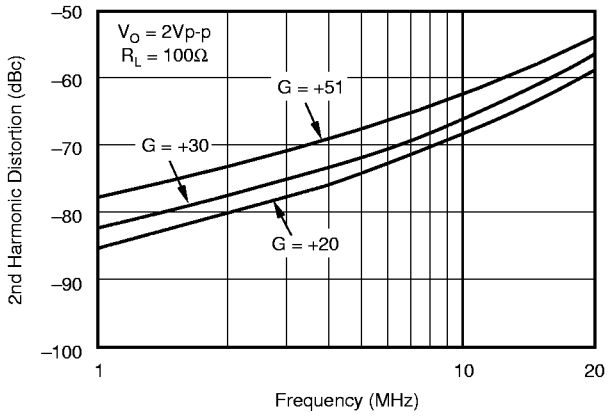
20MHz 3rd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



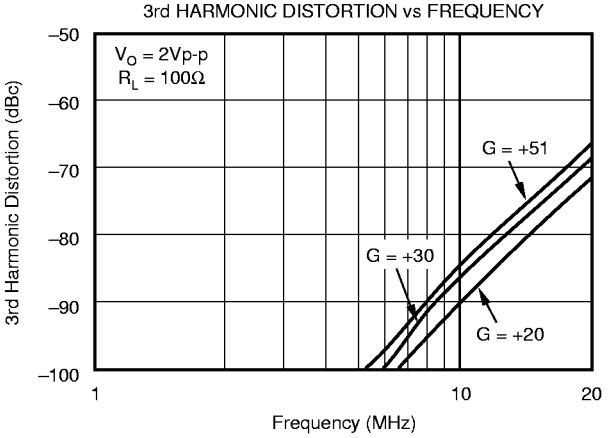
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (CONT)

$R_F = 750\Omega$, $R_G = 39.2\Omega$, G = +20 and $R_L = 100\Omega$, unless otherwise noted (Figure 1).

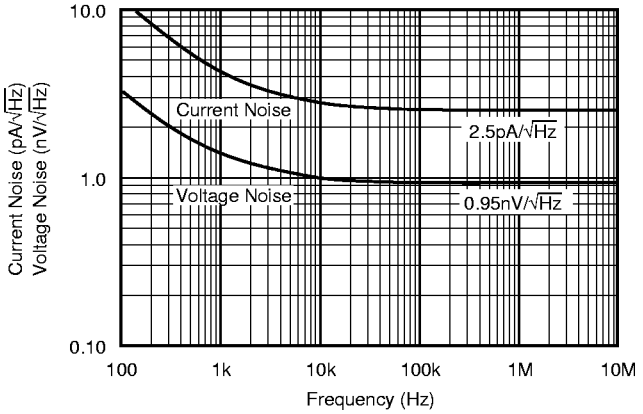
2nd HARMONIC DISTORTION vs FREQUENCY



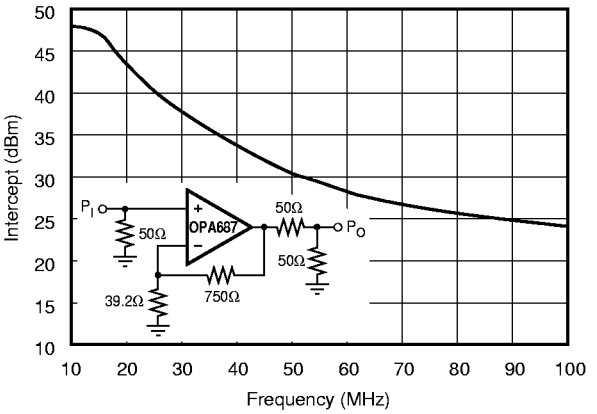
3rd HARMONIC DISTORTION vs FREQUENCY



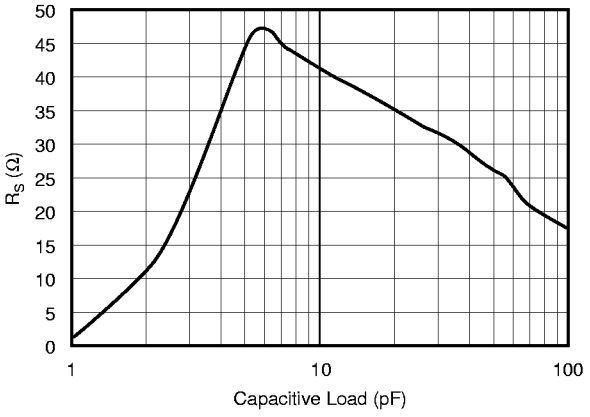
INPUT VOLTAGE and CURRENT NOISE DENSITY



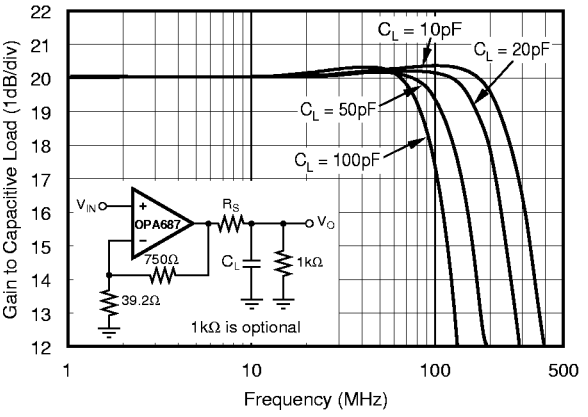
TWO-TONE, 3rd-ORDER INTERMODULATION INTERCEPT vs FREQUENCY



R_S vs CAPACITIVE LOAD



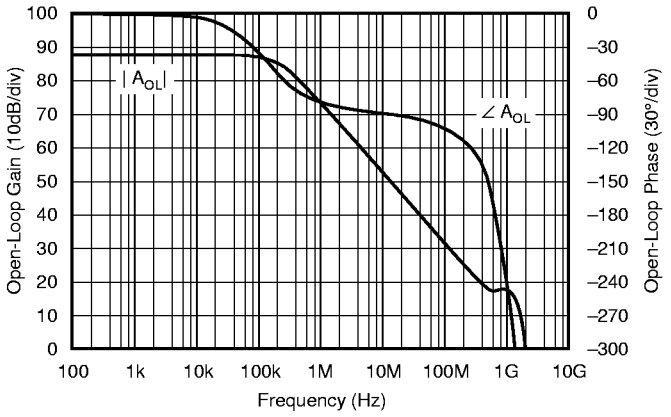
FREQUENCY RESPONSE vs CAPACITIVE LOAD



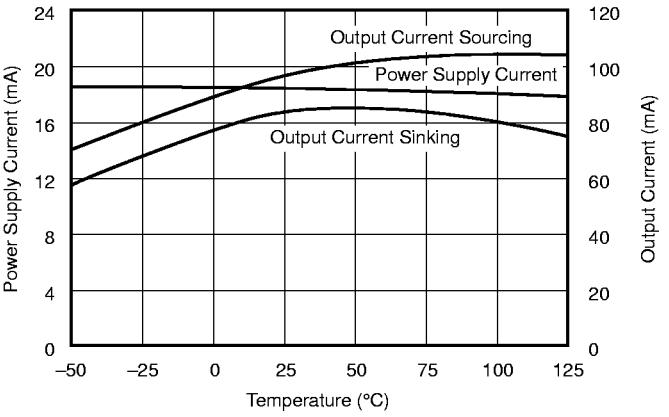
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (CONT)

$V_S = \pm 5V$, G = +20, $R_G = 39.2\Omega$, and $R_L = 100\Omega$, unless otherwise noted (Figure 1).

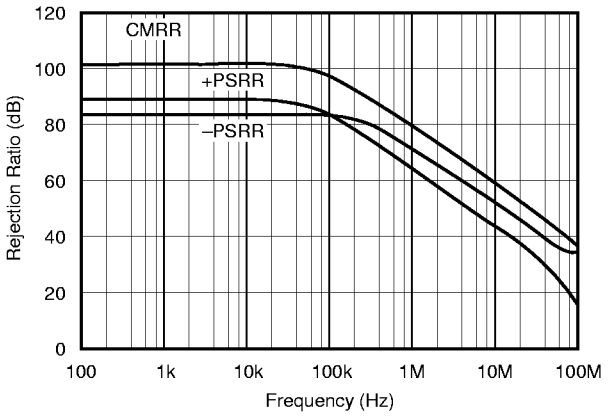
OPEN-LOOP GAIN and PHASE



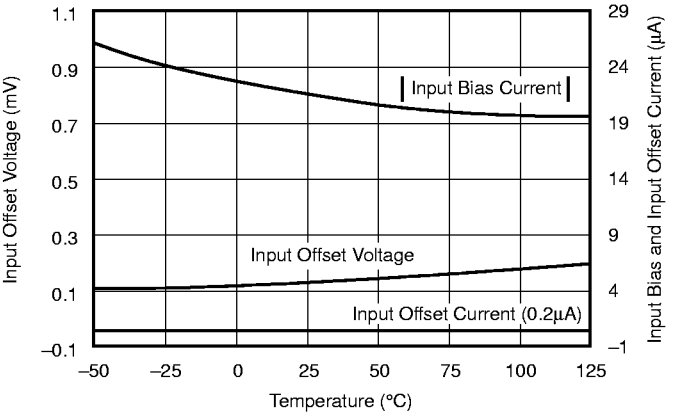
POWER SUPPLY and OUTPUT CURRENT vs TEMPERATURE



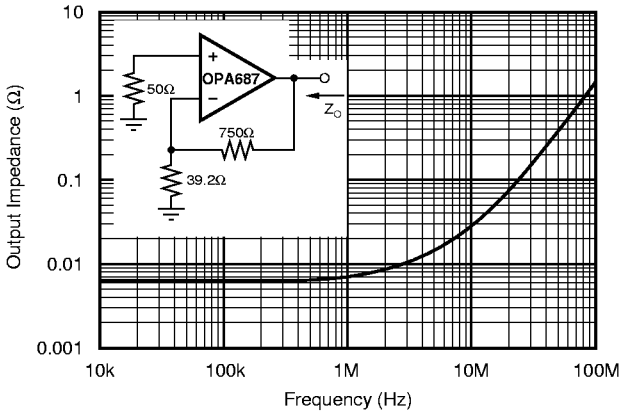
CMRR and PSRR



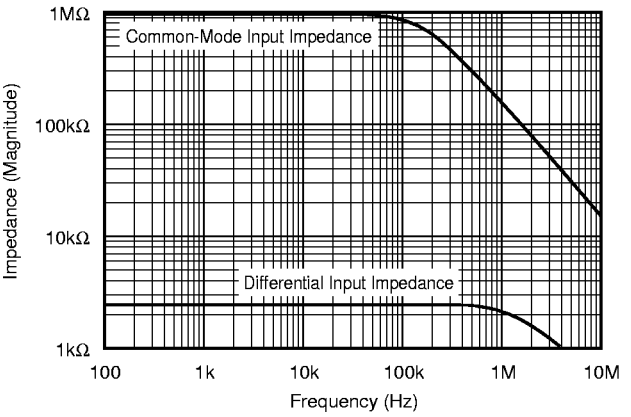
INPUT DC ERRORS vs TEMPERATURE



CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



COMMON-MODE and DIFFERENTIAL INPUT IMPEDANCE



APPLICATIONS INFORMATION

WIDEBAND, NON-INVERTING OPERATION

The OPA687 provides a unique combination of a very low input voltage noise along with a very low distortion output stage to give one of the highest dynamic range op amps available. Its very high Gain Bandwidth Product (GBP) can be used to either deliver high signal bandwidths at high gains, or to deliver very low distortion signals at moderate frequencies and lower gains. To achieve the full performance of the OPA687, careful attention to PC board layout and component selection is required as discussed in the remaining sections of this data sheet.

Figure 1 shows the non-inverting gain of +20 circuit used as the basis for most of the Typical Performance Curves. Most of the curves were characterized using signal sources with 50Ω driving impedance, and with measurement equipment presenting a 50Ω load impedance. In Figure 1, the 50Ω shunt resistor at the V_I terminal matches the source impedance of the test generator, while the 50Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin (V_O in Figure 1) while output power specifications are at the matched 50Ω load. The total 100Ω load at the output combined with the 790Ω total feedback network load, presents the OPA687 with an effective output load of 89Ω for the circuit of Figure 1.

Voltage feedback op amps, unlike current feedback designs, can use a wide range of resistor values to set their gain. The circuit of Figure 1, and the specifications at other gains, use an R_G set to 39.2Ω and R_F adjusted to get the desired gain. Using this guideline will guarantee that the noise added at the output due to Johnson noise of the resistors will not significantly increase the total over that due to the $0.95nV/\sqrt{Hz}$ input voltage noise for the op amp itself. This R_G is suggested as a good starting point for design. Other values are certainly acceptable if required by the design.

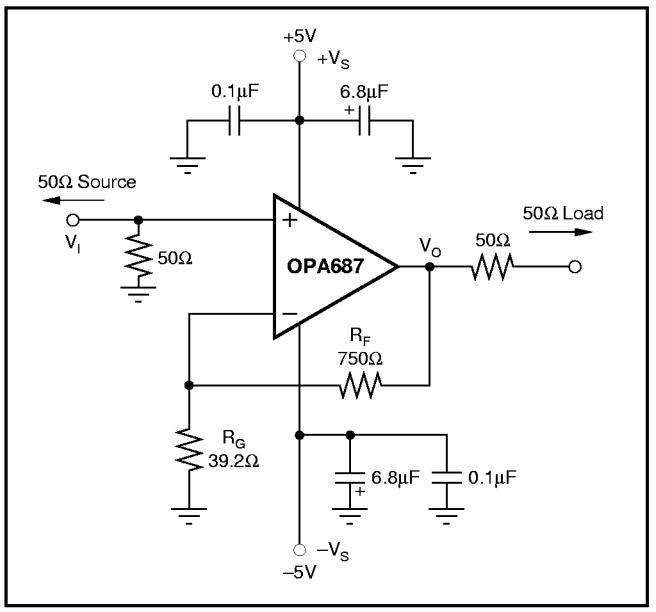


FIGURE 1. Non-Inverting G = +20 Specifications and Test Circuit.

WIDEBAND, INVERTING GAIN OPERATION

There can be significant benefits to operating the OPA687 as an inverting amplifier. This is particularly true when a matched input impedance is required. Figure 2 shows the inverting gain circuit used as a starting point for the Typical Performance Plots showing inverting mode performance.

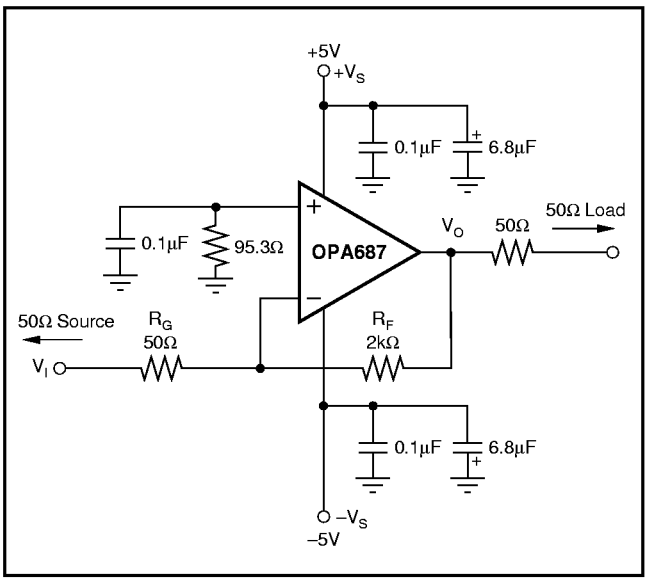


FIGURE 2. Inverting G = –40 Specifications and Test Circuit.

Driving this circuit from a 50Ω source, and constraining the gain resistor, R_G, to equal 50Ω, will give both a signal bandwidth and noise advantage. R_G in this case is acting as both the input termination resistor and the gain setting resistor for the circuit. Although the signal gain for the circuit of Figure 2 is double that for Figure 1, their noise gains are equal when the 50Ω source resistor is included. This has the interesting effect of doubling the equivalent GBP for the amplifier. This can be seen in comparing the G = +12 and G = –20 small-signal frequency response curves. Both show approximately 500MHz bandwidth with 3dB peaking, but the inverting configuration of Figure 2 is giving 4.4dB higher signal gain. The noise gains are approximately equal in this case. If the signal source is actually the low impedance output of another amplifier, R_G should be increased to be greater than the minimum value allowed at the output of that amplifier and R_F adjusted to get the desired gain. It is critical for stable operation of the OPA687 that this driving amplifier show a very low output impedance through frequencies exceeding the expected closed-loop bandwidth for the OPA687.

WIDEBAND, HIGH SENSITIVITY, TRANSIMPEDANCE DESIGN

The high GBP and low input voltage and current noise for the OPA687 make it an ideal wideband transimpedance amplifier for low to moderate transimpedance gains. Very high transimpedance gains (> 100kΩ) will benefit from the low input noise current of a FET-input op amp such as the OPA655. Unity gain stability in the op amp is NOT required

for application as a transimpedance amplifier. Figure 3 shows one possible transimpedance design example that would be particularly suitable for the 155Mbit data rate of an OC-3 receiver. Designs that require high bandwidth from a large area detector with relatively low transimpedance gain will benefit from the low input voltage noise for the OPA687. The amplifier's input voltage noise is peaked up over frequency by the diode source capacitance and can, in many cases, become the limiting factor to input sensitivity. The key elements to the design are the expected diode capacitance (C_D) with the reverse bias voltage ($-V_B$) applied, the desired transimpedance gain, R_F, and the GBP for the OPA687 (3600MHz). With these three variables set (and including the parasitic input capacitance for the OPA687 added to C_D), the feedback capacitor value (C_F) may be set to control the frequency response.

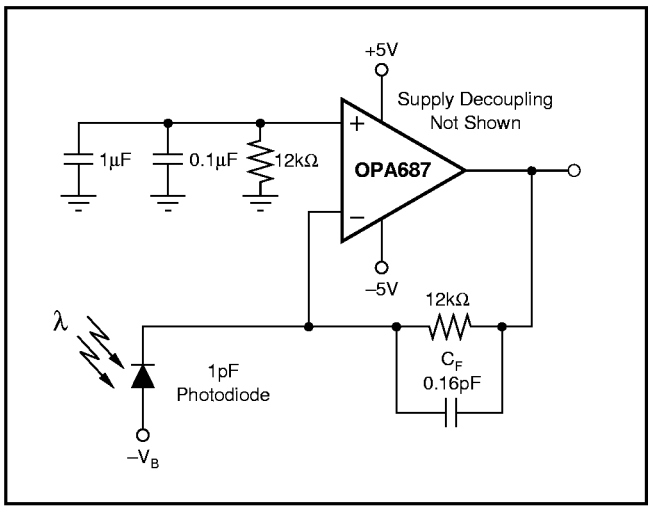


FIGURE 3. Wideband, High Sensitivity, OC-3 Transimpedance Amplifier.

To achieve a maximally flat 2nd-order Butterworth frequency response, the feedback pole should be set to:

$$1/(2\pi R_F C_F) = \sqrt{(GBP/(4\pi R_F C_D))}$$

Adding the common-mode and differential-mode input capacitance (1.2 + 2.5)pF to the 1pF diode source capacitance of Figure 3 (C_D), and targeting a 12kΩ transimpedance gain using the 3600MHz GBP for the OPA687, will require a feedback pole set to 71MHz to get a maximum bandwidth design. This will require a total feedback capacitance of 0.16pF.

Using this maximum bandwidth, maximally flat frequency response target will give an approximate –3dB bandwidth set by:

$$f_{-3dB} = \sqrt{(GBP/2\pi R_F C_D)}Hz$$

The example of Figure 3 will give approximately 100MHz flat bandwidth using the 0.16pF feedback compensation capacitor. This bandwidth will easily support an OC-3 receiver with exceptional sensitivity.

If the total output noise is bandlimited to a frequency less than the feedback pole frequency, a very simple expression for the equivalent input noise current can be derived as:

$$i_{EQ} = \sqrt{i_N^2 + \frac{4kT}{R_F} + \left(\frac{e_N}{R_F}\right)^2 + \frac{(e_N 2\pi C_D f)^2}{3}}$$

Where:

i_{EQ} = Equivalent input noise current if the output noise is bandlimited to $f < 1/(2\pi R_F C_D)$

i_N = Input current noise for the op amp inverting input

e_N = Input voltage noise for the op amp

C_D = Total Inverting Node Capacitance

f = Bandlimiting frequency in Hz (usually a post filter prior to further signal processing)

Evaluating this expression up to the feedback pole frequency at 71MHz for the circuit of Figure 3, gives an equivalent input noise current of 3.0pA/$\sqrt{Hz}$. This is somewhat higher than the 2.5pA/$\sqrt{Hz}$ for just the op amp itself. This total equivalent input current noise is being slightly increased by the last term in the equivalent input noise expression. It is essential in this case to use a low voltage noise op amp. For example, if a slightly higher input noise voltage, but otherwise identical, op amp were used instead of the OPA687 in this application (say 2.0nV/$\sqrt{Hz}$), the total input-referred current noise would increase to 4.0pA/$\sqrt{Hz}$. Low input voltage noise is required for the best sensitivity in these wideband transimpedance applications. This is often unspecified for dedicated transimpedance amplifiers with a total output noise for a specified source capacitance given instead. It is the relatively high input voltage noise for those components that cause higher than expected output noise if the source capacitance is higher than specificd.

LOW GAIN COMPENSATION FOR IMPROVED SFDR

A new external compensation technique may be used at low signal gains to retain the full slew rate and noise benefits of the OPA687 while maintaining the increased loop gain and the associated improvement in distortion offered by the decompensated architecture. This technique shapes the loop gain for good stability while giving an easily controlled second-order low pass frequency response. This technique was used for the circuit on the front page of the data sheet in a differential configuration to achieve extremely high SFDR through high frequencies. That circuit is set up for a differential gain of 8.5V/V from a differential input signal to the output. Using the transformer shown will improve the noise figure and translate from a single to a differential

signal but, if the source is differential already, it may be fed directly into the gain setting resistors. To set the compensation capacitors (C_S and C_F), consider the 1/2 circuit of Figure 4 where the 50Ω source is reflected through the 1:2 transformer and then cut in 1/2 and grounded to give a total impedance to AC ground (for the circuit on the front page of this data sheet) equal to the 200Ω.

Considering only the noise gain (this is the same as the non-inverting signal gain) for the circuit of Figure 4, the low frequency noise gain, (NG_1) will be set by the resistor ratios while the high frequency noise gain (NG_2) will be set by the capacitor ratios. The capacitor values set both the transition frequencies and the high frequency noise gain. If the high frequency noise gain, determined by $NG_2 = 1 + C_S/C_F$, is set to a value greater than the recommended minimum stable gain for the op amp, and the noise gain pole, set by $1/R_FC_F$, is placed correctly, a very well-controlled, second-order low pass frequency response will result.

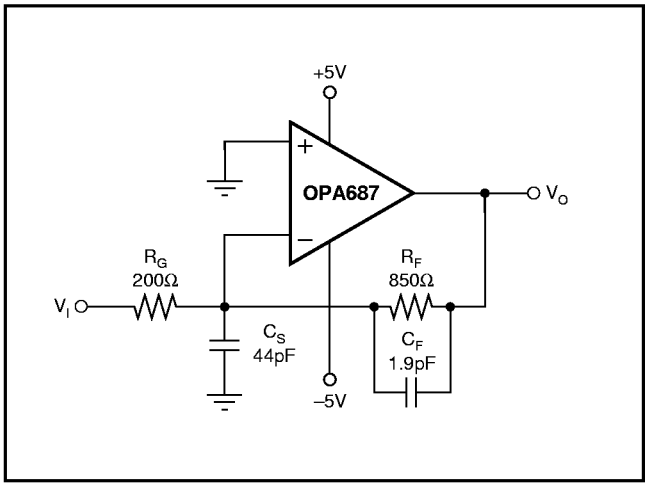


FIGURE 4. Broadband Low Inverting Gain External Compensation.

To choose the values for both C_S and C_F, two parameters and only three equations need to be solved. The first parameter is the target high frequency noise gain NG_2, which should be greater than the minimum stable gain for the OPA687. Here, a target NG_2 of 24 will be used. The second parameter is the desired low frequency signal gain, which also sets the low frequency noise gain NG_1. To simplify this discussion, we will target a maximally flat second-order low pass Butterworth frequency response (Q = 0.707). The signal gain of –4.25 shown in Figure 4 will set the low frequency noise gain to $NG_1 = 1 + R_F/R_G$ (= 5.25 in this example). Then, using only these two gains and the GBP for the OPA687 (3600MHz), the key frequency in the compensation can be determined as:

$$Z_O = \frac{GBP}{NG_1^2}\left[\left(1-\frac{NG_1}{NG_2}\right)-\sqrt{1-2\frac{NG_1}{NG_2}}\right]$$

Physically, this Z_0 (4.1MHz for the values shown above) is set by $1/(2\pi \bullet R_F(C_F + C_S))$ and is the frequency at which the rising portion of the noise gain would intersect unity gain if projected back to 0dB gain. The actual zero in the noise gain occurs at $NG_1 \bullet Z_0$ and the pole in the noise gain occurs at $NG_2 \bullet Z_0$. Since GBP is expressed in Hz, multiply Z_0 by 2π and use this to get C_F by solving:

$$C_F = \frac{1}{2\pi \bullet R_F Z_O NG_2} \quad (= 1.90pF)$$

Finally, since C_S and C_F set the high frequency noise gain, determine C_S by:

$$C_S = (NG_2 - 1)\,C_F \quad (= 43.8pF)$$

The resulting closed-loop bandwidth will be approximately equal to:

$$f_{-3dB} \cong \sqrt{Z_O\ GBP} \quad (= 121MHz)$$

For the values shown in Figure 4, the f_{-3dB} will be approximately 121MHz. This is less than that predicted by simply dividing the GBP product by NG_1. The compensation network controls the bandwidth to a lower value while providing the full slew rate at the output and an exceptional distortion performance due to increased loop gain at frequencies below $NG_1 \bullet Z_0$. The capacitor values shown in Figure 4 are calculated for $NG_1 = 5.25$ and $NG_2 = 24$ with no adjustment for parasitics. The full circuit on the front page of this datasheet shows the capacitors adjusted for parasitics.

Figure 5 shows the measured 2-tone, 3rd-order distortion for just the amplifier portion of the circuit shown on the front page (based on the analysis of Figure 4).

The upper curve is for a total 2-tone envelope of 4Vp-p, requiring two tones, each at 2Vp-p across the OPA687 outputs. The lower curve is for a 2Vp-p envelope requiring each tone to be 1Vp-p. The basic measurement dynamic range for the two close-in spurious tones is approximately 85dBc. The 4Vp-p test does not show measurable 3rd-order

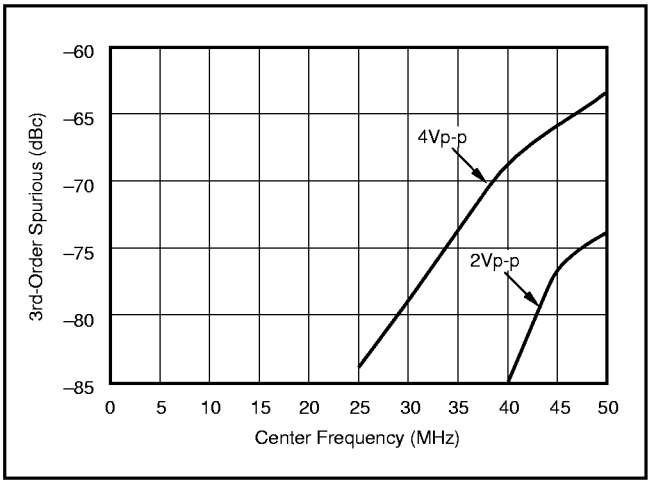


FIGURE 5. Measured 2-Tone, 3rd-Order Distortion for Differential ADC Driver.

spurious until 25MHz ,while the 2Vp-p is unmeasurable up to 40MHz center frequency. Two-tone, 2nd-order intermodulation distortion were unmeasurable for the circuit on the front page of this data sheet.

LOW NOISE FIGURE, HIGH DYNAMIC RANGE AMPLIFIER

The low input noise voltage of the OPA687 and its very high 2-tone intercept can be used to good advantage as a fixed-gain IF amplifier. While input noise figures in the 10dB range (for a matched 50Ω input) are easily achieved with just the OPA687, Figure 6 shows a technique to reduce the noise figure even further while providing a broadband, high gain IF amplifier stage using two stages of the OPA687.

This circuit uses two stages of forward gain with an overall feedback loop to set the input impedance match. The input transformer provides both a noiseless voltage gain and a signal inversion to retain an overall non-inverting signal path from P_I to P_O—since the 2nd amplifier stage is inverting to provide the correct feedback polarity through the 6.19kΩ resistor. To achieve a 50Ω input match at the primary of the 1:2 transformer, the secondary must see a 200Ω load impedance. At higher frequencies, the match is provided by the 200Ω resistor in series with 10pF. At lower signal frequencies (f < 80MHz), the input match is set by the feedback through the 6.19kΩ resistor. The low noise figure (5dB) for this circuit is achieved by using the transformer, the low voltage noise OPA687, and the input match set by feedback. The first stage amplifier provides a gain of +15. The very high SFDR is provided by operating the output stage a low signal gain of –2 and using the inverting compensation to hold it stable. Depending on the load that is driven, this circuit can give a 2-tone SFDR that exceeds 90dB through 30MHz. Besides offering a very high dynamic range, this circuit improves on standard IF amplifiers by offering a precisely controlled gain and a very flexible output interface capability.

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

Two PC boards are available to assist in the initial evaluation of circuit performance using the OPA687 in its two package styles. Both of these are available free as an unpopulated PC board delivered with descriptive documentation. The summary information for these boards is shown in the table below.

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
OPA687U	8-Pin SO-8	DEM-OPA68xU	MKT-351
OPA687N	6-Lead SOT23-6	DEM-OPA6xxN	MKT-348

Contact the Burr-Brown applications support line to request any of these boards.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA687 is available through either the Burr-Brown Internet web page (http://www.burr-brown.com) or as one model on a disk from the Burr-Brown Applications department (1-800-548-6132). The Applications department is also available for design assistance at this number. These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance.

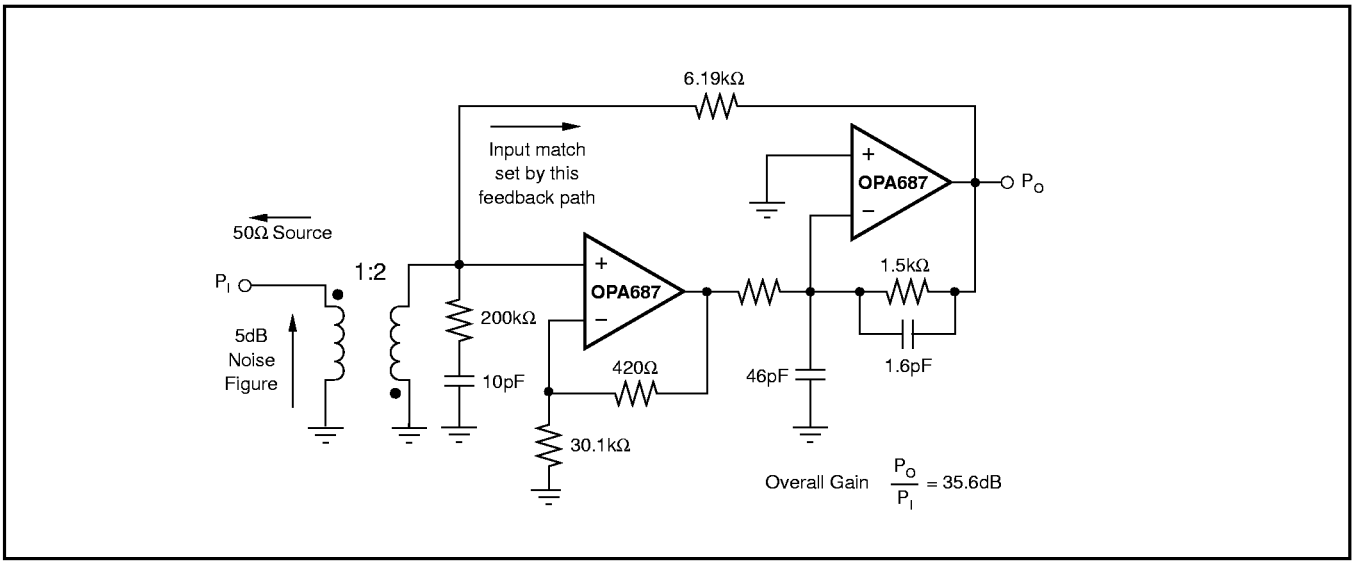


FIGURE 6. Very High Dynamic Range High Gain Amplifier.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO MINIMIZE NOISE

The OPA687 provides a very low input noise voltage while requiring a low 18.5mA of quiescent current. To take full advantage of this low input noise, careful attention to the other possible noise contributors is required. Figure 7 shows the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

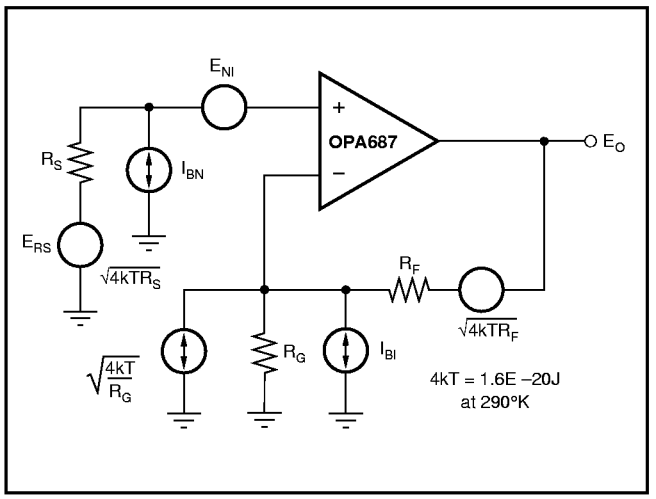


FIGURE 7. Op Amp Noise Analysis Model.

The total output spot-noise voltage can be computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, then taking the square root to get back to a spot-noise voltage. Equation 1 shows the general form for this output noise voltage using the terms shown in Figure 7.

Equation 1

$$E_O = \sqrt{\left(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right)NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG}$$

Dividing this expression by the noise gain (NG = 1 + R_F/R_G) will give the equivalent input-referred, spot-noise voltage at the non-inverting input as shown in Equation 2.

Equation 2

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Putting high resistor values into Equation 2 can quickly dominate the total equivalent input-referred noise. A source impedance on the non-inverting input of 56Ω will add a Johnson voltage noise term equal to just that for the amplifier itself. Holding the gain and source resistors low (as was used in the Typical Performance Curves) will minimize the resistor noise contribution in Equation 2. Evaluating Equation 2 for the circuit of Figure 1 will give a total equivalent input noise of 1.4nV/$\sqrt{Hz}$. This is slightly increased from the 0.95nV/$\sqrt{Hz}$ for the op amp itself due to the contribution of the resistor and bias current noise terms.

FREQUENCY RESPONSE CONTROL

Voltage feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the GBP shown in the specifications. Ideally, dividing GBP by the non-inverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high gain configurations. At low gains (increased feedback factors), most high-speed amplifiers will exhibit a more complex response with lower phase margin. The OPA687 is compensated to give a maximally flat 2nd-order Butterworth closed-loop response at a non-inverting gain of +20 (Figure 1). This results in a typical gain of +20 bandwidth of 290MHz, far exceeding that predicted by dividing the 3600MHz GBP by 20. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +50, the OPA687 will very nearly match the 72MHz bandwidth predicted using the simple formula and the typical GBP of 3600MHz.

Inverting operation offers some interesting opportunities to increase the available gain bandwidth product. When the source impedance is matched by the gain resistor (Figure 2), the signal gain is (1 + R_F/R_G) while the noise gain for bandwidth purposes is (1 + $R_F/2R_G$). This cuts the noise gain in half, increasing the minimum stable gain for inverting operation under these condition to –20 and the equivalent gain bandwidth product to 7.2GHz.

DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter, including additional external capacitance which may be recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier like the OPA687 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Performance Curves show the recommended R_S vs Capacitive Load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA687. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA687 output pin (see Board Layout Guidelines).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For the OPA687 operating in a gain of +20, the frequency response at the output pin is very flat to begin with, allowing relatively small values of R_S to be used for low capacitive loads. As the signal gain is increased, the unloaded phase margin will also increase. Driving capacitive loads at higher gains will require lower R_S values than shown for a gain of +20.

DISTORTION PERFORMANCE

The OPA687 is capable of delivering an exceptionally low distortion signal at high frequencies over a wide range of gains. The distortion plots in the Typical Performance Curves show the typical distortion under a wide variety of conditions. Most of these plots are limited to 110dB dynamic range. The OPA687's distortion driving a 500Ω load does not rise above –90dBc until either the signal level exceeds 3.0V and/or the fundamental frequency exceeds 5MHz.

Generally, until the fundamental signal reaches very high frequencies or powers, the 2nd harmonic will dominate the distortion with negligible 3rd harmonic component. Focusing then on the 2nd harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network, in the non-inverting configuration this is sum of $R_F + R_G$, while in the inverting configuration this is just R_F (Figure 2). Increasing output voltage swing increases harmonic distortion directly. A 6dB increase in output swing will generally increase the 2nd harmonic 12dB and the 3rd harmonic 18dB. Increasing the signal gain will also increase the 2nd harmonic distortion. Again, a 6dB increase in gain will increase the 2nd and 3rd harmonic by about 6dB even with a constant output power and frequency. And finally, the distortion increases as the fundamental frequency increases due to the roll-off in the loop gain with frequency. Conversely, the distortion will improve going to lower frequencies down to the dominant open-loop pole at approximately 200kHz.

In most applications, the 2nd harmonic will set the limit to dynamic range. Even order non-linearities arise from slight imbalances between the positive and negative halves of an output sinusoid. These imbalanced non-linearities arise from such mechanisms as voltage dependent base-collector capacitances and imbalanced source impedances looking out of the two amplifier power pins. Once a circuit and board layout has been determined, these imbalances can typically be nulled out by adjusting the DC operating point for the signal. An example DC tune is shown in Figure 8. This circuit has a DC-coupled inverting signal path to the output pin that provides gain for a small DC offsetting signal brought into the non-inverting input pin. The output is AC-coupled to block off this DC operating point from interacting with the next stage.

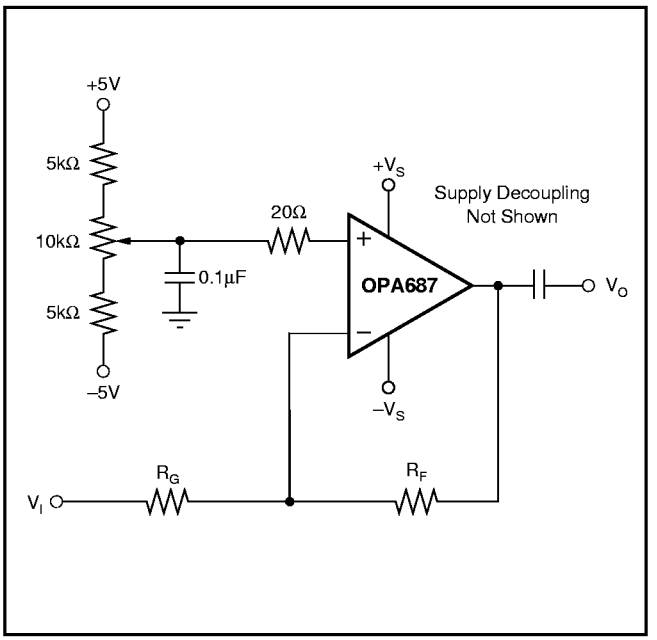


FIGURE 8. DC Adjustment for 2nd Harmonic Distortion.

For a 1Vp-p output swing in the 10MHz to 20MHz region, an output DC voltage in the ±1.5V range will null the 2nd harmonic distortion. Tests into a 200Ω converter input load have shown > 20dB decrease in the 2nd harmonic using this technique. Once the required voltage is found for a particular board, circuit, and signal requirement, that voltage is very repeatable from part to part and may be set permanently on the non-inverting input. Minimal degradation this improved 2nd harmonic distortion over temperature will be observed. An alternative means to eliminate the 2nd harmonic distortion is to operate two OPA687's differentially as shown on the front page of the data sheet. Both single-tone and 2-tone 2nd harmonic distortions for this differential configuration are essentially unmeasureable through 30MHz.

The OPA687 has an extremely low 3rd-order harmonic distortion. This also gives a high 2-tone, 3rd-order intermodulation intercept as shown in the Typical Performance Curves. This intercept curve is defined at the 50Ω load when driven through a 50Ω matching resistor to allow direct comparisons to RF MMIC devices. This network attenuates the voltage swing from the output pin to the load by 6dB. If the OPA687 drives directly into the input of a high impedance device, such as an ADC, this 6dB attenuation is not taken. Under these conditions, the intercept will increase by a minimum 6dBm. The intercept is used to

predict the intermodulation spurious for two closely-spaced frequencies. If the two test frequencies, f_1 and f_2, are specified in terms of average and delta frequency, $f_O = (f_1 + f_2)/2$ and $\Delta f = |f_2 - f_1|/2$, the two, 3-order, close-in spurious tones will appear at $f_O \pm 3 \bullet \Delta f$. The difference between two equal test-tone power levels and these intermodulation spurious power levels is given by (dBc = 2 • (IM3 – P_O)) where IM3 is the intercept taken from the Typical Performance Curve and P_O is the power level in dBm at the 50Ω load for one of the two, closely-spaced test frequencies. For instance, at 20MHz, the OPA687—at a gain of +20, has an intercept of 43dBm at a matched 50Ω load. If the full envelope of the two frequencies needs to be 2Vp-p, this requires each tone to be 4dBm. The 3rd-order intermodulation spurious tones will then be 2 • (43 – 4)=78dBc below the test-tone power level (–74dBm). If this same 2Vp-p, 2-tone envelope were delivered directly into the input of an ADC without the matching loss or the loading of the 50Ω network, the intercept would increase to at least 49dBm. With the same signal and gain conditions, but now driving directly into a light load, the spurious tones will then be at least 2 • (49 – 4) = 90dBc below the 4dBm test-tone power levels centered on 20MHz. Tests have shown that, in reality, they are much lower due to the lighter loading presented by most ADCs.

DC ACCURACY AND OFFSET CONTROL

The OPA687 can provide excellent DC signal accuracy due to its high open-loop gain, high common-mode rejection, high power supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of its low ±1.0mV input offset voltage, careful attention to input bias current cancellation is also required. The low noise input stage for the OPA687 has a relatively high input bias current (20µA typ into the pins) but with a very close match between the two input currents—typically ±200nA input offset current. The total output offset voltage may be considerably reduced by matching the source impedances looking out of the two inputs. For example, one way to add bias current cancellation to the circuit of Figure 1 would be to insert a 12.1Ω series resistor into the non-inverting input from the 50Ω terminating resistor. When the 50Ω source resistor is DC-coupled, this will increase the source impedance for the non-inverting input bias current to 37.1Ω. Since this is now equal to the impedance looking out of the inverting input ($R_F \| R_G$) for Figure 1, the circuit will cancel the gains for the bias currents to the output leaving only the offset current times the feedback resistor as a residual DC error term at the output. Using the 750Ω feedback resistor, this output error will now be less than ±1.8µA • 750Ω = ±1.4mV over the full temperature range for the circuit of Figure 1 with a 12.1Ω resistor added as described. The output DC offset will then be dominated by the input offset voltage multiplied by the signal gain. For the circuit of Figure 1, this will give a worst-case output DC offset of ±1.6mV • 20 = ±32mV over the full temperature range.

A fine-scale output offset null, or DC operating point adjustment is sometimes required. Numerous techniques are available for introducing a DC offset control into an op amp circuit. Most of these techniques eventually reduce to setting up a DC current through the feedback resistor. One key consideration to selecting a technique is to insure that it has a minimal impact on the desired signal path frequency response. If the signal path is intended to be non-inverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the non-inverting input can be considered. For a DC-coupled inverting input signal, this DC offset signal will set up a DC current back into the source that must be considered. An offset adjustment placed on the inverting op amp input can also change the noise gain and frequency response flatness. Figure 9 shows one example of an offset adjustment for a DC-coupled signal path that will have minimum impact on the signal frequency response. In this case, the input is brought into an inverting gain resistor with the DC adjustment and additional current summed into the inverting node. The resistor values setting this offset adjustment are much larger than the signal path resistors. This will insure that this adjustment has minimal impact on the loop gain and hence, the frequency response.

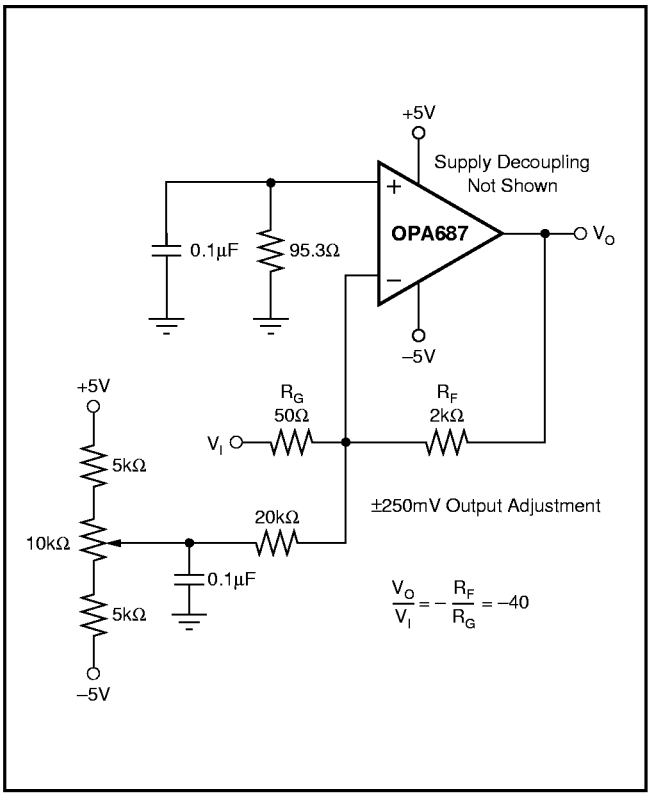


FIGURE 9. DC-Coupled, Inverting Gain of –40, with Offset Adjustment.

DISABLE OPERATION

The OPA687 provides an optional disable feature that may be used to reduce system power. If the $\overline{DIS}$ control pin is left unconnected, the OPA687 will operate normally. To disable, the control pin must be asserted low. Figure 10 shows a simplified internal circuit for the disable control feature.

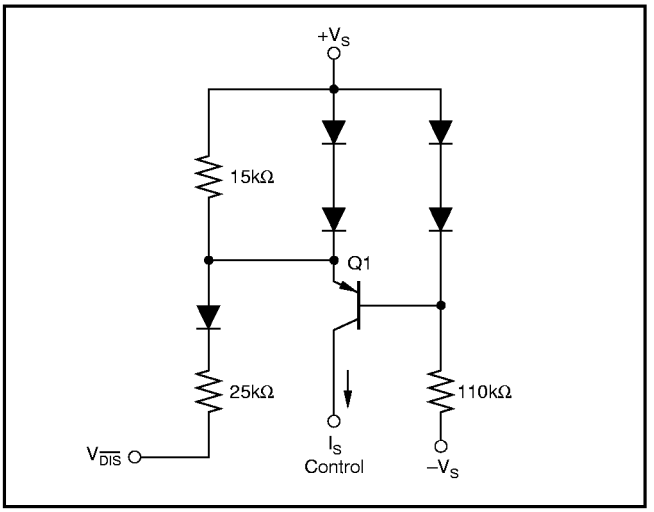


FIGURE 10. Simplified Disabled Control Circuit.

In normal operation, base current to Q1 is provided through the 110kΩ resistor while the emitter current through the 15kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{DIS}}$ is pulled low, additional current is pulled through the 15kΩ resistor, eventually turning on these two diodes (≈ 100µA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-based voltage of Q1 at approximately zero volts. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the disable mode are only those required to operate the circuit of Figure 10.

THERMAL ANALYSIS

The OPA687 will not require heatsinking or airflow in most applications. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading. This is the absolute highest power that can be dissipated for a given R_L. All actual applications will dissipate less power in the output stage.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As an absolute worst-case example, compute the maximum T_J using an OPA687N (SOT23-6 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load.

$P_D = 10V\ (20.5mA) + 5^2/(4 \bullet (100\Omega \parallel 789\Omega)) = 275mW$

Maximum $T_J = +85°C + (0.28W \bullet 150°C/W) = 127°C$

All actual applications will operate at a lower junction temperature than the 127°C computed above. Compute your actual output stage power to get an accurate estimate of maximum junction temperature, or use the results shown here as an absolute maximum.

BOARD LAYOUT

Achieving optimum performance with a high frequency amplifier like the OPA687 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the non-inverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA687. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wirewound type resistors in a high frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as non-inverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feed-

back resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 2.0kΩ, this parasitic capacitance can add a pole and/or a zero below 400MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. It has been suggested here that a good starting point for design would be set the R_G be set to 39.2Ω. Doing this will automatically keep the resistor noise terms low, and minimize the effect of their parasitic capacitance.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended R_S vs Capacitive Load. Low parasitic capacitive loads (< 4pF) may not need an R_S since the OPA687 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic cap. loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA687 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S vs Capacitive Load. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high speed part like the OPA687 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA687 onto the board.

INPUT AND ESD PROTECTION

The OPA687 is built using a very high speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 11.

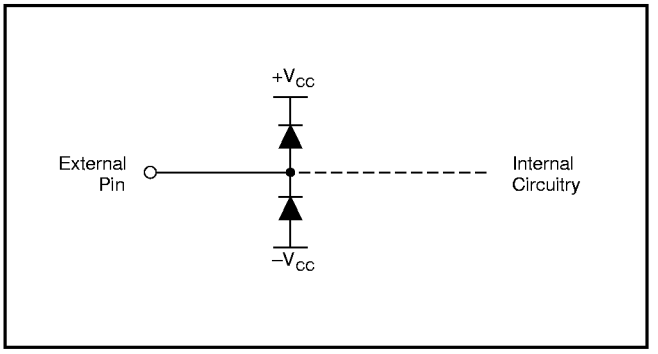
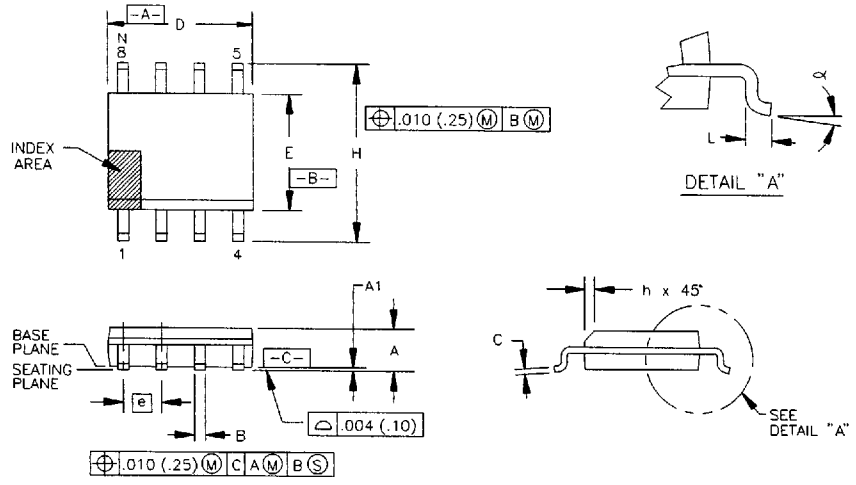


FIGURE 11. Internal ESD Protection.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g., in systems with ±15V supply parts driving into the OPA687), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

Package Number 182 - 8-Lead SOIC



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.23	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.20	0.25	
D	.189	.1968	4.80	4.98	2
E	.1497	.1574	3.80	4.00	3
e	.050 BASIC		1.27 BASIC		
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	4
L	.016	.050	0.41	1.27	5
N	8		8		6
α	0°	8°	0°	8°	

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER:	ZZ182	REV.: H
JEDEC NUMBER:	MS-012-AA	