

## 20 mΩ, Slew Rate Controlled Load Switch in WCSP6

### DESCRIPTION

SiP32458 and SiP32459 are slew rate controlled integrated high side load switches that operate in the input voltage range from 1.5 V to 5.5 V.

SiP32458 and SiP32459 are of P-channel MOSFET switching element with integrated gate pump that provides 20 mΩ switch on resistance over a wide input voltage range.

These devices have low voltage logic control threshold that can interface with low voltage control I/O directly without extra level shift or driver. A 2.8 MΩ pull-down resistor is integrated at logic control EN pin.

The slow slew rate of SiP32458 and SiP32459 in the range of 3 ms limits the in-rush current and minimized the switching noise.

The SiP32458 features a reverse current blocking capability while the SiP32459 features an integrated output discharge switch.

Both SiP32458 and SiP32459 are available in compact wafer level WCSP package, WCSP6 1 mm x 1.5 mm with 0.5 mm pitch.

### FEATURES

- Low input voltage, 1.5 V to 5.5 V
- Low  $R_{ON}$ , 20 mΩ typical at 5 V
- Slew rate control
- Low logic control
- Reverse current blocking when disabled (SiP32458, without output discharge switch)
- Integrated output discharge switch (SiP32459 only)
- Integrated pull down resistor at EN pin
- 6 bumps WCSP package
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?9991](http://www.vishay.com/doc?9991)



### APPLICATIONS

- Battery operated devices
- Smart phones
- GPS and PMP
- Computer
- Medical and healthcare equipment
- Industrial and instrument
- Cellular phones and portable media players
- Game console

### TYPICAL APPLICATION CIRCUIT

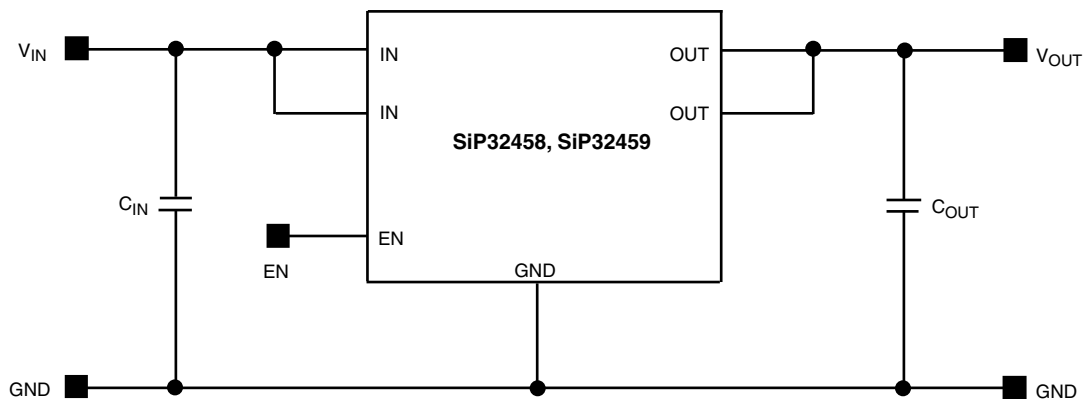


Figure 1 - SiP32458 and SiP32459 Typical Application Circuit

**ORDERING INFORMATION**

Temperature Range	Package	Marking	Part Number
- 40 °C to 85 °C	WCSP: 6 Bumps (2 x 3, 0.5 mm pitch, 250 µm bump height, 1.5 mm x 1 mm die size)	AA	SiP32458DB-T2-GE1
		AB	SiP32459DB-T2-GE1

Note:

GE1 denotes halogen-free and RoHS compliant

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Limit	Unit
Supply Input Voltage ( $V_{IN}$ )	- 0.3 to 6	V
Enable Input Voltage ( $V_{EN}$ )	- 0.3 to 6	
Output Voltage ( $V_{OUT}$ )	- 0.3 to 6	
Maximum Continuous Switch Current ( $I_{max.}$ )	3	A
Maximum Pulsed Current ( $I_{DM}$ ) $V_{IN}$ (Pulsed at 1 ms, 10 % Duty Cycle)	6	
ESD Rating (HBM)	4000	V
Junction Temperature ( $T_J$ )	- 40 to 150	°C
Thermal Resistance ( $\theta_{JA}$ ) <sup>a</sup>	110	°C/W
Power Dissipation ( $P_D$ ) <sup>a</sup>	500	mW

Notes:

a. Device mounted with all bumps soldered to PC board.

b. Derate 9.1 mW/°C above  $T_A = 70$  °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING RANGE**

Parameter	Limit	Unit
Input Voltage Range ( $V_{IN}$ )	1.5 to 5.5	V
Operating Junction Temperature Range	- 40 to 125	°C

SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Specified $V_{IN} = 1.5\text{ V to }5.5\text{ V}$ , $T_A = -40\text{ }^\circ\text{C to }85\text{ }^\circ\text{C}$ (Typical values are at $V_{IN} = 4.5\text{ V}$ , $T_A = 25\text{ }^\circ\text{C}$ )		Limits			Unit
				Min. <sup>a</sup>	Typ. <sup>b</sup>	Max. <sup>a</sup>	
Operating Voltage <sup>c</sup>	$V_{IN}$			1.5	-	5.5	V
Quiescent Current	$I_Q$	$V_{EN} = V_{IN}$ , OUT = open		-	4.2	9.5	$\mu\text{A}$
Off Supply Current	$I_{Q(off)}$	SiP32458	EN = GND, OUT = open	-	-	1	
		SiP32459		-	-	10	
Off Switch Current	$I_{DS(off)}$	EN = GND, OUT = 0 V		-	-	10	
Reverse Blocking Current	$I_{RB}$	$V_{OUT} = 2.5\text{ V}$ , $V_{IN} = 0.75\text{ V}$ , $V_{EN} = 0\text{ V}$ (SiP32458 only)		-	-	10	
On-Resistance	$R_{DS(on)}$	$V_{IN} = 1.5\text{ V}$ , $I_L = 500\text{ mA}$ , $T_A = 25\text{ }^\circ\text{C}$		-	30	36	$\text{m}\Omega$
		$V_{IN} = 1.8\text{ V}$ , $I_L = 500\text{ mA}$ , $T_A = 25\text{ }^\circ\text{C}$		-	26	32	
		$V_{IN} = 3.3\text{ V}$ , $I_L = 500\text{ mA}$ , $T_A = 25\text{ }^\circ\text{C}$		-	20	26	
		$V_{IN} = 5\text{ V}$ , $I_L = 1\text{ A}$ , $T_A = 25\text{ }^\circ\text{C}$		-	20	26	
On-Resistance Temp.-Coefficient	$TC_{RDS}$			-	2820	-	ppm/ $^\circ\text{C}$
Output Pulldown Resistance	$R_{PD}$	$V_{IN} = 3.3\text{ V}$ , $I_{OUT} = 5\text{ mA}$ , $V_{EN} = 0\text{ V}$ (SiP32459 only)		-	70	-	$\Omega$
EN Input Low Voltage <sup>c</sup>	$V_{IL}$	$V_{IN} = 1.5\text{ V}$		-	-	0.4	V
EN Input High Voltage <sup>c</sup>	$V_{IH}$	$V_{IN} = 5.5\text{ V}$		1	-	-	
EN Input Leakage	$I_{EN}$	$V_{IN} = 5.5\text{ V}$ , $V_{EN} = 0\text{ V}$		-	-	1	$\mu\text{A}$
		$V_{IN} = 5.5\text{ V}$ , $V_{EN} = 1.2\text{ V}$		-	0.44	1	
EN Pull Down Resistor	$R_{EN}$	$V_{IN} = 5.5\text{ V}$ , $V_{EN} = 1.2\text{ V}$		-	2.8	-	$\text{M}\Omega$
Output Turn-On Delay Time	$t_{d(on)}$	$V_{IN} = 4.5\text{ V}$ , $R_{LOAD} = 5\text{ }\Omega$ , $C_L = 100\text{ }\mu\text{F}$ , $T_A = 25\text{ }^\circ\text{C}$		-	0.5	-	ms
Output Turn-On Rise Time	$t_r$			-	3	-	
Output Turn-Off Delay Time	$t_{d(off)}$			-	18	-	

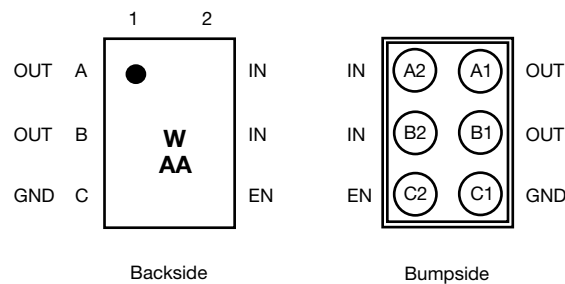
Notes:

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

 c. For  $V_{IN}$  outside this range consult typical EN threshold curve.

## PIN CONFIGURATION


**Figure 2 - WCSP 2 x 3 Package**

PIN DESCRIPTION		
Pin Number	Name	Function
A1, B1	OUT	These are the output pins of the switch
C1	GND	Ground connection
A2, B2	IN	These are input pins of the switch
C2	EN	Enable input

## BLOCK DIAGRAM

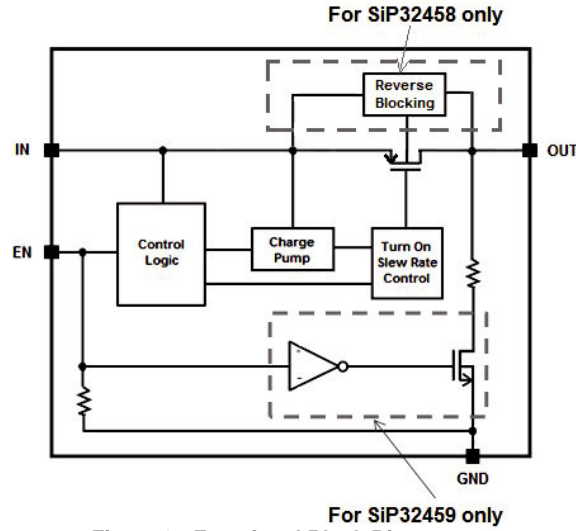


Figure 3 - Functional Block Diagram

## TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

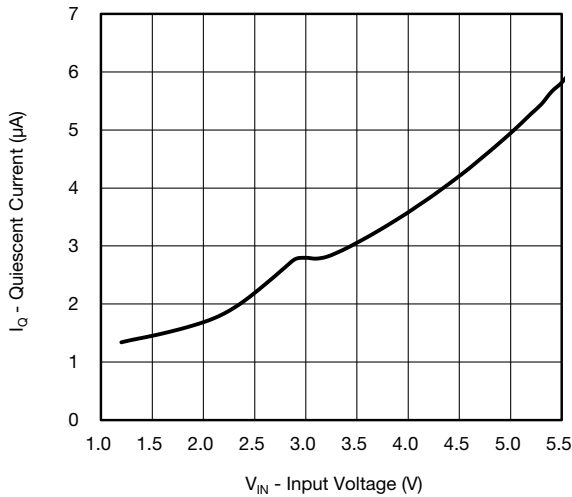


Figure 4 - Quiescent Current vs. Input Voltage

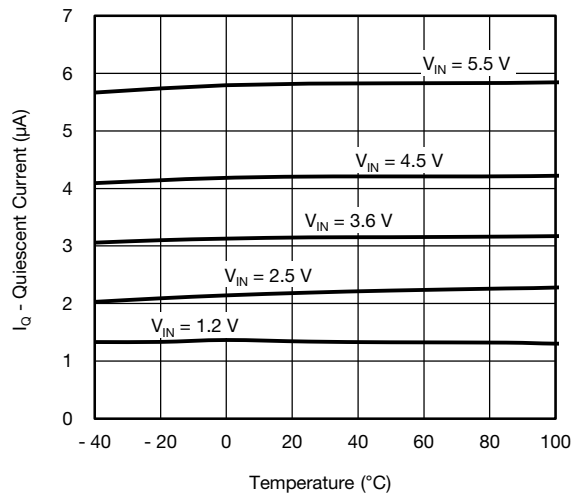


Figure 6 - Quiescent Current vs. Temperature

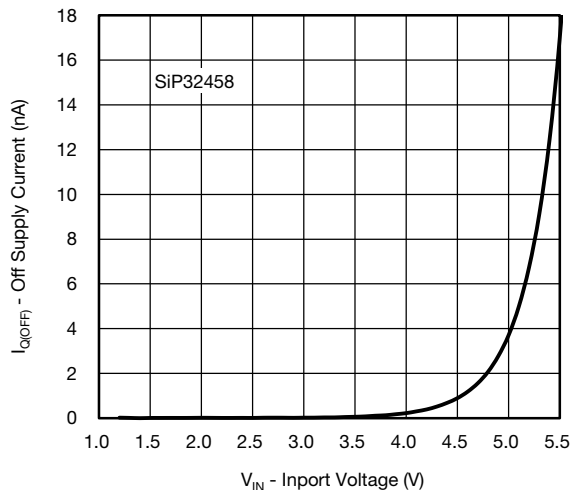


Figure 5 - Off Supply Current vs. Input Voltage

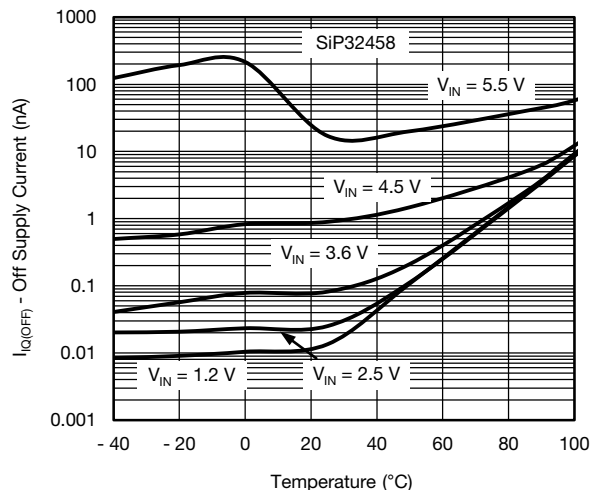
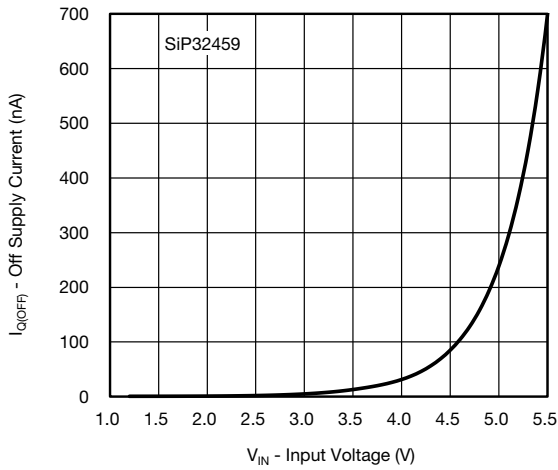
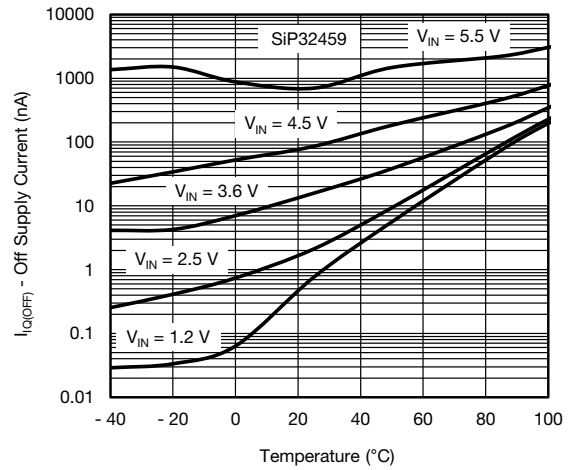


Figure 7 - Off Supply Current vs. Temperature

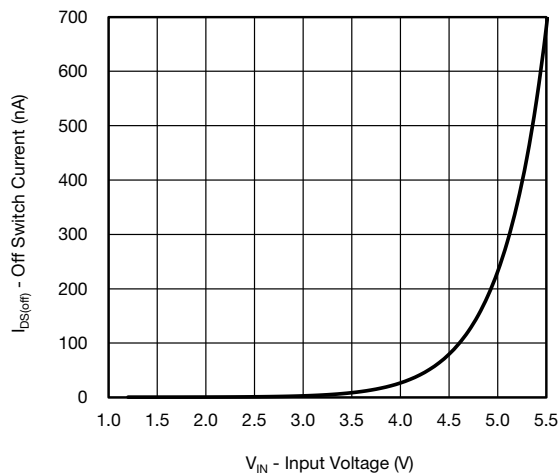
**TYPICAL CHARACTERISTICS** (internally regulated, 25 °C, unless otherwise noted)



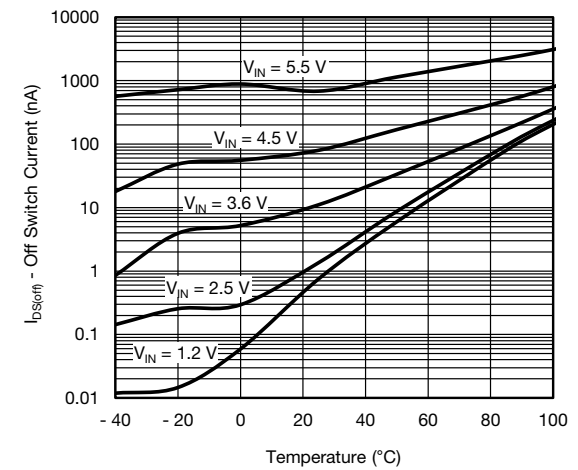
**Figure 8 - Off Supply Current vs. Input Voltage**



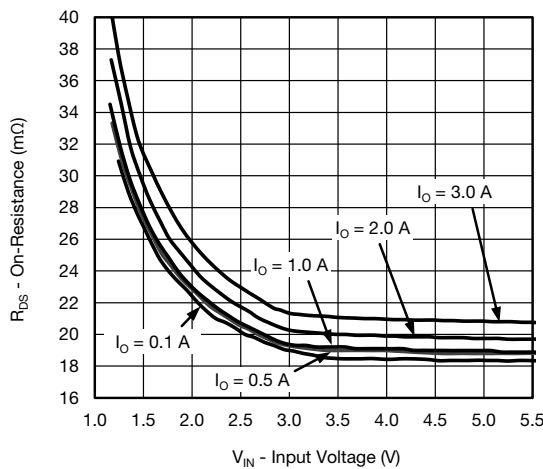
**Figure 11 - Off Supply Current vs. Temperature**



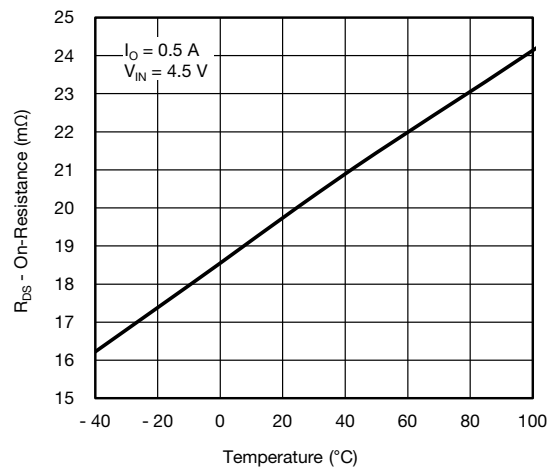
**Figure 9 - Off Switch Current vs. Input Voltage**



**Figure 12 - Off Switch Current vs. Temperature**



**Figure 10 -  $R_{DS(on)}$  vs. Input Voltage**



**Figure 13 -  $R_{DS(on)}$  vs. Temperature**

### TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

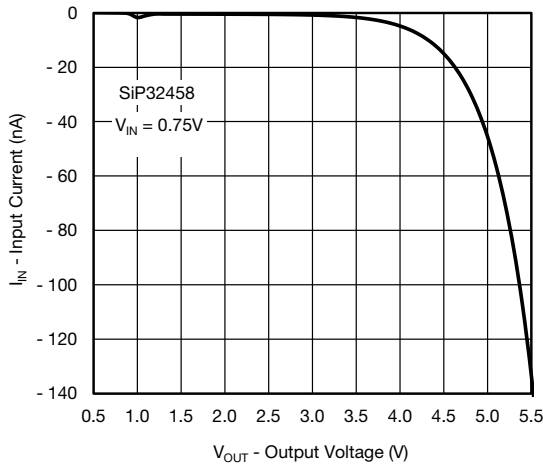


Figure 14 - Reverse Blocking Current vs. Output Voltage

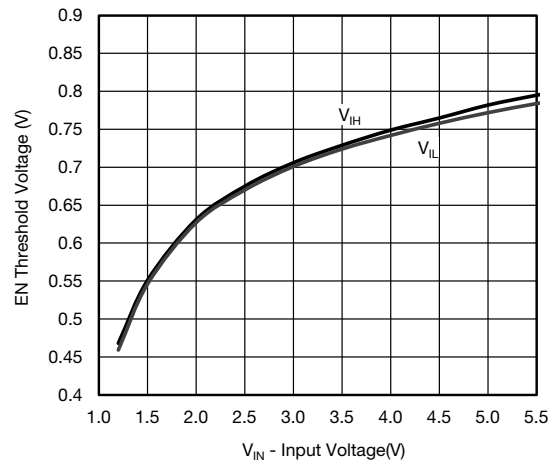


Figure 17 - EN Threshold Voltage vs. Input Voltage

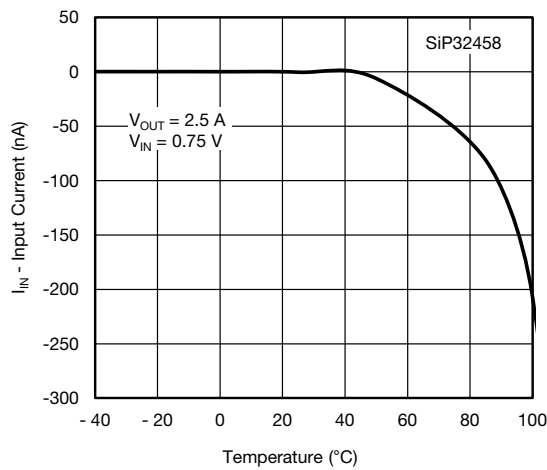


Figure 15 - Reverse Blocking Current vs. Temperature

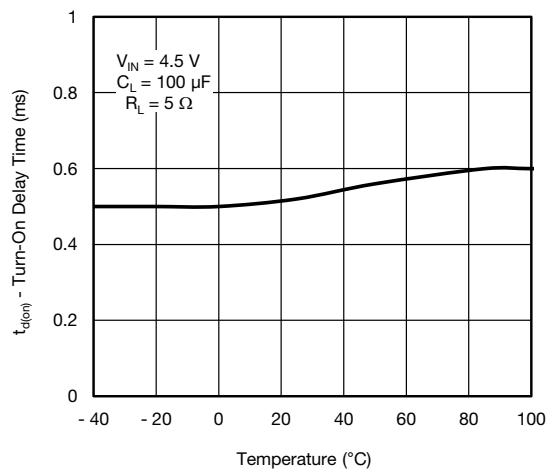


Figure 18 - Turn-On Delay Time vs. Temperature

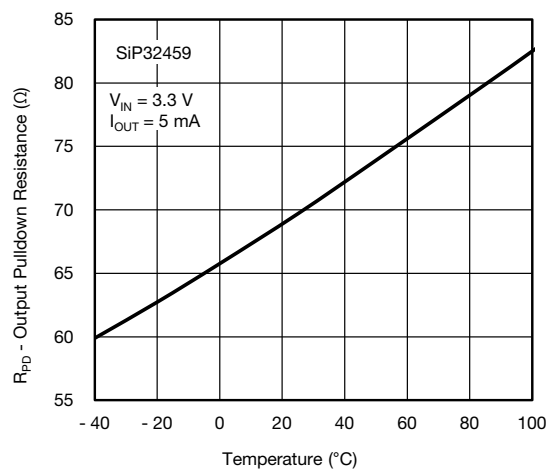


Figure 16 - Output Pulldown Resistance vs. Temperature

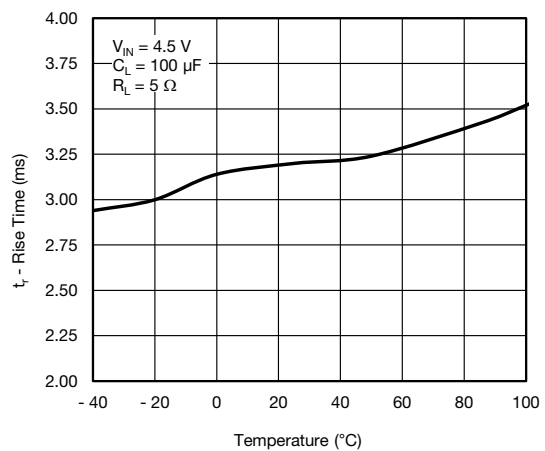


Figure 19 - Rise Time vs. Temperature

**TYPICAL CHARACTERISTICS** (internally regulated, 25 °C, unless otherwise noted)

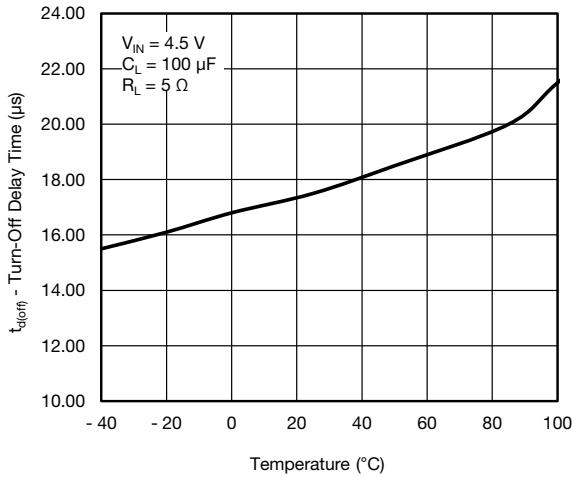


Figure 20 - Turn-Off Delay Time vs. Temperature

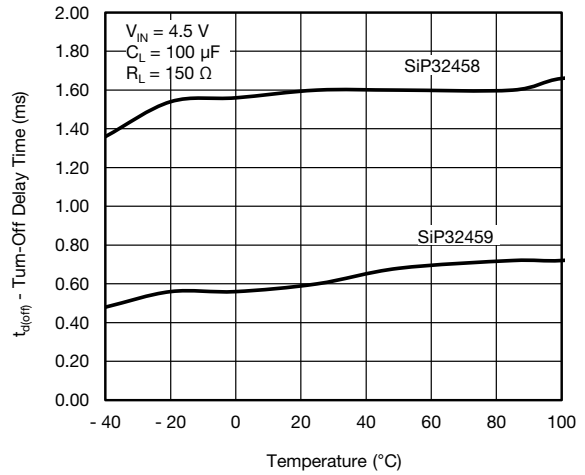


Figure 21 - Turn-Off Delay Time vs. Temperature

**TYPICAL WAVEFORMS**

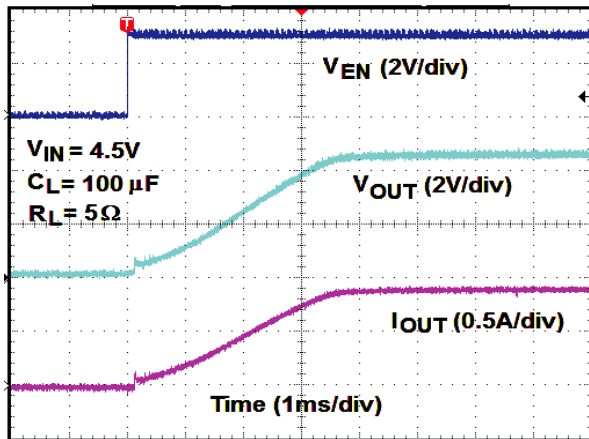


Figure 22 - Turn-On Time  
( $V_{IN} = 4.5 V$ ,  $R_L = 5 \Omega$ ,  $C_L = 100 \mu F$ )

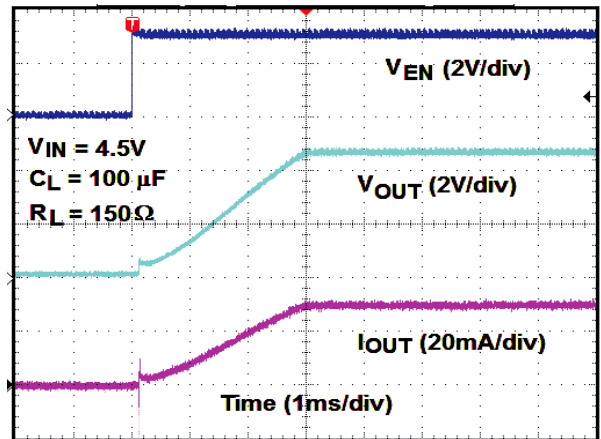


Figure 24 - Turn-On Time  
( $V_{IN} = 4.5 V$ ,  $R_L = 150 \Omega$ ,  $C_L = 100 \mu F$ )

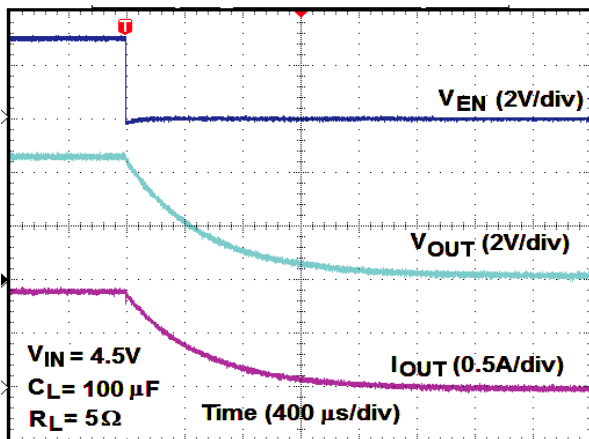


Figure 23 - Turn-Off Time  
( $V_{IN} = 4.5 V$ ,  $R_L = 5 \Omega$ ,  $C_L = 100 \mu F$ )

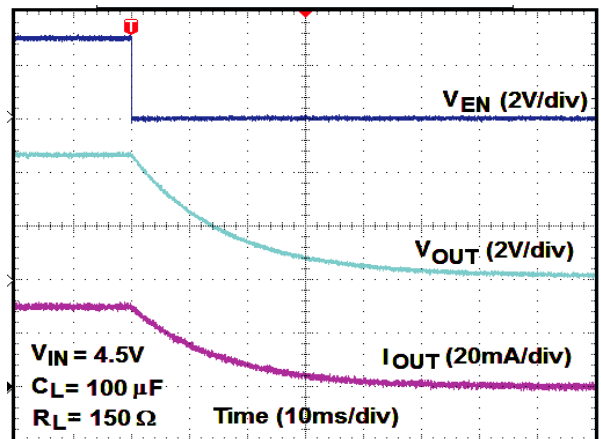


Figure 25 - Turn-Off Time, SiP32458  
( $V_{IN} = 4.5 V$ ,  $R_L = 150 \Omega$ ,  $C_L = 100 \mu F$ )

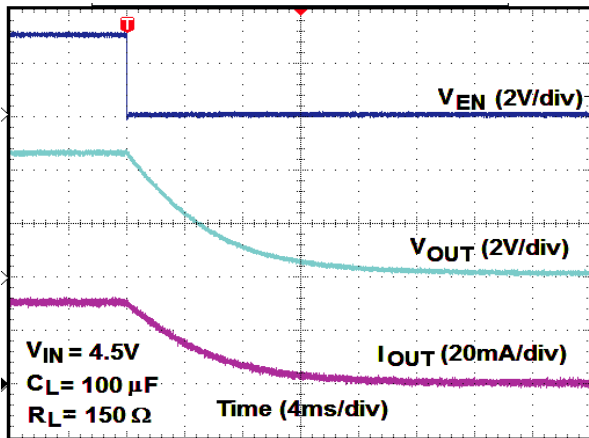


Figure 26 - Turn-Off Time, SiP32459  
( $V_{IN} = 4.5\text{ V}$ ,  $R_L = 150\ \Omega$ ,  $C_L = 100\ \mu\text{F}$ )

## DETAILED DESCRIPTION

SiP32458 and SiP32459 are P-channel power MOSFET designed as high side load switches. They incorporate a negative charge pump at the gate to keep the gate to source voltage high when turned on therefore keep the on resistance low at lower input voltage range. SiP32458 and SiP32459 are designed with slow slew rate to minimize the inrush current during turn on. The SiP32458 has a reverse blocking circuit to prevent the current from going back to the input in case the output voltage is higher than the input voltage. The SiP32459 has an output pulldown resistor to discharge the output capacitance when the device is off.

## APPLICATION INFORMATION

### Input Capacitor

While a bypass capacitor on the input is not required, a 4.7  $\mu\text{F}$  or larger capacitor for  $C_{IN}$  is recommended in almost all applications. The bypass capacitor should be placed as physically close as possible to the input pin to be effective in minimizing transients on the input. Ceramic capacitors are recommended over tantalum because of their ability to withstand input current surges from low impedance sources such as batteries in portable devices.

### Output Capacitor

A 0.1  $\mu\text{F}$  capacitor across  $V_{OUT}$  and GND is recommended to insure proper slew operation. There is inrush current through the output MOSFET and the magnitude of the inrush current depends on the output capacitor, the bigger the  $C_{OUT}$  the higher the inrush current. There are no ESR or capacitor type requirement.

### Enable

The EN pin is compatible with CMOS logic voltage levels. It requires at least 0.4 V or below to fully shut down the device and 1 V or above to fully turn on the device. There is a 2.8  $\text{M}\Omega$  resistor connected between EN pin and GND pin.

## Protection Against Reverse Voltage Condition

The SiP32458 contains the reverse blocking circuit to keep the output current from flowing back to the input in case the output voltage is higher than the input voltage.

## Thermal Considerations

These devices are designed to maintain a constant output load current. Due to physical limitations of the layout and assembly of the device the maximum switch current is 3 A as stated in the Absolute Maximum Ratings table. However, another limiting characteristic for the safe operating load current is the thermal power dissipation of the package. To obtain the highest power dissipation (and a thermal resistance of 110  $^{\circ}\text{C}/\text{W}$ ) the device should be connected to a heat sink on the printed circuit board.

The maximum power dissipation in any application is dependant on the maximum junction temperature,  $T_{J(\text{max.})} = 125\ ^{\circ}\text{C}$ , the junction-to-ambient thermal resistance,  $\theta_{J-A} = 110\ ^{\circ}\text{C}/\text{W}$ , and the ambient temperature,  $T_A$ , which may be formulaically expressed as:

$$P(\text{max.}) = \frac{T_J(\text{max.}) - T_A}{\theta_{J-A}} = \frac{125 - T_A}{280}$$

It then follows that, assuming an ambient temperature of 70  $^{\circ}\text{C}$ , the maximum power dissipation will be limited to about 500 mW.

So long as the load current is below the 3 A limit, the maximum continuous switch current becomes a function two things: the package power dissipation and the  $R_{DS(\text{ON})}$  at the ambient temperature.

As an example let us calculate the worst case maximum load current at  $T_A = 70\ ^{\circ}\text{C}$ . The worst case  $R_{DS(\text{ON})}$  at 25  $^{\circ}\text{C}$  is 36  $\text{m}\Omega$  at  $V_{IN} = 1.5\ \text{V}$ . The  $R_{DS(\text{ON})}$  at 70  $^{\circ}\text{C}$  can be extrapolated from this data using the following formula:

$$R_{DS(\text{ON})}(\text{at } 70\ ^{\circ}\text{C}) = R_{DS(\text{ON})}(\text{at } 25\ ^{\circ}\text{C}) \times (1 + T_C \times \Delta T)$$

Where  $T_C$  is 2820 ppm/ $^{\circ}\text{C}$ . Continuing with the calculation we have

$$R_{DS(\text{ON})}(\text{at } 70\ ^{\circ}\text{C}) = 36\ \text{m}\Omega \times (1 + 0.00282 \times (70\ ^{\circ}\text{C} - 25\ ^{\circ}\text{C})) = 40.5\ \text{m}\Omega$$

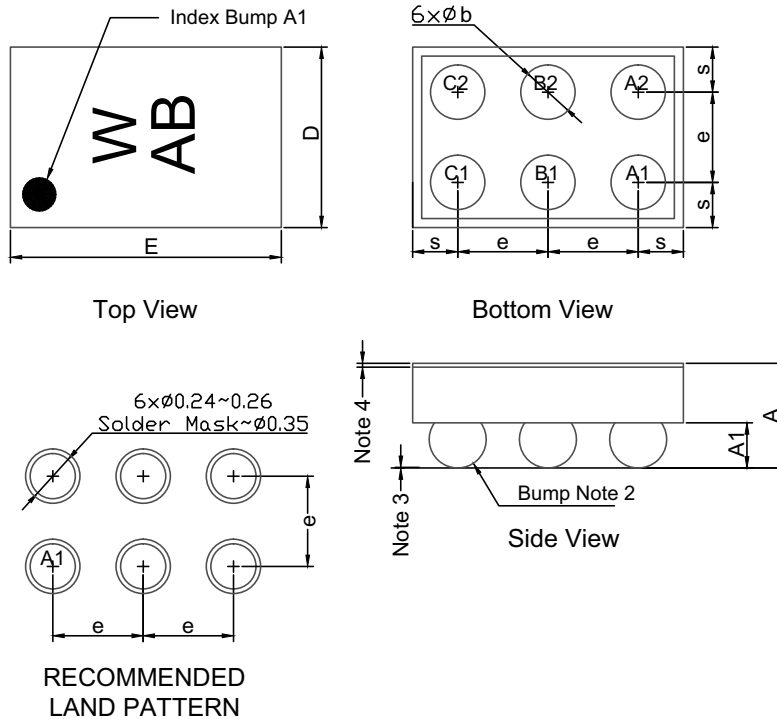
The maximum current limit is then determined by

$$I_{\text{LOAD}}(\text{max.}) < \sqrt{\frac{P(\text{max.})}{R_{DS(\text{ON})}}}$$

which in this case is 3.5 A. Under the stated input voltage condition, if the 3.5 A current limit is exceeded the internal die temperature will rise and eventually, possibly damage the device.

To avoid possible permanent damage to the device and keep a reasonable design margin, it is recommended to operate the device maximum up to 3 A only as listed in the Absolute Maximum Ratings table.



**PACKAGE OUTLINE**
**WCSP: 6 Bumps (2 x 3, 0.5 mm Pitch, 250 μm Bump Height, 1 mm x 1.5 mm Die Size)**


Dimension	MILLIMETERS <sup>5</sup>			INCHES		
	Min.	Nom.	MAX.	Min.	Nom.	MAX.
A	0.540	0.572	0.620	0.0212	0.0225	0.0244
A1	0.214	0.250	0.286	0.0084	0.0098	0.0113
b	0.279	0.310	0.372	0.0109	0.0122	0.0146
e	0.500			0.0197		
s	0.230	0.250	0.270	0.0090	0.0098	0.0106
D	0.920	0.960	1.000	0.0362	0.0378	0.0394
E	1.420	1.460	1.500	0.0559	0.0575	0.0591

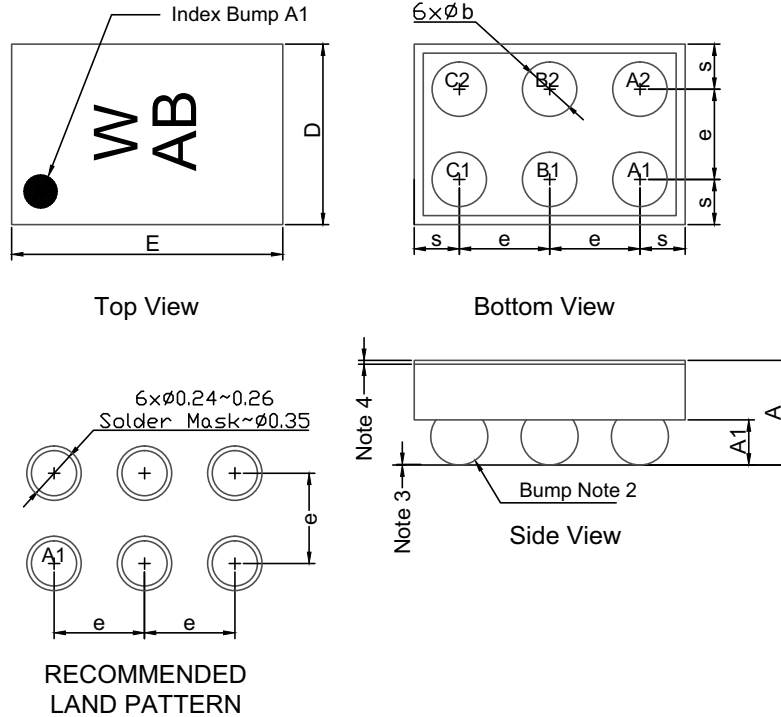
**Notes** (unless otherwise specified)

1. Laser mark on the silicon die back coated with an epoxy film.
2. Bumps are SAC396.
3. 0.050 max. co-planarity.
4. Laminate tape thickness is 0.022 mm.
5. Use millimeters as the primary measurement.

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### WCSP6: 6 Bumps

(2 x 3, 0.5 mm pitch, 250 μm bump height, 1 mm x 1.5 mm die size)



DIMENSION	MILLIMETERS <sup>(5)</sup>			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.540	0.572	0.620	0.0212	0.0225	0.0244
A1	0.214	0.250	0.286	0.0084	0.0098	0.0113
b	0.279	0.310	0.372	0.0109	0.0122	0.0146
e	0.500			0.0197		
s	0.230	0.250	0.270	0.0090	0.0098	0.0106
D	0.920	0.960	1.000	0.0362	0.0378	0.0394
E	1.420	1.460	1.500	0.0559	0.0575	0.0591

**Notes** (unless otherwise specified)

- (1) Laser mark on the silicon die back coated with an epoxy film.
- (2) Bumps are SAC396.
- (3) 0.050 max. co-planarity.
- (4) Laminate tape thickness is 0.022 mm.
- (5) Use millimeters as the primary measurement.

ECN: S13-1424-Rev. B, 01-Jul-13  
 DWG: 6011



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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**