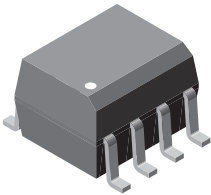
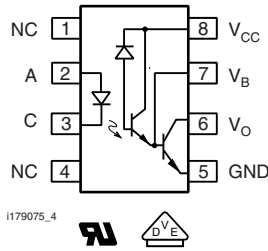




High Speed Optocoupler, 100 kBd, Low Input Current, High Gain



1179074



FEATURES

- High current transfer ratio, 300 %
- Low input current, 0.5 mA
- High output current, 60 mA
- TTL compatible output, V_{OL} = 0.1 V
- Adjustable bandwidth access to base
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS COMPLIANT

DESCRIPTION

Very high current ratio together with 4000 V_{RMS} isolation are achieved by coupling an LED with an integrated high gain photo detector in a SOIC-8 package. Separate pins for the photo diode and output stage enable TTL compatible saturation voltages with high speed operation. Photodarlington operation is achieved by tying the V_{CC} and V_O terminals together. Access to the base terminal allows adjustment to the gain bandwidth.

The SFH6318 is ideal for TTL applications since the 300 % minimum current transfer ratio with an LED current of 1.6 mA enables operation with one unit load-in and one unit load-out with a 2.2 kΩ pull-up resistor.

The SFH6319 is best suited for low power logic applications involving CMOS and low power TTL. A 400 % current transfer ratio with only 0.5 mA of LED current is guaranteed from 0 °C to 70 °C.

Caution:

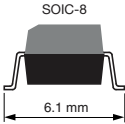
Due to the small geometries of this device, it should be handled with electrostatic discharge (ESD) precautions. Proper grounding would prevent damage further and / or degradation which may be induced by ESD.

APPLICATIONS

- Logic ground isolation - TTL / TTL, TTL / CMOS, CMOS / CMOS, CMOS / TTL
- EIA RS 232C line receiver
- Low input current line receiver long lines, party lines
- Telephone ring detector
- Line voltage status indication - low input power dissipation
- Low power systems - ground isolation

AGENCY APPROVALS

- UL1577, file no. E52744
- cUL, file no. E52744
- DIN EN 60747-5-5 (VDE 0884-5) available with option 1
- CSA 93751

ORDERING INFORMATION		
<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="border: 1px solid black; padding: 2px 5px;">S</div> <div style="border: 1px solid black; padding: 2px 5px;">F</div> <div style="border: 1px solid black; padding: 2px 5px;">H</div> <div style="border: 1px solid black; padding: 2px 5px;">6</div> <div style="border: 1px solid black; padding: 2px 5px;">3</div> <div style="border: 1px solid black; padding: 2px 5px;">#</div> <div style="border: 1px solid black; padding: 2px 5px;">#</div> <div style="border: 1px solid black; padding: 2px 5px;">T</div> </div> <p style="text-align: center;">PART NUMBER</p>		
		
AGENCY CERTIFIED / PACKAGE	CTR (%)	
UL, CSA	≥ 300	≥ 500
SOIC-8	SFH6318T	SFH6319T
SOIC-8, tube	SFH6318	SFH6319



ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)					
PARAMETER	TEST CONDITION	PART	SYMBOL	VALUE	UNIT
INPUT					
Reverse voltage			V_R	3	V
Supply and output voltage	V_{CC} (pin 8 to 5), V_O (pin 6 to 5)	SFH6318	V_{CC}, V_O	-0.5 to 7	V
		SFH6319	V_{CC}, V_O	-0.5 to 18	V
Input power dissipation			P_{diss}	35	mW
Derate linearly above				50	$^{\circ}\text{C}$
Free air temperature				0.7	mW/ $^{\circ}\text{C}$
Average input current			$I_{F(AVG)}$	20	mA
Peak input current	50 % duty cycle; 1 ms pulse width		I_{FRM}	40	mA
Peak transient input current	$t_p \leq 1\text{ }\mu\text{s}$, 300 pps		I_{FSM}	1	A
OUTPUT					
Output current (pin 6)			I_O	60	mA
Emitter-base reverse current (pin 5 to 7)				0.5	V
Output power dissipation			P_{diss}	150	mW
Derate linearly from 25 $^{\circ}\text{C}$				2	mW/ $^{\circ}\text{C}$
COUPLER					
Storage temperature			T_{stg}	-55 to +125	$^{\circ}\text{C}$
Lead soldering temperature	$t = 10\text{ s}$		T_{slid}	260	$^{\circ}\text{C}$
Junction temperature			T_j	100	$^{\circ}\text{C}$
Ambient temperature range			T_{amb}	-55 to +100	$^{\circ}\text{C}$

Note

- Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability.

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
INPUT						
Forward voltage	$I_F = 1.6\text{ mA}$	V_F	-	1.4	1.7	V
Temperature coefficient, forward voltage	$I_F = 1.6\text{ mA}$	$\Delta V_F / \Delta T_{amb}$	-	-1.8	-	mV/ $^{\circ}\text{C}$
OUTPUT						
Logic low output voltage ⁽¹⁾	$I_F = 1.6\text{ mA}$, $I_O = 4.8\text{ mA}$, $V_{CC} = 4.5\text{ V}$	V_{OL}	-	0.1	0.4	V
	$I_F = 1.6\text{ mA}$, $I_O = 8\text{ mA}$, $V_{CC} = 4.5\text{ V}$	V_{OL}	-	0.1	0.4	V
	$I_F = 5\text{ mA}$, $I_O = 15\text{ mA}$, $V_{CC} = 4.5\text{ V}$	V_{OL}	-	0.15	0.4	V
	$I_F = 12\text{ mA}$, $I_O = 24\text{ mA}$, $V_{CC} = 4.5\text{ V}$	V_{OL}	-	0.25	0.4	V
Logic high output current ⁽¹⁾	$I_F = 0\text{ mA}$, $V_O = V_{CC} = 7\text{ V}$	I_{IO}	-	0.1	250	μA
	$I_F = 0\text{ mA}$, $V_O = V_{CC} = 18\text{ V}$	I_{IO}	-	0.05	100	μA
Logic low supply current ⁽¹⁾	$I_F = 1.6\text{ mA}$, $V_O = \text{OPEN}$, $V_{CC} = 18\text{ V}$	I_{CCL}	-	0.2	1.5	mA
Logic high supply current ⁽¹⁾	$I_F = 0\text{ mA}$, $V_O = \text{OPEN}$, $V_{CC} = 18\text{ V}$	I_{CCH}	-	0.01	10	μA
COUPLER						
Capacitance (input to output) ⁽²⁾	$f = 1\text{ MHz}$	C_{IO}	-	0.6	-	pF
Input capacitance	$f = 1\text{ MHz}$, $V_F = 0$	C_{IN}	-	25	-	pF

Notes

- Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.
 $T_{amb} = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$. Typical values are specified at $T_{amb} = 25\text{ }^{\circ}\text{C}$.
- ⁽¹⁾ Pin 7 open.
- ⁽²⁾ Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.

CURRENT TRANSFER RATIO							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Current transfer ratio ⁽¹⁾	$I_F = 1.6 \text{ mA}, V_O = 0.4 \text{ V}, V_{CC} = 4.5 \text{ V}$	SFH6318	CTR	300	1600	2600	%
	$I_F = 0.5 \text{ mA}, V_O = 0.4 \text{ V}, V_{CC} = 4.5 \text{ V}$	SFH6319	CTR	400	2000	3500	%
	$I_F = 1.6 \text{ mA}, V_O = 0.4 \text{ V}, V_{CC} = 4.5 \text{ V}$	SFH6319	CTR	500	1600	2600	%

Notes

- $T_{amb} = 0 \text{ }^\circ\text{C}$ to $70 \text{ }^\circ\text{C}$. Typical values are specified at $T_{amb} = 25 \text{ }^\circ\text{C}$.
DC current transfer ratio is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F times 100 %. Pin 7 open.
- (1) Pin 7 open

SWITCHING CHARACTERISTICS ($T_{amb} = 25 \text{ }^\circ\text{C}$, unless otherwise specified)							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Propagation delay time to logic low at output	$I_F = 1.6 \text{ mA}, R_L = 2.2 \text{ k}\Omega$	SFH6318	t_{PHL}	-	2	10	μs
Propagation delay time to logic low at output ⁽¹⁾	$I_F = 0.5 \text{ mA}, R_L = 4.7 \text{ k}\Omega$	SFH6319	t_{PHL}	-	6	25	μs
Propagation delay time to logic low at output ⁽¹⁾	$I_F = 12 \text{ mA}, R_L = 270 \Omega$	SFH6319	t_{PHL}	-	0.6	1	μs
Propagation delay time to logic high at output	$I_F = 1.6 \text{ mA}, R_L = 2.2 \text{ k}\Omega$	SFH6318	t_{PLH}	-	2	35	μs
Propagation delay time to logic high at output ⁽¹⁾	$I_F = 0.5 \text{ mA}, R_L = 4.7 \text{ k}\Omega$	SFH6319	t_{PLH}	-	4	60	μs
Propagation delay time to logic high at output ⁽¹⁾	$I_F = 12 \text{ mA}, R_L = 270 \Omega$	SFH6319	t_{PLH}	-	1.5	7	μs

Note

- (1) Pin 7 open. Using a resistor between pin 5 and 7 will decrease gain and delay time.

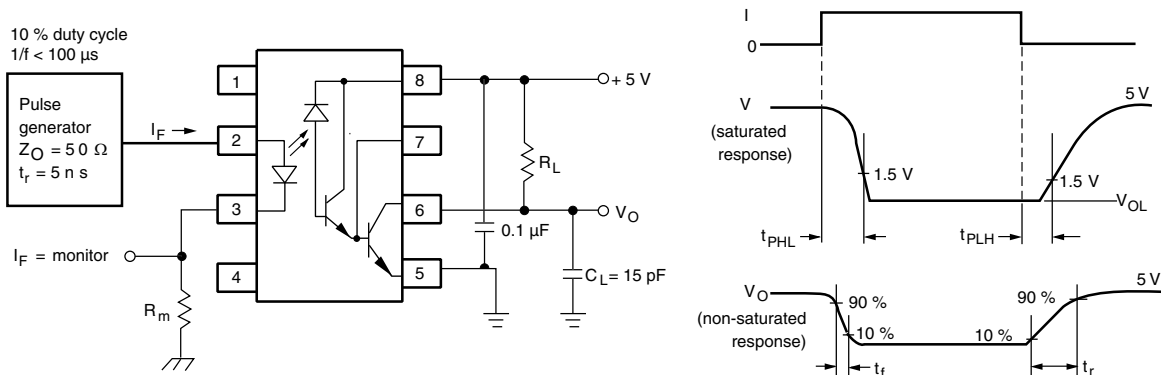


Fig. 1 - Switching Test Circuit

COMMON MODE TRANSIENT IMMUNITY							
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Common mode transient immunity at logic high level output ⁽¹⁾⁽²⁾	$I_F = 0 \text{ mA}, R_L = 2.2 \text{ k}\Omega, V_{CM} = 10 \text{ V}_{P-P}$	$ CM_H $	-	1000	-	$\text{V}/\mu\text{s}$	
Common mode transient immunity at logic low level output ⁽¹⁾⁽²⁾	$I_F = 1.6 \text{ mA}, R_L = 2.2 \text{ k}\Omega, V_{CM} = 10 \text{ V}_{P-P}$	$ CM_L $	-	1000	-	$\text{V}/\mu\text{s}$	

Notes

- (1) Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{CM} , to assure that the output will remain in a logic high state (i.e. $V_O > 2 \text{ V}$) common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e. $V_O < 0.8 \text{ V}$).
- (2) In applications where dv/dt may exceed $50\,000 \text{ V}/\mu\text{s}$ (such as state discharge) a series resistor, R_{CC} should be included to protect I_C from destructively high surge currents. The recommended value is refer to figure 2.
 $R_{CC} \cong [(V)/0.15 I_F (\text{mA})] \text{ k}\Omega$.

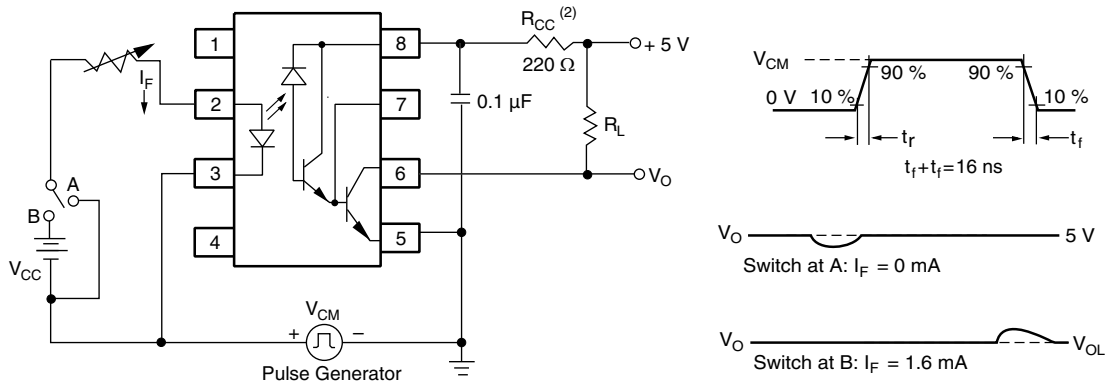


Fig. 2 - Test Circuit for Transient Immunity and Typical Waveforms

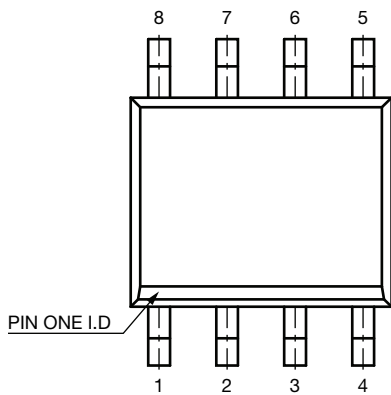
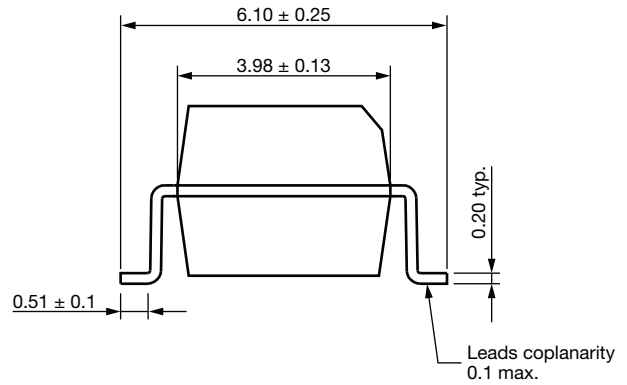
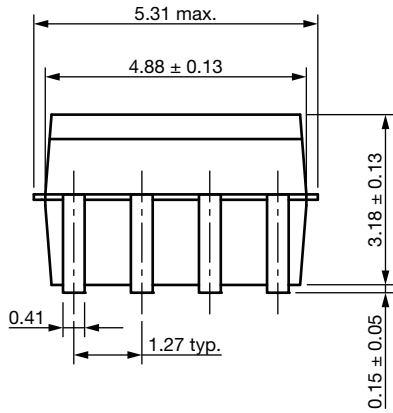
SAFETY AND INSULATION RATINGS				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Climatic classification	According to IEC 68 part 1		55/100/21	
Pollution degree	According to DIN VDE 0109		2	
Comparative tracking index	Insulation group IIIa	CTI	175	
Maximum rated withstanding isolation voltage	According to UL1577, t = 1 min	V _{ISO}	3333	V _{RMS}
Tested withstanding isolation voltage	According to UL1577, t = 1 s	V _{ISO}	4000	V _{RMS}
Maximum transient isolation voltage	According to DIN EN 60747-5-5	V _{IOTM}	6000	V _{peak}
Maximum repetitive peak isolation voltage	According to DIN EN 60747-5-5	V _{IORM}	560	V _{peak}
Isolation resistance	V _{IO} = 500 V, T _{amb} = 25 °C	R _{IO}	≥ 10 ¹²	Ω
	V _{IO} = 500 V, T _{amb} = 100 °C	R _{IO}	≥ 10 ¹¹	Ω
	V _{IO} = 500 V, T _{amb} = T _S	R _{IO}	≥ 10 ⁹	Ω
Output safety power		P _{SO}	350	mW
Input safety current		I _{SI}	150	mA
Safety temperature		T _S	165	°C
Creepage distance			≥ 4	mm
Clearance distance			≥ 4	mm
Input to output test voltage, method B	V _{IORM} × 1.875 = V _{PR} , 100 % production test with t _M = 1 s, partial discharge < 5 pC	V _{PR}	1050	V _{peak}
Input to output test voltage, method A	V _{IORM} × 1.6 = V _{PR} , 100 % sample test with t _M = 10 s, partial discharge < 5 pC	V _{PR}	896	V _{peak}

Note

- As per IEC 60747-5-5, § 7.4.3.8.2, this optocoupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of protective circuits.



PACKAGE DIMENSIONS (in millimeters)



Technical drawings according to DIN specifications

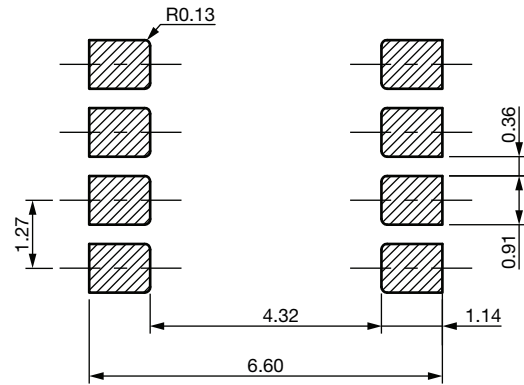


Fig. 3 - Package Drawing

PACKAGE MARKING

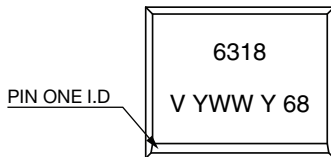


Fig. 4 - SFH6318

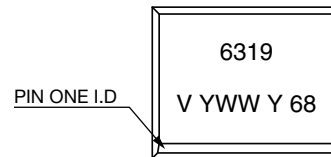


Fig. 5 - SFH6319

Note

- Tape and reel suffix (T) is not part of the package marking.

PACKING INFORMATION

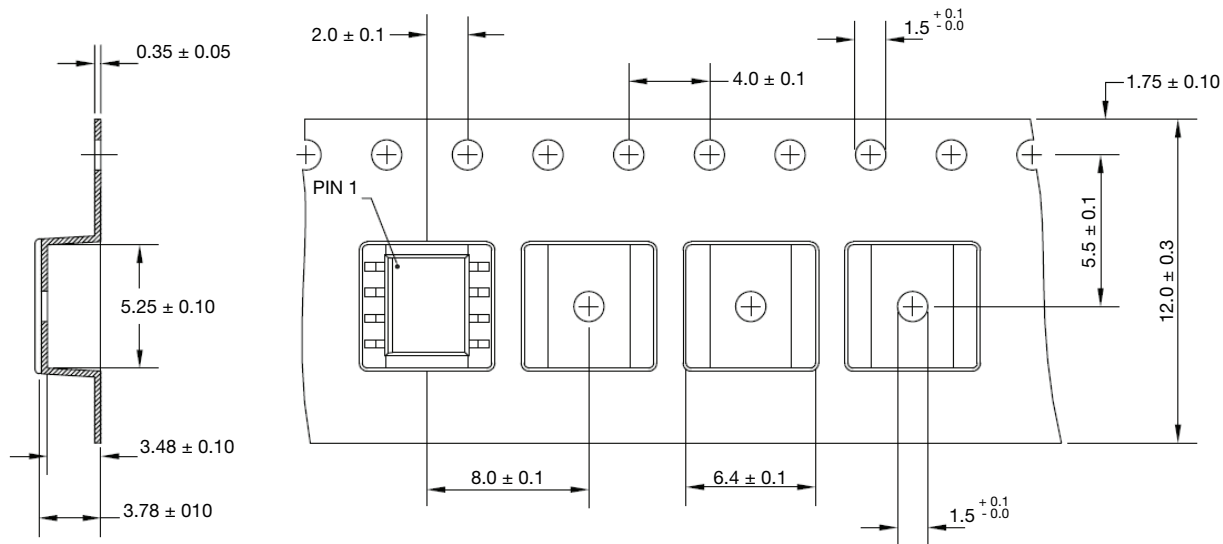


Fig. 6 - Tape and Reel Packing (2000 pieces on reel)

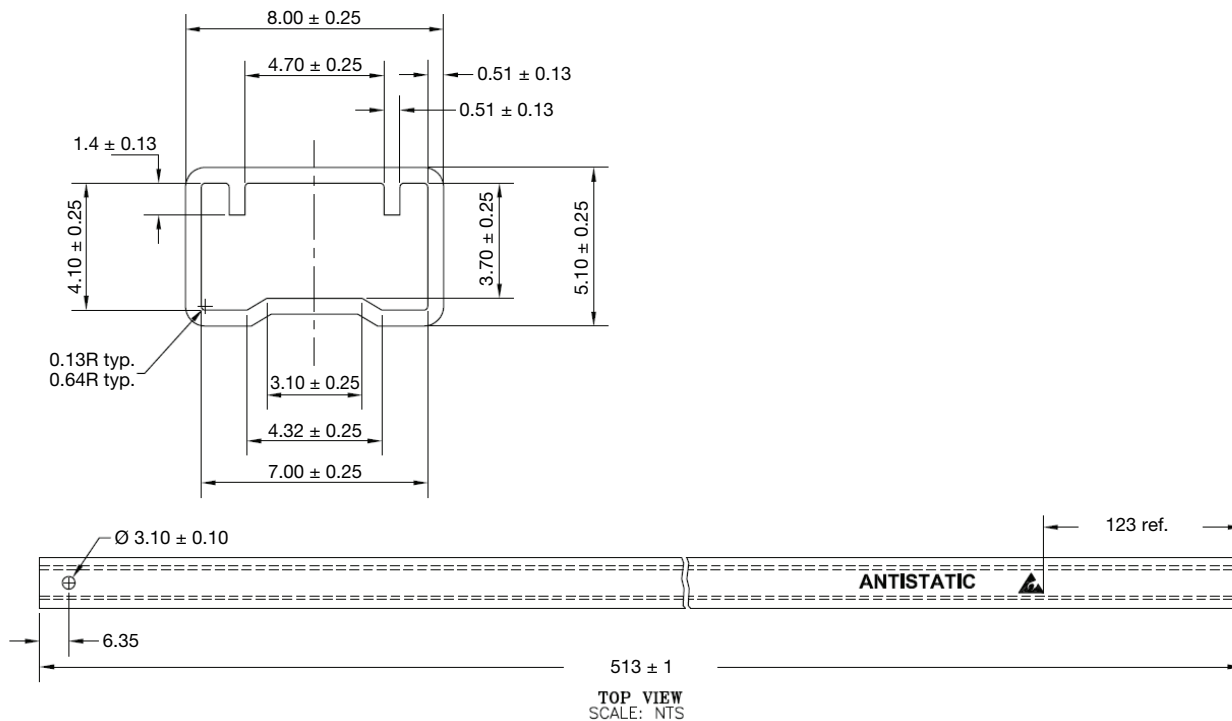
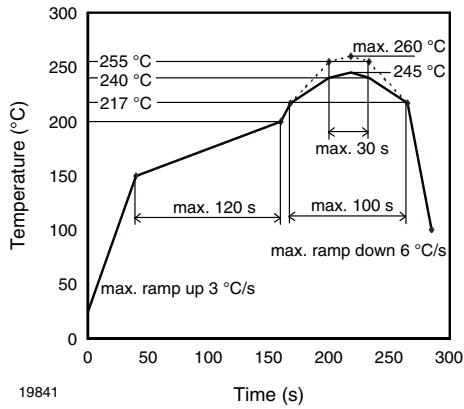


Fig. 7 - Tube Packing

DEVICE PER TUBE			
TYPE	UNITS/TUBE	TUBES/BOX	UNITS/BOX
SOIC-8	100	30	3000

SOLDER PROFILE



19841

Fig. 8 - Lead (Pb)-free Reflow Solder Profile according to J-STD-020

HANDLING AND STORAGE CONDITIONS

ESD level: HBM class 2

Floor life: unlimited

Conditions: $T_{amb} < 30\text{ °C}$, RH < 85 %

Moisture sensitivity level 1, according to J-STD-020



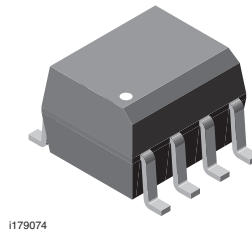
Footprint and Schematic Information for SFH6318, SFH6319

The footprint and schematic symbols for the following parts can be accessed using the associated links. They are available in Eagle, Altium, KiCad, OrCAD / Allegro, Pulsonix, and PADS.

Note that the 3D models for these parts can be found on the Vishay product page.

PART NUMBER	FOOTPRINT / SCHEMATIC
SFH6318	www.snapeda.com/parts/SFH6318/Vishay/view-part
SFH6318T	www.snapeda.com/parts/SFH6318T/Vishay/view-part
SFH6319	www.snapeda.com/parts/SFH6319/Vishay/view-part
SFH6319T	www.snapeda.com/parts/SFH6319T/Vishay/view-part

For technical issues and product support, please contact optocoupleranswers@vishay.com.





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