Document Title

64M-BIT (x1 / x2 / x4) 3.3V CMOS MXSMIO (SERIAL MULTI I/O) FLASH MEMORY

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	June 2, 2012	Preliminary
0.1	Add 16-pin SOP (300mil) package type	June 28, 2012	
0.2	Add 8-pin SOP (209mil) package type	July 10, 2012	
0.3	Add FAST READ DUAL OUTPUT (3Bh) command	November 1, 2012	
0.4	Refine QE bit definition to control only hardware protect function	November 19, 2012	
0.5	Change Figure-36-1, 36-2 and refine erase cycling	January 14, 2013	
1.0	Final version release	March 5, 2013	Final
1.1	SFDP address 08h ID code 37 changed to 00 SFDP address 38h & 4Ah EB dummy code data bits 04~00 changed from 00110b to 00100b	May 9, 2013	
1.2	Add A25LQ64M-FE type in ordering information This type fixes QE bit “1” The hardware protect function is disabled in this type Add 8-pin DIP package type	July 01, 2013	
1.3	Modify the fast program time spec.	January 9, 2014	
1.4	Change Figure 7. unique ID to 64 bytes	July 3, 2014	
1.5	Minor error corrections on Page 8, 15, 23, 26, 33, 34, 42, 43 & 44	July 23, 2015	

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FEATURES

GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 64Mb: 67,108,864 x 1 bit structure or 33,554,432 x 2 bits (two I/O mode) structure or 16,777,216 x 4 bits (four I/O mode) structure
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to V_{CC} +1V
- Low V_{CC} write inhibit is from 2.2V to 2.4V

PERFORMANCE

- High Performance
  - Fast read for SPI mode
    - 1 I/O: 104MHz with 8 dummy cycles
    - 2 I/O: 84MHz with 4 dummy cycles, equivalent to 168MHz
    - 4 I/O: 104MHz with 2+4 dummy cycles, equivalent to 416MHz
  - Fast read for QPI mode
    - 4 I/O: 84MHz with 2+2 dummy cycles, equivalent to 336MHz
    - 4 I/O: 104MHz with 2+4 dummy cycles, equivalent to 416MHz
  - Fast program time: 0.3ms (typ.) and 0.8ms (max./10K)/ 2ms (max./100K) /page (256-byte per page)
  - Byte program time: 6μs (typical)
  - 8/16/32/64 byte Wrap-Around Burst Read Mode
  - Fast erase time: 40ms (typ.)/sector (4K-byte per sector); 80ms (typ.)/block (32K-byte per block), 120ms (typ.) / block (64K-byte per block); 12s(typ.) /chip
- Low Power Consumption
  - Low active read current: 25mA (max.) at 104MHz, 20mA (max.) at 84MHz
  - Low active erase/programming current: 20mA (typ.)
  - Standby current: 2μA (typ.)
- Deep Power Down: 2μA(typ.)
- Typical 100,000 erase/program cycles
- 10 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
    The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
  - Additional 4k-bit secured OTP
  - 1K bit SFDP serial flash definition parameter
  - 64 bytes unique ID for each device
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector or block
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programmed should have page in the erased state first)
- Status Register Feature
- Command Reset
- Program/Erase Suspend
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- When using A25LQ64M-FE, the Hardware Protected Mode (HPM) is disabled

HARDWARE FEATURES

- Serial Clock (C)
  - Serial clock input
- DI (IO_0)
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- DO (IO_1)
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- $\overline{W}$ (IO_2)
  - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- IO_3
  - Serial input & Output for 4 x I/O read mode
- PACKAGE
  - 8-pin DIP (300mil), 8-pin SOP (209mil), 16-pin SOP (300mil), 8-pin WSON (6*5mm) or 24-ball BGA (6*8mm)
  - All Pb-free (Lead-free) products are RoHS2.0 compliant

GENERAL DESCRIPTION

A25LQ64 is 67,108,864 bits serial Flash memory, which is configured as 8,388,608 x 8 internally. When it is in two or four I/O mode, the structure becomes 33,554,432 bits x 2 or 16,777,216 bits x 4. A25LQ64 feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a Serial Clock (C), a serial data input (DI), and a serial data output (DO). Serial access to the device is enabled by $\overline{S}$ input.

When it is in two I/O read mode, the DI pin and DO pin become IO_0 pin and IO_1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the DI pin, DO pin and $\overline{W}$ pin become IO_0 pin, IO_1 pin, IO_2 pin and IO_3 pin for address/dummy bits input and data output.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for erase command is executed on sector (4K-byte), block (32K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and $\overline{S}$ is high, it is put in standby mode and draws less than 10μA DC current.

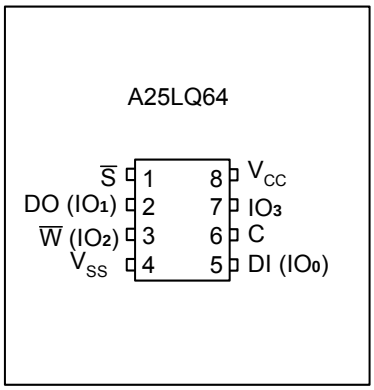
Table 1. Additional Feature Comparison

Additional Features / Part Name	Protection and Security		Read Performance					
			SPI				QPI	
	Flexible Block Protection (BP0-BP3)	4K-bit security OTP	1 I/O (104 MHz)	2 I/O (84 MHz)	4 I/O (84 MHz)	4 I/O (104 MHz)	4 I/O (84 MHz)	4 I/O (104 MHz)
A25LQ64	V	V	V	V	V	V	V	V

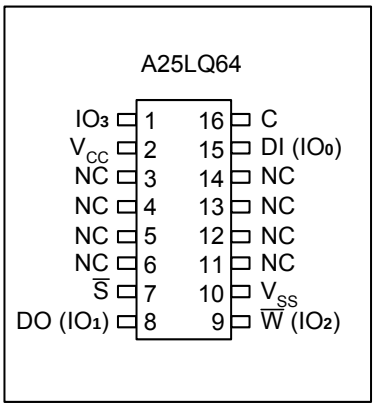
Additional Features / Part Name	Identifier			
	RES (command: AB hex)	REMS (command: 90 hex)	RDID (command: 9F hex)	QRIID (Command: AF hex)
A25LQ64	16 (hex)	37 16 (hex) (if ADD=0)	37 40 17	37 40 17

Pin Configuration

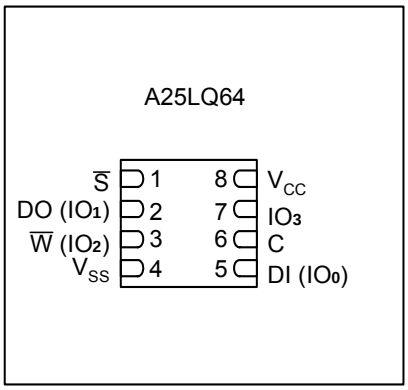
■ 8-pin DIP / SOP



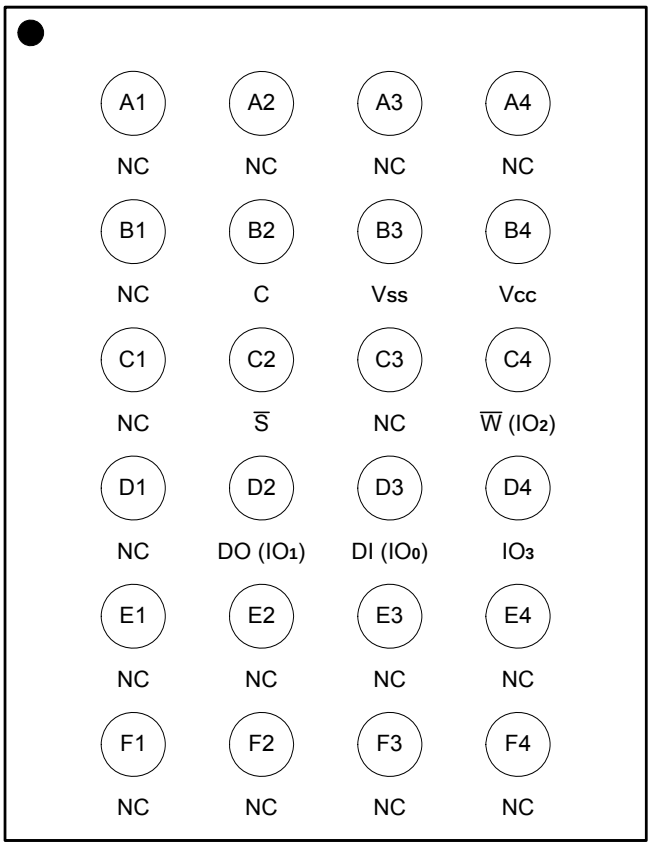
■ 16-pin SOP



■ 8-pin WSON



■ 24-ball BGA

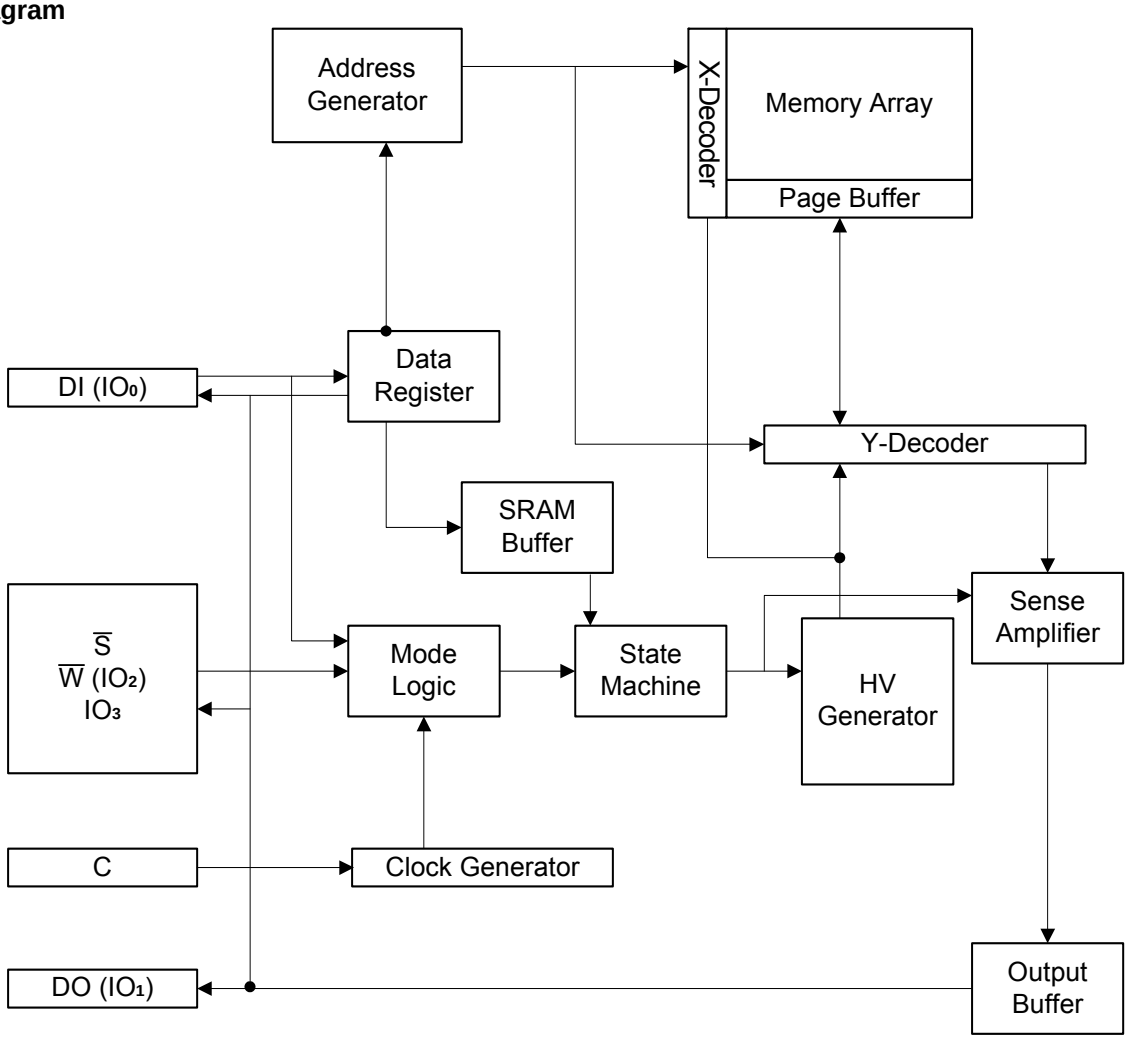


Top View, Balls Facing Down

Pin Descriptions

Pin Name	Description
$\overline{S}$	Chip Select
DI (IO_0)	Serial Data Input (for 1 x I/O) / Serial Data Input & Output (for 2 x I/O or 4 x I/O read mode)
DO (IO_1)	Serial Data Output (for 1 x I/O) / Serial Data Input & Output (for 2 x I/O or 4 x I/O read mode)
C	Serial Clock
$\overline{W}$ (IO_2)	Write protection: connect to V_{SS} or Serial Data Input & Output (for 4 x I/O read mode)
IO_3	Serial Data Input & Output (for 4 x I/O read mode)
Vcc	+ 3.3V Power Supply
V_{SS}	Ground
NC	No Connect

Block Diagram



DATA PROTECTION

The A25LQ64 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transition or system noise.

- Power-on reset and t_{PUW}: to avoid sudden power switch by system power supply transition, the power-on reset and t_{PUW} (internal timer) may protect the Flash.
- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP) command completion
  - Sector Erase (SE) command completion
  - Block Erase 32KB (BE32K) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion
  - Program/Erase Suspend
  - Softreset command completion
  - Write Security Register (WRSCUR) command completion
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES) and softreset command.
- Block lock protection and additional 4K-bit secured OTP: there are block protection and 4K secured OTP which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of "Protected Area Sizes", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
  Please refer to table of "protected area sizes".
- The Hardware Protected Mode (HPM) use $\overline{W}$ (IO_2) to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit. When using A25LQ64M-FE, the Hardware Protected Mode (HPM) is disabled.
- In four I/O and QPI mode, the feature of HPM will be disabled

Table 2. Protected Area Sizes

Status Bit				Protect Area
BP3	BP2	BP1	BP0	64Mb
0	0	0	0	0 (none)
0	0	0	1	1 (2 blocks, block 126th~127th)
0	0	1	0	2 (4 blocks, block 124th~127th)
0	0	1	1	3 (8 blocks, block 120th~127th)
0	1	0	0	4 (16 blocks, block 112th~127th)
0	1	0	1	5 (32 blocks, block 96th~127th)
0	1	1	0	6 (64 blocks, block 64th~127th)
0	1	1	1	7 (128 blocks, all)
1	0	0	0	8 (128 blocks, all)
1	0	0	1	9 (128 blocks, all)
1	0	1	0	10 (128 blocks, all)
1	0	1	1	11 (128 blocks, all)
1	1	0	0	12 (128 blocks, all)
1	1	0	1	13 (128 blocks, all)
1	1	1	0	14 (128 blocks, all)
1	1	1	1	15 (128 blocks, all)

II. Additional 4K-bit secured OTP: to provide 4K-bit one-time program area - Which may be locked by customer through WRSCUR command. The address range and size please refer to Table 3. 4K-bit secured OTP definition.

- Security register bit 1 (LDSO) indicates whether the 4K-bit secured OTP is locked or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with Enter Security OTP command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing Exit Security OTP command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR (write security register) command to set bit 1 (LDSO) as "1". Please refer to Table 8. Security register definition for security register bit definition.
- Note: Once lock-down by LDSO bit, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

Sector Size	Address Range
4096 bit	xxx000 – xxx1FF

Memory Organization

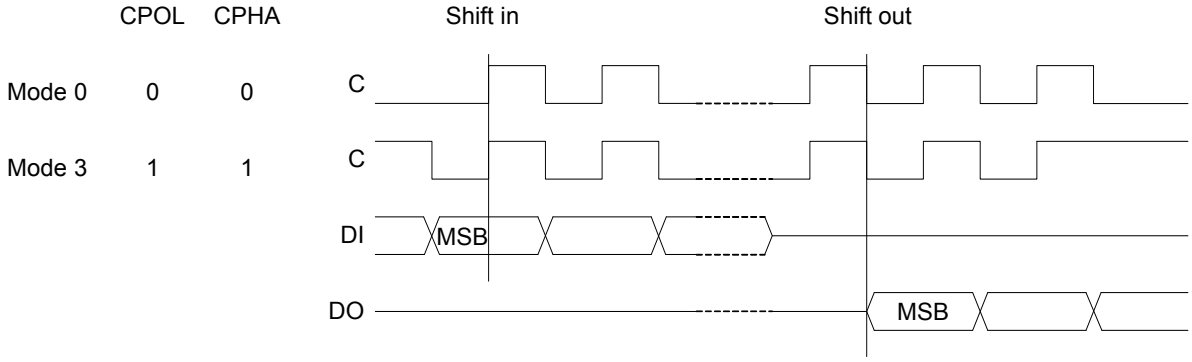
Table 4. Memory Organization (64Mb)

Block (64K-byte)	Block (32K-byte)	Sector (4K-byte)	Address Range	
127	255	2047	7FF000h	7FFFFFh
		⋮		
		2040	7F8000h	7F8FFFh
	254	2039	7F7000h	7F7FFFh
		⋮		
		2032	7F0000h	7F0FFFh
126	253	2031	7EF000h	7EFFFFh
		⋮		
		2024	7E8000h	7E8FFFh
	252	2023	7E7000h	7E7FFFh
		⋮		
		2016	7E0000h	7E0FFFh
125	251	2015	7DF000h	7DFFFFh
		⋮		
		2008	7D8000h	7D8FFFh
	250	2007	7D7000h	7D7FFFh
		⋮		
		2000	7D0000h	7D0FFFh
⋮	⋮	⋮	⋮	⋮
2	5	47	02F000h	02FFFFh
		⋮		
		40	028000h	028FFFh
	4	39	027000h	027FFFh
		⋮		
		32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
		⋮		
		24	018000h	018FFFh
	2	23	017000h	017FFFh
		⋮		
		16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
		⋮		
		8	008000h	008FFFh
	0	7	007000h	007FFFh
		⋮		
		0	000000h	000FFFh

DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next $\overline{S}$ falling edge. In standby mode, DO pin of this LSI should be High-Z.
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next $\overline{S}$ rising edge.
4. Input data is latched on the rising edge of Serial Clock (C) and data shifts out on the falling edge of Serial Clock (C). The difference of Serial mode 0 and mode 3 is shown as Figure 1. "Serial Modes Supported".
5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST READ, 2READ, 4READ, RES, REMS, QPIID, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the $\overline{S}$ can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the $\overline{S}$ must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for Serial Clock (C) high while idle, CPOL=0 for Serial Clock (C) low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

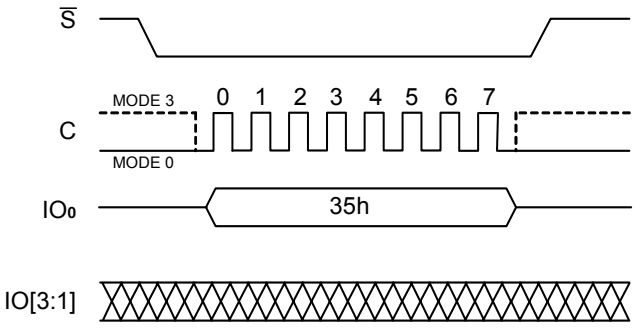
Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode (EQIO)

By issuing 35H command, the QPI mode is enable.

Figure 2. Enable QPI Sequence (Command 35H)

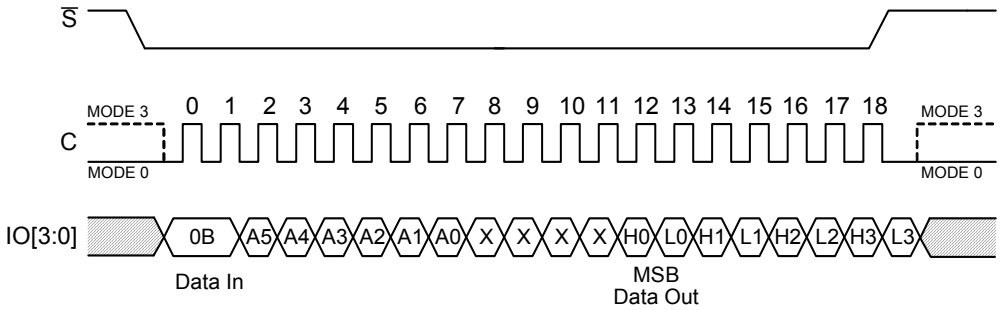


Quad Peripheral Interface (QPI) operation

To use QPI protocol, the host drives $\overline{S}$ low then sends the Fast Read command, 0BH, followed by 6 address cycles and four dummy cycles. Most significant bit (MSB) comes first, as shown in figure 3.

After the dummy cycle, the Quad Peripheral Interface (QPI) Flash Memory outputs data on the falling edge of the Serial Clock (C) signal starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on $\overline{S}$. The internal address pointer automatically increases until the highest memory address is reached. When reached the highest memory address, the address pointer returns to the beginning of the address space.

Figure 3. High-Speed Read Sequence (QPI) (Command 0BH)

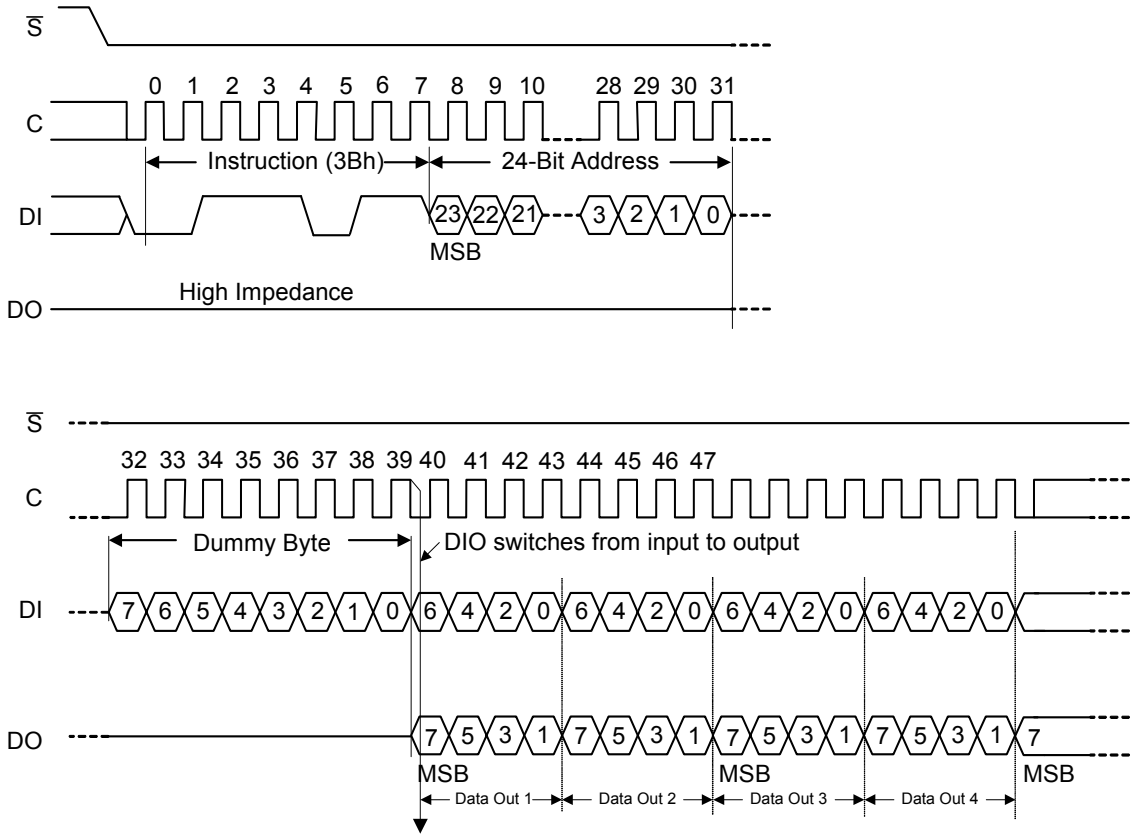


Read Data Bytes at Higher Speed by Dual Output (FAST READ DUAL OUTPUT)

The FAST READ DUAL OUTPUT (3Bh) instruction is similar to the FAST READ (0Bh) instruction except the data is output on two pins, IO_0 and IO_1, instead of just DO. This allows data to be transferred from the A25LQ64 at twice the rate of standard SPI devices.

Similar to the FAST READ instruction, the FAST READ DUAL OUTPUT instruction can operate at the highest possible frequency of f_C (See AC Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in figure 4. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO_0 and IO_1 pins should be high-impedance prior to the falling edge of the first data out clock.

Figure 4. FAST READ DUAL OUTPUT Instruction Sequence and Data-Out Sequence

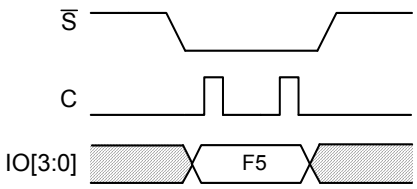


Note: Address bit A23 is Don't Care, for A25LQ64

Reset QPI mode (RSTQIO)

By issuing F5H command, the device is reset to 1-I/O SPI mode.

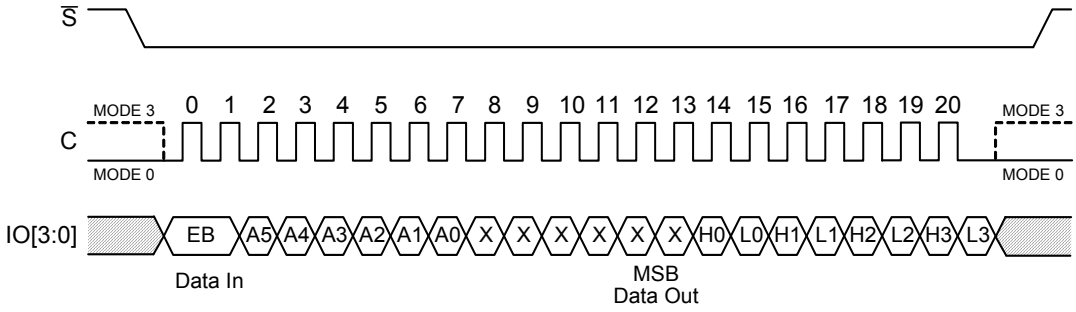
Figure 5. Reset QPI Mode (Command F5H)



Fast QPI Read mode (FASTRDQ)

To increase the code transmission speed, the device provides a "Fast QPI Read Mode" (FASTRDQ). By issuing command code EBH, the FASTRDQ mode is enable. The number of dummy cycle increase from 4 to 6 cycles. The read cycle frequency will increase from 84MHz to 104MHz.

Figure 6. Fast QPI Read Mode (FASTRDQ) (Command EBH)



COMMAND DESCRIPTION

Table 5. Command Set

Read Commands

I/O	1	1	1	1	2	2
Read Mode	SPI	SPI	SPI	SPI	SPI	SPI
Command (byte)	READ (normal read)	FAST READ * (fast read data)	SFDP	UNIQUE ID	2READ (2 x I/O read command) Note1	FAST READ DAUL OUTPUT * (fast read data)
Clock rate (MHz)	66	104	104	104	84	104
1st byte	03 (hex)	0B (hex)	5A (hex)	4B (hex)	BB (hex)	3B (hex)
2nd byte	AD1(8)	AD1(8)	AD1 (8)	Dummy (8)	AD1(4)	AD1(8)
3rd byte	AD2(8)	AD2(8)	AD2 (8)	Dummy (8)	AD2(4)	AD2(8)
4th byte	AD3(8)	AD3(8)	AD3 (8)	Dummy (8)	AD3(4)	AD3(8)
5th byte		Dummy(8)	Dummy(8)	Dummy (8)	Dummy(4)	Dummy(8)
Action	n bytes read out until $\overline{S}$ goes high	n bytes read out until $\overline{S}$ goes high	n bytes read out until $\overline{S}$ goes high	n bytes read out until $\overline{S}$ goes high	n bytes read out by 2 x I/O until $\overline{S}$ goes high	n bytes read out by 2 x I/O until $\overline{S}$ goes high

4	4	4	4
SPI	SPI	QPI	QPI
W4READ	4READ * (4 x I/O read command) Note1	FAST READ * (fast read data)	4READ * (4 x I/O read command) Note1
84	104	84	104
E7 (hex)	EB (hex)	0B (hex)	EB (hex)
AD1(2)	AD1(2)	AD1(2)	AD1(2)
AD2(2)	AD2(2)	AD2(2)	AD2(2)
AD3(2)	AD3(2)	AD3(2)	AD3(2)
Dummy(4)	Dummy(6)	Dummy(4)	Dummy(6)
Quad I/O read with 4 dummy cycles in 84MHz	Quad I/O read with 6 dummy cycles in 104MHz	Quad I/O read with 4 dummy cycles in 104MHz	Quad I/O read with 6 dummy cycles in 104MHz

Program/Erase Commands

Command (byte)	WREN* (write enable)	WRDI * (write disable)	RDSR * (read status register)	WRSR * (write status register)	4PP (quad page program)	SE * (sector erase)	BE 32K * (block erase 32KB)
1st byte	06 (hex)	04 (hex)	05 (hex)	01 (hex)	38 (hex)	20 (hex)	52 (hex)
2nd byte				Values	AD1	AD1	AD1
3rd byte					AD2	AD2	AD2
4th byte					AD3	AD3	AD3
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to write new values of the status register	quad input to program the selected page	to erase the selected sector	to erase the selected 32K block

Command (byte)	BE * (block erase 64KB)	CE * (chip erase)	PP * (page program)	DP * (Deep power down)	RDP * (Release from deep power down)	PGM/ERS Suspend * (Suspends Program/ Erase)	PGM/ERS Resume * (Resumes Program/ Erase)
1st byte	D8 (hex)	60 or C7 (hex)	02 (hex)	B9 (hex)	AB (hex)	B0 (hex)	30 (hex)
2nd byte	AD1		AD1				
3rd byte	AD2		AD2				
4th byte	AD3		AD3				
Action	to erase the selected block	to erase whole chip	to program the selected page	enters deep power down mode	release from deep power down mode		

Security/ID/Mode Setting/Reset Commands

Command (byte)	RDID (read identification)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	ENSO * (enter secured OTP)	EXSO * (exit secured OTP)	RDSCUR * (read security register)	WRSCUR * (write security register)
1st byte	9F (hex)	AB (hex)	90 (hex)	B1 (hex)	C1 (hex)	2B (hex)	2F (hex)
2nd byte		x	x				
3rd byte		x	x				
4th byte		x	ADD (Note 2)				
5th byte							
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	to enter the 4K-bit secured OTP mode	to exit the 4K-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock- down, cannot be update)

Command (byte)	NOP * (No Operation)	RSTEN * (Reset Enable)	RST * (Reset Memory)	EQIO (Enable Quad I/O)	RSTQIO (Reset Quad I/O)	QPIID (QPI ID Read)	SBL * (Set Burst Length)
1st byte	00 (hex)	66 (hex)	99 (hex)	35 (hex)	F5 (hex)	AF (hex)	C0 (hex)
2nd byte							Value
3rd byte							
4th byte							
Action				Entering the QPI mode	Exiting the QPI mode	ID in QPI interface	to set Burst length

Note 1: Command set highlighted with (*) are supported both in SPI and QPI mode.
Note 2: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on DI (IO_0) which is different from 1 x I/O condition.
Note 3: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.
Note 4: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.
Note 5: RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.

Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: $\overline{S}$ goes low→sending WREN instruction code→ $\overline{S}$ goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The DO[3:1] are don't care in SPI mode. (Please refer to Figure 15-1 and Figure 15-2)

Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: $\overline{S}$ goes low→sending WRDI instruction code→ $\overline{S}$ goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The DO[3:1] are don't care in SPI mode. (Please refer to Figure 16-1 and Figure 16-2)

The WEL bit is reset by following situations:

- Power-up
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Quad Page Program (4PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction
- Pgm/Ers Suspend

Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Manufacturer ID and Device ID are listed as Table 7. ID Definitions.

The sequence of issuing RDID instruction is: $\overline{S}$ goes low→ sending RDID instruction code→24-bits ID data out on DO→ to end RDID operation can drive $\overline{S}$ to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of Program/Erase operation which is currently in progress. When $\overline{S}$ goes high, the device is at standby stage.

Read Status Register (RDSR)

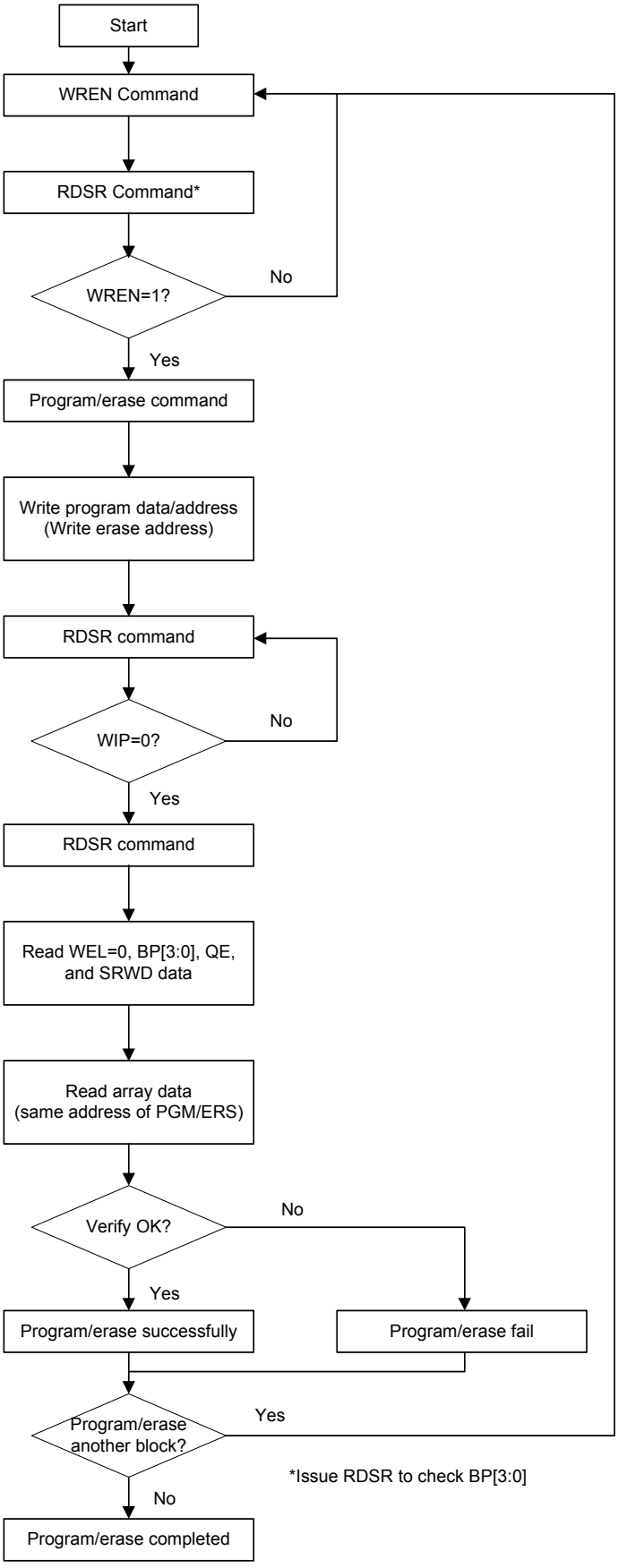
The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: $\overline{S}$ goes low→ sending RDSR instruction code→ Status Register data out on DO.

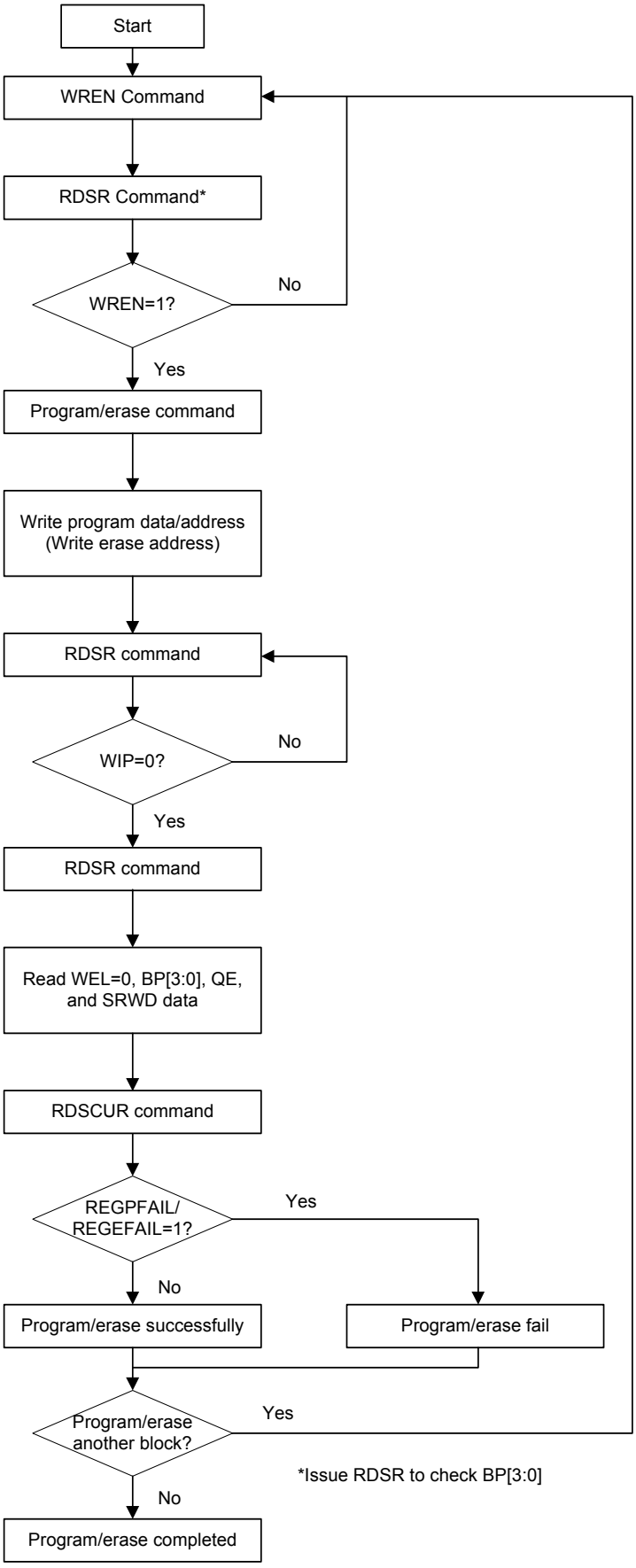
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The DO[3:1] are don't care when during SPI mode. (Please refer to Figure 18-1 and Figure 18-2)

For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

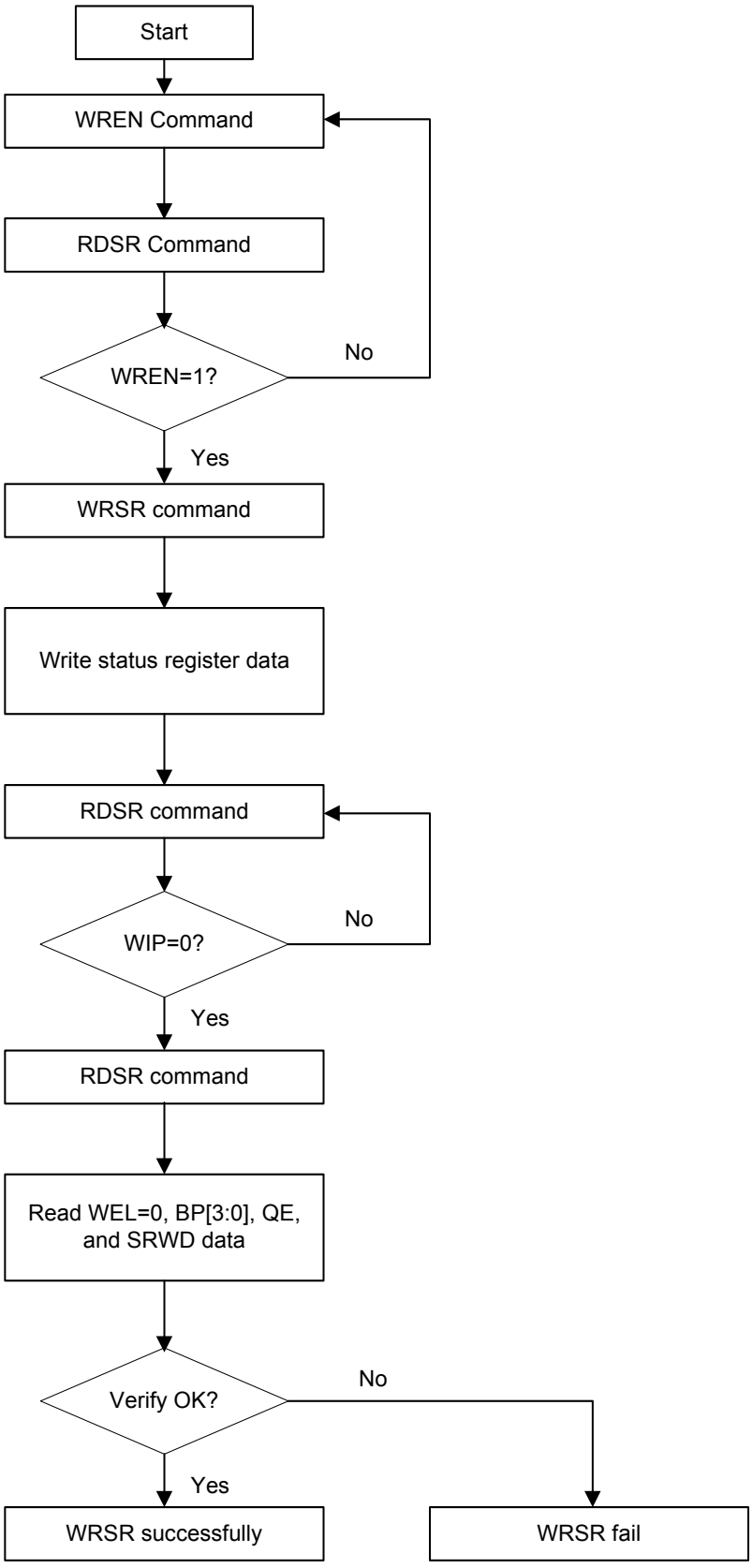
Program/ Erase flow with read array data



Program/ Erase flow without read array data (read REGPFAIL/REGEFAIL flag)



WRSR flow


Start
WREN Command
RDSR Command
WREN=1?
No
Yes
WRSR command
Write status register data
RDSR command
WIP=0?
No
Yes
RDSR command
Read WEL=0, BP[3:0], QE, and SRWD data
Verify OK?
No
Yes
WRSR successfully
WRSR fail

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/ erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/ erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in table 2) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is unprotected.

QE bit. The Quad Enhance (QE) bit, non-volatile bit, enhances SPI Quad modes. It controls only hardware protect function in SPI mode. It is reset to "0" (factory default) to enable hardware protect function or is set to "1" to disable hardware protect function. The SPI Quad I/O commands will be always accepted by flash no matter QE bit is “1” or “0”. The QE bit has to be set the through WRSR command Status Register bit 6. In SPI mode and QE bit is “0”. ($\overline{W}$) pin should not keep floating in case incidentally hardware protected when SRWD bit is “1”. A25LQ64M-FE fixes QE bit “1”.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection ($\overline{W}$) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and $\overline{W}$ pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Status Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SRWD (status register write protect)	QE (Quad Enhance) (note 2)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1=Quad Enhance 0=not Quad Enhance	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: See the Table 2. Protected Area Size.

Note 2: A25LQ64M-FE fixes QE bit “1”.

Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in Table 2). The WRSR also can set or reset the Quad Enhance (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection ($\overline{W}$) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: $\overline{S}$ goes low→ sending WRSR instruction code→ Status Register data on DI→$\overline{S}$ goes high. (Please refer to Figure 19-1 and Figure 19-2)

The $\overline{S}$ must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tw) is initiated as soon as Chip Select ($\overline{S}$) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tw timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset. A25LQ64M-FE fixes QE bit "1", when using this type, the Hardware Protected Mode (HPM) is disabled.

Table 6. Protection Modes

Mode	Status register condition	$\overline{W}$ and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	$\overline{W}$ =1 and SRWD bit=0, or $\overline{W}$ =0 and SRWD bit=0, or $\overline{W}$ =1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	$\overline{W}$ =0, SRWD bit=1	The protected area cannot be program or erase.

Note:
1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in Table 2.
2. When using A25LQ64M-FE, the Hardware Protected Mode (HPM) is disabled.

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):

- When SRWD bit=0, no matter $\overline{W}$ is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and $\overline{W}$ is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).

Note:

If SRWD bit=1 but $\overline{W}$ is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed. When using A25LQ64M-FE, the Hardware Protected Mode (HPM) is disabled.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then $\overline{W}$ is low (or $\overline{W}$ is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the $\overline{W}$ to against data modification. When using A25LQ64M-FE, the Hardware Protected Mode (HPM) is disabled.

Note:

To exit the hardware protected mode requires $\overline{W}$ driving high once the hardware protected mode is entered. If the $\overline{W}$ pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.
If the system enter QPI or set QE=1, the feature of HPM will be disabled.

Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of Serial Clock (C), and data shifts out on the falling edge of Serial Clock (C) at a maximum frequency f_R. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.
The sequence of issuing READ instruction is: $\overline{S}$ goes low→sending READ instruction code→ 3-byte address on DI→ data out on DO→to end READ operation can use $\overline{S}$ to high at any time during data out. (Please refer to Figure 20)

Read Data Bytes at Higher Speed (FAST READ)

The FAST READ instruction is for quickly reading data out. The address is latched on rising edge of Serial Clock (C), and data of each bit shifts out on the falling edge of Serial Clock (C) at a maximum frequency f_C. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST READ instruction. The address counter rolls over to 0 when the highest address has been reached.

Read on SPI Mode The sequence of issuing FAST READ instruction is: $\overline{S}$ goes low→ sending FAST READ instruction code→ 3-byte address on DI→1-dummy byte (default) address on DI→ data out on DO→ to end FAST READ operation can use $\overline{S}$ to high at any time during data out. (Please refer to Figure 21-1)

Read on QPI Mode The sequence of issuing FAST READ instruction in QPI mode is: $\overline{S}$ goes low→ sending FAST READ instruction, 2 cycles→ 24-bit address interleave on IO_3, IO_2, IO_1 & IO_0→ 4 dummy cycles→data out interleave on IO_3, IO_2, IO_1 & IO_0→ to end QPI FAST READ operation can use $\overline{S}$ to high at any time during data out. (Please refer to Figure 21-2)
In the performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h,5Ah,F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h and afterwards $\overline{S}$ is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.
While Program/Erase/Write Status Register cycle is in progress, FAST READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

2 x I/O Read Mode (2READ)

The 2READ instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of Serial Clock (C), and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of Serial Clock (C) at a maximum frequency f_T. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.
The sequence of issuing 2READ instruction is: $\overline{S}$ goes low→ sending 2READ instruction→ 24-bit address interleave on IO_1 & IO_0→ 4 dummy cycles on IO_1 & IO_0→ data out interleave on IO_1 & IO_0→ to end 2READ operation can use $\overline{S}$ to high at any time during data out (Please refer to Figure 22. for 2 x I/O Read Mode Timing Waveform).
While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial Flash in read mode. The address is latched on rising edge of Serial Clock (C), and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of Serial Clock (C) at a maximum frequency f_Q. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

4 x I/O Read on SPI Mode (4READ) The sequence of issuing 4READ instruction is: $\overline{S}$ goes low→ sending 4READ instruction→ 24-bit address interleave on IO_3, IO_2, IO_1 & IO_0 → 2+4 dummy cycles→data out interleave on IO_3, IO_2, IO_1 & IO_0 → to end 4READ operation can use $\overline{S}$ to high at any time during data out.
W4READ instruction (E7) is also available is SPI mode for 4 I/O read. The sequence is similar to 4READ, but with only 4 dummy cycles. The clock rate runs at 84MHz.

4 x I/O Read on QPI Mode (4READ) The 4READ instruction also support on QPI command mode. The sequence of issuing 4READ instruction QPI mode is: $\overline{S}$ goes low→ sending 4READ instruction→ 24-bit address interleave IO_3, IO_2, IO_1 & IO_0 →2+4 dummy cycles→data out interleave on IO_3, IO_2, IO_1 & IO_0→ to end 4READ operation can use $\overline{S}$ to high at any time during data out (Please refer to Figure 23. for 4 x I/O Read Mode Timing Waveform).
Another sequence of issuing 4 READ instruction especially useful in random access is : $\overline{S}$ goes low→sending 4 READ instruction→3-bytes address interleave on IO_3, IO_2, IO_1 & IO_0 →performance enhance toggling bit P[7:0]→ 4 dummy cycles →data out still $\overline{S}$ goes high →$\overline{S}$ goes low (reduce 4 Read instruction) →24-bit random access address (Please refer to Figure 24-1 and Figure 24-2 for 4 x I/O Read Enhance Performance Mode Timing Waveform).
In the performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make

this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh, 00h, AAh or 55h and afterwards $\overline{S}$ is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.
While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Burst Read

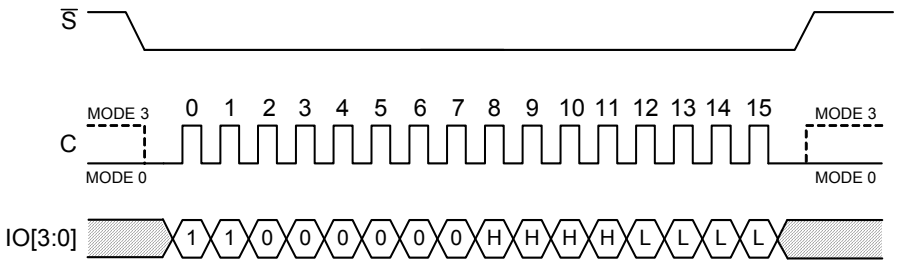
This device supports Burst Read in both SPI and QPI mode.
To set the Burst length, following command operation is required..
Issuing command: "C0h" in the first Byte (8-clocks), following 4 clocks defining wrap around enable with "0h" and disable with"1h".

Next 4 clocks is to define wrap around depth. Definition as following table:

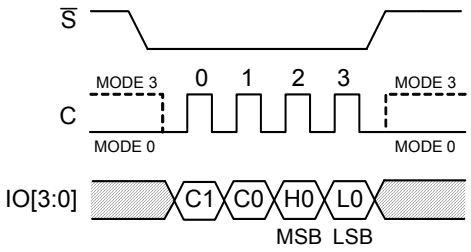
Data	Wrap Around	Wrap Depth	Data	Wrap Around	Wrap Depth
1xh	No	X	00h	Yes	8-byte
1xh	No	X	01h	Yes	16-byte
1xh	No	X	02h	Yes	32-byte
1xh	No	X	03h	Yes	64-byte

The wrap around unit is defined within the 256Byte page, with random initial address. It's defined as "wrap-around mode disable" for the default state of the device. To exit wrap around, it is required to issue another "C0" command in which data='1xh". Otherwise, wrap around status will be retained until power down or reset command. To change wrap around depth, it is required to issue another "C0" command in which data="0xh". QPI "0Bh" "EBh" and SPI "EBh" "E7h" support wrap around feature after wrap around enable. Burst read is supported in both SPI and QPI mode. The device id default without Burst read.

SPI Mode



QPI Mode



Note:
MSB = Most Significant Bit
LSB = Least Significant Bit

Performance Enhance Mode

The device could waive the command cycle bits if the two cycle bits after address cycle toggles. (Please note Figure 24-1 and Figure 24-2. 4 x I/O Read enhance performance mode sequence).
Performance enhance mode is supported in both SPI and QPI mode.
In QPI mode, “EBh” “0Bh” and SPI “EBh” “E7h” commands support enhance mode. The performance enhance mode is not supported in dual I/O mode.
After entering enhance mode, following $\overline{S}$ go high, the device will stay in the read mode and treat $\overline{S}$ go low of the first clock as address instead of command cycle.
To exit enhance mode, a new fast read command whose first two dummy cycles is not toggle then exit. Or issue ”FFh” command to exit enhance mode.

Performance Enhance Mode Reset (FFh)

To conduct the Performance Enhance Mode Reset operation in SPI mode, FFh command code, 8 clocks, should be issued in 1I/O sequence. In QPI Mode, FFFFFFFFh command code, 8 clocks, in 4I/O should be issued. (Please refer to Figure 38)
If the system controller is being Reset during operation, the flash device will return to the standard SPI operation.
Upon Reset of main chip, SPI instruction would be issued from the system. Instructions like Read ID (9Fh) or Fast Read (0Bh) would be issued.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode. (Please refer to Figure 38)

Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see table of memory organization) is a valid address for Sector Erase (SE) instruction. The $\overline{S}$ must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.
Address bits (A22-A12) select the sector address.
The sequence of issuing SE instruction is: $\overline{S}$ goes low→ sending SE instruction code→ 3-byte address on DI→ $\overline{S}$ goes high.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode. (Please refer to Figure 27-1 and Figure 27-2)
The self-timed Sector Erase Cycle time (t_{SE}) is initiated as soon as Chip Select ($\overline{S}$) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the t_{SE} timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector.

Block Erase (BE32K)

The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (see table of memory organization) is a valid address for Block Erase (BE32K) instruction. The $\overline{S}$ must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.
The sequence of issuing BE32K instruction is: $\overline{S}$ goes low→ sending BE32K instruction code→ 3-byte address on DI→ $\overline{S}$ goes high.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode. (Please refer to Figure 28-1 and Figure 28-2)
The self-timed Block Erase Cycle time ($t_{BE}32K$) is initiated as soon as Chip Select ($\overline{S}$) goes high. The Write in Progress (WIP) bit still can be check out during the Block Erase cycle is in progress. The WIP sets 1 during the $t_{BE}32K$ timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase ($t_{BE}32K$) instruction will not be executed on the block.

Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to table of memory organization) is a valid address for Block Erase (BE) instruction. The $\overline{S}$ must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.
The sequence of issuing BE instruction is: $\overline{S}$ goes low→ sending BE instruction code→ 3-byte address on DI→ $\overline{S}$ goes high.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode. (Please refer to Figure 29-1 and Figure 29-2)
The self-timed Block Erase Cycle time (t_{SE}) is initiated as soon as Chip Select ($\overline{S}$) goes high. The Write in Progress (WIP) bit still can be check out during the Block Erase cycle is in progress. The WIP sets 1 during the t_{SE} timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the block.

Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The $\overline{S}$ must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.
The sequence of issuing CE instruction is: $\overline{S}$ goes low→sending CE instruction code→ $\overline{S}$ goes high.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can

accept by this instruction. The IO[3:1] are don't care when during SPI mode. (Please refer to Figure 30-1 and Figure 30-2)
The self-timed Chip Erase Cycle time (t_{CE}) is initiated as soon as Chip Select ($\overline{S}$) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the t_{CE} timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP3, BP2, BP1, BP0 all set to "0".

Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (The eight least significant address bits) should be set to 0. If the eight least significant address bits (A7-A0) are not all 0, all transmitted data going beyond the end of the current page are programmed from the start address of the same page (from the address A7-A0 are all 0). If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the requested address of the page without effect on other address of the same page.
The sequence of issuing PP instruction is: $\overline{S}$ goes low→ sending PP instruction code→ 3-byte address on DI→ at least 1-byte on data on DI→$\overline{S}$ goes high. (Please refer to Figure 25-1 and Figure 25-2)
The $\overline{S}$ must be kept to low during the whole Page Program cycle; The $\overline{S}$ must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.
The self-timed Page Program Cycle time (t_{PP}) is initiated as soon as Chip Select ($\overline{S}$) goes high. The Write in Progress (WIP) bit still can be check out during the Page Program cycle is in progress. The WIP sets 1 during the t_{PP} timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode.

4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: IO_0, IO_1, IO_2, and IO_3 as address and data input, which can improve programmer performance and the effectiveness of application of lower clock less than 33MHz. For system with faster clock, the Quad page program cannot provide more actual favors, because the required internal page program time is far more than the time data flows in. Therefore, we suggest that while executing this command (especially during sending data), user can slow the clock speed down to 33MHz below. The other function descriptions are as same as standard page program.
The sequence of issuing 4PP instruction is: $\overline{S}$ goes low→ sending 4PP instruction code→ 3-byte address on IO[3:0]→ at least 1-byte on data on IO[3:0]→$\overline{S}$ goes high.

Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When $\overline{S}$ goes high, it's only in deep power-down mode not standby mode. It's different from Standby mode.
The sequence of issuing DP instruction is: $\overline{S}$ goes low→sending DP instruction code→$\overline{S}$ goes high.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode. (Please refer to Figure 31-1 and Figure 31-2)
Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction and softreset command. (those instructions allow the ID being reading out). When Power-down, or software reset command the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For DP instruction the $\overline{S}$ must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select ($\overline{S}$) goes high, a delay of t_{DP} is required before entering the Deep Power-down mode.

Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select ($\overline{S}$) High. When Chip Select ($\overline{S}$) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select ($\overline{S}$) must remain High for at least tRES2(max), as specified in Table 12. AC Characteristics. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode.
RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions on next page. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.
The sequence is shown as Figure 32, Figure 33-1 and Figure 33-2. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.
Only SPI (8 clocks) command cycle can accept by this instruction.

The RES instruction is ended by $\overline{S}$ goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on Serial Clock (C) while $\overline{S}$ is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of t_{RES2} to transit to standby mode, and $\overline{S}$ must remain to high at least t_{RES2}(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.
The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the $\overline{S}$ pin low and shift the instruction code "90h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID (37h) and the Device ID are shifted out on the falling edge of Serial Clock (C) with most significant bit (MSB) first as shown in Figure 34 The Device ID values are listed in Table 7 of ID Definitions. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving $\overline{S}$ high.

QPI ID Read (QPIID)

The QPIID is Quad mode RDID A25LQ64. The sequence of issue QPIID instruction is $\overline{S}$ goes low→sending QPI ID instruction→Data out on DO→$\overline{S}$ goes high. Most significant bit (MSB) first.
Immediately following the command cycle the device outputs data on the falling edge of the Serial Clock (C) signal. The data output stream is continuous until terminated by a low to high transition of $\overline{S}$. The device outputs three bytes of data: manufacturer, device type, and device ID.

Table 7. ID Definitions

Command Type	A25LQ64		
RDID (JEDEC ID)	Manufacturer ID	Memory Type	Memory Density
	37	40	17
RES	Electronic ID		
	17		
REMS	Manufacturer ID	Device ID	
	37	16	

Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 4K-bit secured OTP mode. The additional 4K-bit secured OTP is independent from main array, which may use to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.
The sequence of issuing ENSO instruction is: $\overline{S}$ goes low→ sending ENSO instruction to enter Secured OTP mode→$\overline{S}$ goes high.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode.

Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 4K-bit secured OTP mode.
The sequence of issuing EXSO instruction is: $\overline{S}$ goes low→ sending EXSO instruction to exit Secured OTP mode→$\overline{S}$ goes high.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode.

Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.
The sequence of issuing RDSCUR instruction is : $\overline{S}$ goes low→sending RDSCUR instruction→Security Register data out on DO→$\overline{S}$ goes high.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode.
The definition of the Security Register bits is as below:
Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be update any more. While it is in 4K-bit secured OTP mode, main array access is not allowed.

Write Security Register (WRSCUR)

The WRSCUR instruction is for setting the values of Security Register Bits. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more. The LDSO bit is an OTP bit. Once the LDSO bit is set, the value of LDSO bit can not be altered any more.
The sequence of issuing WRSCUR instruction is : $\overline{S}$ goes low→ sending WRSCUR instruction→ Status Register data on DI→ $\overline{S}$ goes high.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode.
The $\overline{S}$ must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

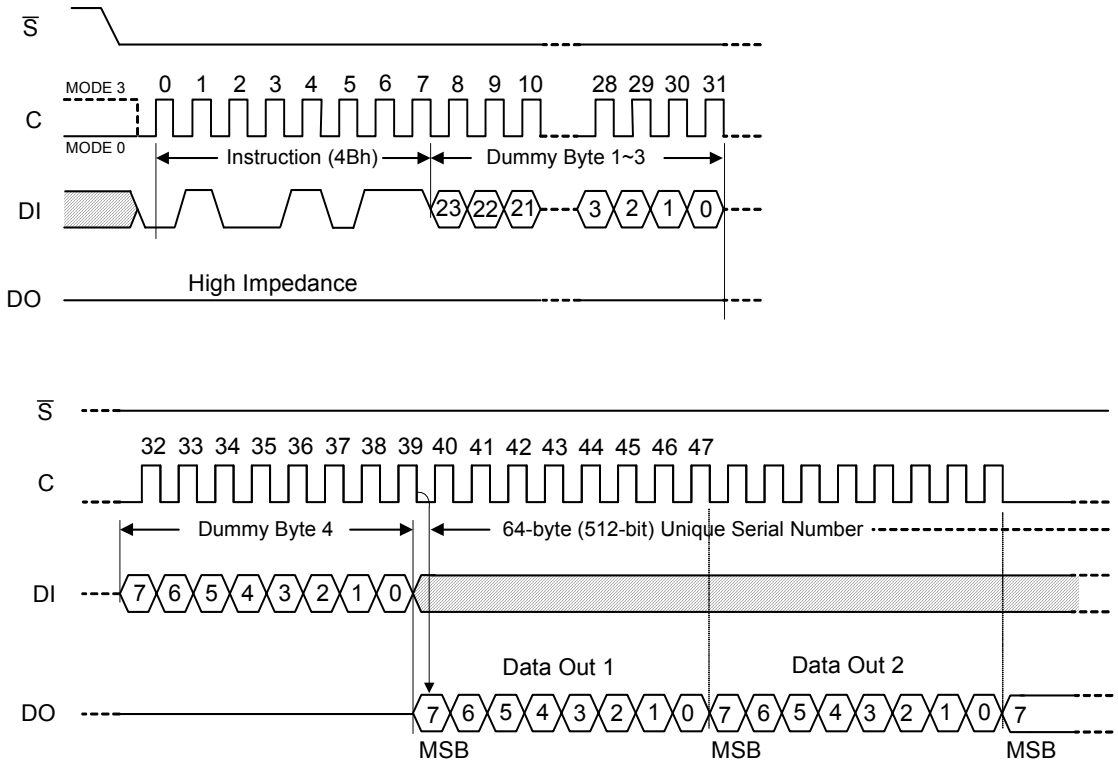
Table 8. Security Register Definition

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	E_FAIL	P_FAIL	Reserved	Erase Suspend bit	Program Suspend bit	LDSO (indicate if lock-down)	Reserved
0	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	-	0=Erase is not suspended 1= Erase suspended (default=0)	0=Program is not suspended 1= Program suspended (default=0)	0 = not lock-down 1 = lock-down (cannot program/ erase OTP)	0
Read Only	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Non-volatile bit (OTP)	Read Only

Read Unique ID Number (4Bh)(1)

The Read Unique ID Number instruction accesses a factory-set read-only 64-byte number that is unique to each A25LQ64 device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the $\overline{S}$ pin low and shifting the instruction code "4Bh" followed by a four bytes of dummy clocks. After which, the 64-byte ID is shifted out on the falling edge of Serial Clock (C) as shown in figure 7.

Figure 7. Read Unique ID Number Instruction Sequence



Note:

For A25LQ64 this feature is available upon special request. Please contact AMIC for details.

Read SFDP Mode (5Ah)

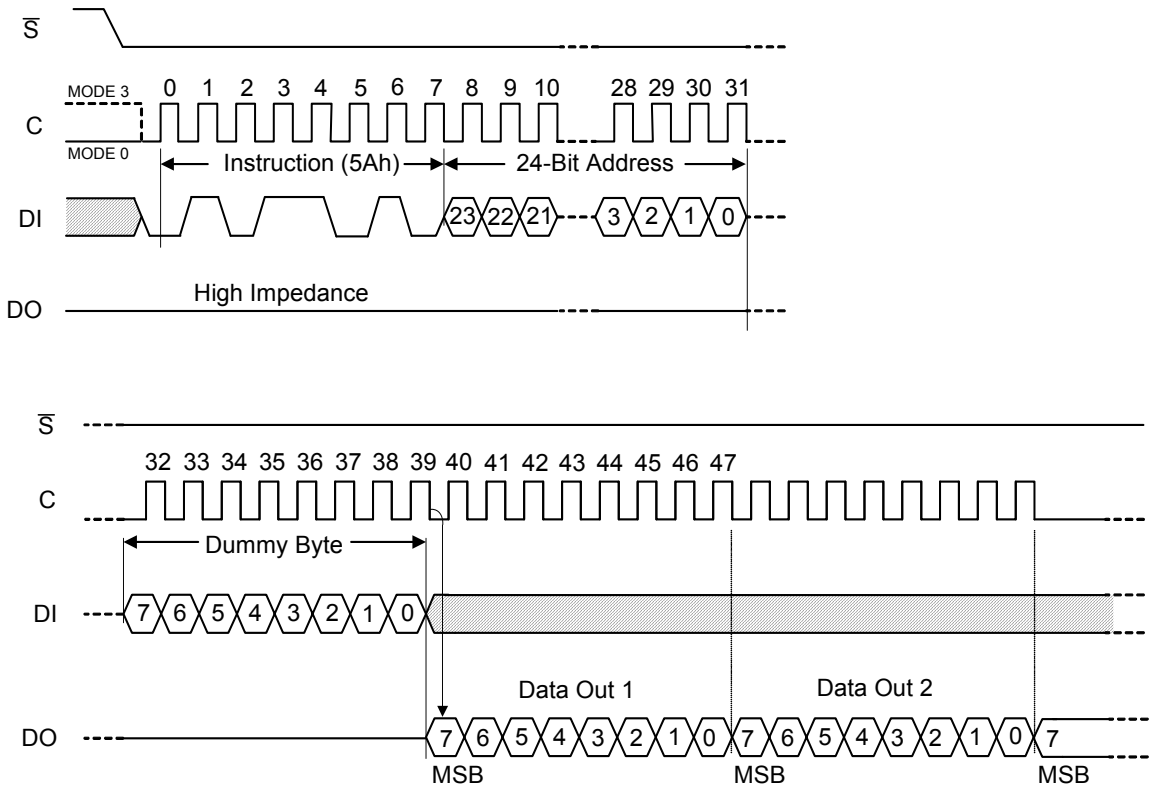
Read SFDP Mode

A25LQ64 features Serial Flash Discoverable Parameters (SFDP) mode. Host system can retrieve the operating characteristics, structure and vendor specified information such as identifying information, memory size, operating voltage and timing information of this device by SFDP mode.

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read SFDP Mode is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on DO, each bit being shifted out, at a maximum frequency FR, during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 8. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Serial Flash Discoverable Parameters (SFDP) instruction. When the highest address is reached, the address counter rolls over to 0x00h, allowing the read sequence to be continued indefinitely. The Serial Flash Discoverable Parameters (SFDP) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read Data Bytes at Serial Flash Discoverable Parameters (SFDP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 8. Read SFDP Mode Instruction Sequence Diagram



Note: Please note the above address cycles are base on 3-byte address mode.

Table 9. Serial Flash Discoverable Parameters (SFDP) Signature and Parameter Identification Data Value (Advanced Information)

Description	Address (h) (Byte Mode)	Data (Bit)	Data	Comment
SFDP Signature	00h	07 : 00	53h	Signature [31:0]: Hex: 50444653
	01h	15 : 08	46h	
	02h	23 : 16	44h	
	03h	31 : 24	50h	
SFDP Minor Revision Number	04h	07 : 00	00h	Star from 0x00
SFDP Major Revision Number	05h	15 : 08	01h	Star from 0x01
Number of Parameter Headers (NPH)	06h	23 : 16	00h	1 parameter header
Unused	07h	31 : 24	FFh	Reserved
ID Number	08h	07 : 00	00h	
Parameter Table Minor Revision Number	09h	15 : 08	00h	Star from 0x00
Parameter Table Major Revision Number	0Ah	23 : 16	01h	Star from 0x01
Parameter Table Length (in DW)	0Bh	31 : 24	09h	9 DWORDs
Parameter Table Pointer (PTP)	0Ch	07 : 00	30h	000030h
	0Dh	15 : 08	00h	
	0Eh	23 : 16	00h	
Unused	0Fh	31 : 24	FFh	Reserved

Table 10. Parameter ID (0) (Advanced Information)

Description	Address (h) (Byte Mode)	Data (Bit)	Data	Comment
Block / Sector Erase sizes Identifies the erase granularity for all Flash Components	30h	00	01b	00 = reserved 01 = 4KB erase 10 = reserved 11 = 64KB erase
		01		
Write Granularity		02	1b	0 = No, 1 = Yes
Write Enable Instruction Required for Writing to Volatile Status Register		03	00b	00 = N/A 01 = use 50h opcode 11 = use 06h opcode
Write Enable Opcode Select for Writing to Volatile Status Register		04		
Unused		05	111b	Reserved
		06		
		07		
4 Kilo-Byte Erase Opcode	31h	08	20h	4 KB Erase Support (FFh = not supported)
		09		
		10		
		11		
		12		
		13		
		14		
		15		
Supports (1-1-2) Fast Read Device supports single input opcode & address and dual output data Fast Read	32h	16	1b	0 = not supported 1 = supported
Address Byte Number of bytes used in addressing for flash array write and erase.		17	00b	00 = 3-Byte 01 = 3- or 4-Byte (e.g. defaults to 3-Byte mode; enters 4-Byte mode on command) 10 = 4-Byte 11 = reserved
		18		
Supports Double Transfer Rate (DTR) Clocking Indicates the device supports some type of double transfer rate clocking.		19	0b	0 = not supported 1 = supported
Supports (1-2-2) Fast Read Device supports single input opcode, dual input address, and dual output data Fast Read		20	1b	0 = not supported 1 = supported
Supports (1-4-4) Fast Read Device supports single input opcode, quad input address, and quad output data Fast Read		21	1b	0 = not supported 1 = supported
Supports (1-1-4) Fast Read Device supports single input opcode & address and quad output data Fast Read		22	0b	0 = not supported 1 = supported
Unused		23	1b	Reserved
Unused	33h	24	FFh	Reserved
		25		
		26		
		27		
		28		
		29		
		30		
		31		

Table 10. Parameter ID (0) (Advanced Information) (continued)

Description	Address (h) (Byte Mode)	Data (Bit)	Data	Comment
Flash Memory Density	37h : 34h	31 : 00	03FFFFFFh	64 Mbits

Table 10. Parameter ID (0) (Advanced Information) (continued)

Description	Address (h) (Byte Mode)	Data (Bit)	Data	Comment
(1-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output	38h	00 01 02 03 04	00100b	4 dummy clocks
Quad Input Address Quad Output (1-4-4) Fast Read Number of Mode Bits		05 06 07	010b	8 mode bits
(1-4-4) Fast Read Opcode Opcode for single input opcode, quad input address, and quad output data Fast Read.	39h	08 09 10 11 12 13 14 15	EBh	
(1-1-4) Fast Read Number of Wait states (dummy clocks) needed before valid output	3Ah	16 17 18 19 20	00000b	Not Supported
(1-1-4) Fast Read Number of Mode Bits		21 22 23	000b	Not Supported
(1-1-4) Fast Read Opcode Opcode for single input opcode & address and quad output data Fast Read.	3Bh	31 : 24	FFh	Not Supported

Table 10. Parameter ID (0) (Advanced Information) (continued)

Description	Address (h) (Byte Mode)	Data (Bit)	Data	Comment
(1-1-2) Fast Read Number of Wait states (dummy clocks) needed before valid output	3Ch	00 01 02 03 04	01000b	8 dummy clocks
(1-1-2) Fast Read Number of Mode Bits		05 06 07	000b	Not Supported
(1-1-2) Fast Read Opcode Opcode for single input opcode & address and dual output data Fast Read.	3Dh	15 : 08	3Bh	
(1-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output	3Eh	16 17 18 19 20	00100b	4 dummy clocks
(1-2-2) Fast Read Number of Mode Bits		21 22 23	000b	Not Supported
(1-2-2) Fast Read Opcode Opcode for single input opcode, dual input address, and dual output data Fast Read.	3Fh	31 : 24	BBh	

Table 10. Parameter ID (0) (Advanced Information) (continued)

Description	Address (h) (Byte Mode)	Data (Bit)	Data	Comment
Supports (4-4-4) Fast Read Device supports Quad input opcode & address and quad output data Fast Read.	40h	00	1b	0 = not supported 1 = supported
Reserved. These bits default to all 1's		01 02 03	111b	Reserved
Supports (2-2-2) Fast Read Device supports dual input opcode & address and dual output data Fast Read.		04	0b	0 = not supported 1 = supported
Reserved. These bits default to all 1's		05 06 07	111b	Reserved
Reserved. These bits default to all 1's	43h : 41h	31 : 08	FFh	Reserved

Table 10. Parameter ID (0) (Advanced Information) (continued)

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Reserved. These bits default to all 1's	45h : 44h	15 : 00	FFh	Reserved
(2-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output	46h	16 17 18 19 20	00000b	Not Supported
(2-2-2) Fast Read Number of Mode Bits		21 22 23	000b	Not Supported
(2-2-2) Fast Read Opcode Opcode for dual input opcode & address and dual output data Fast Read.	47h	31 : 24	FFh	Not Supported

Table 10. Parameter ID (0) (Advanced Information) (continued)

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Reserved. These bits default to all 1's	49h : 48h	15 : 00	FFh	Reserved
(4-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output	4Ah	16 17 18 19 20	00100b	4 dummy clocks
(4-4-4) Fast Read Number of Mode Bits		21 22 23	010b	8 mode bits
(4-4-4) Fast Read Opcode Opcode for quad input opcode/address, quad output data Fast Read.	4Bh	31 : 24	EBh	Must Enter QPI Mode Firstly

Table 10. Parameter ID (0) (Advanced Information) (continued)

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Sector Type 1 Size	4Ch	07 : 00	0Ch	4 KB
Sector Type 1 Opcode	4Dh	15 : 08	20h	
Sector Type 2 Size	4Eh	23 : 16	0Fh	32 KB
Sector Type 2 Opcode	4Fh	31 : 24	52h	

Table 10. Parameter ID (0) (Advanced Information) (continued)

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Sector Type 3 Size	50h	07 : 00	10h	64 KB
Sector Type 3 Opcode	51h	15 : 08	D8h	
Sector Type 4 Size	52h	23 : 16	00h	Not Supported
Sector Type 4 Opcode	53h	31 : 24	FFh	Not Supported

Program/Erase Suspend/Resume

The device allow the interruption of Sector-Erase, Block-Erase or Page-Program operations and conduct other operations. Details as follows.
To enter the suspend/resume mode: issuing B0h for suspend; 30h for resume (SPI/QPI all acceptable)
Read security register bit2 (PSB) and bit3 (ESB) (please refer to table 8 to check suspend ready information.
Suspend to suspend ready timing: 20μs.
Resume to another suspend timing: 1ms.
ESB bit (Erase Suspend Bit) indicates the status of Erase suspend operation. When issue a suspend command during erase operation ESB=1, when erase operation resumes, ESB will be reset to "0".
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode.

Erase Suspend

Erase suspend allow the interruption of all erase operations.
After erase suspend, WEL bit will be clear, only read related, resume and reset command can be accepted unconditionally. (including: 03h, 0Bh, 3Bh, BBh, EBh, E7h, 9Fh, AFh, 90h, 05h, 2Bh, B1h, C1h, 5Ah, 3Ch, 30h, 66h, 99h, C0h, 35h, F5h, 00h, ABh)
For erase suspend to program operation, the programming command (38, 02) can be accepted under conditions as follows:
The block group (BG) is divided into 32BGs in this device, each BG's density is 2Mb. While conducting erase suspend in one BG, the programming operation that follows can only be conducted in one of the other BGs and should not be conducted in the BG executing the suspend operation. The boundaries of the BGs are illustrated as below table.

BG (2M bit)	Address Range	BG (2M bit)	Address Range
31	7C0000h-7FFFFFh	15	3C0000h-3FFFFFh
30	780000h-7BFFFFh	14	380000h-3BFFFFh
29	740000h-77FFFFh	13	340000h-37FFFFh
28	700000h-73FFFFh	12	300000h-33FFFFh
27	6C0000h-6FFFFFh	11	2C0000h-2FFFFFh
26	680000h-6BFFFFh	10	280000h-2BFFFFh
25	640000h-67FFFFh	9	240000h-27FFFFh
24	600000h-63FFFFh	8	200000h-23FFFFh
23	5C0000h-5FFFFFh	7	1C0000h-1FFFFFh
22	580000h-5BFFFFh	6	180000h-1BFFFFh
21	540000h-57FFFFh	5	140000h-17FFFFh
20	500000h-53FFFFh	4	100000h-13FFFFh
19	4C0000h-4FFFFFh	3	0C0000h-0FFFFFh
18	480000h-4BFFFFh	2	080000h-0BFFFFh
17	440000h-47FFFFh	1	040000h-07FFFFh
16	400000h-43FFFFh	0	000000h-03FFFFh

After issue erase suspend command, latency time 20μs is needed before issue another command. For "Suspend to Read", "Resume to Read", "Resume to Suspend" timing specification please note Figure 41-1, Figure 41-2 and Figure 41-3.
ESB bit (Erase Suspend Bit) indicates the status of Erase suspend operation. When issue a suspend command during erase operation ESB=1, when erase operation resumes, ESB will be reset to "0".
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode.
When ESB bit is issued, the Write Enable Latch (WEL) bit will be reset.
See Figure 41-1 for Suspend to Read latency.

Program Suspend

Program suspend allows the interruption of all program operations.
After program suspend, WEL bit will be cleared, only read related, resume and reset command can be accepted. (including: 03h, 0Bh, 3Bh, BBh, EBh, E7h, 9Fh, AFh, 90h, 05h, 2Bh, B1h, C1h, 5Ah, 3Ch, 30h, 66h, 99h, C0h, 35h, F5h, 00h, ABh)
After issue program suspend command, latency time 20μs is needed before issue another command.
For "Suspend to Read", "Resume to Read", "Resume to Suspend" timing specification please note Figure 41-1, Figure 41-2 and Figure 41-3.
PSB bit (Program Suspend Bit) indicates the status of Program suspend operation. When issue a suspend command during program operation PSB=1, when program operation resumes, PSB will be reset to "0".
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode.

Write-Resume

The Write operation is being resumed when Write-Resume instruction issued. ESB or PSB (suspend status bit) in Status register will be changed back to “0”
The operation of Write-Resume is as follows: $\overline{S}$ drives low → send write resume command cycle (30H) → drive $\overline{S}$ high. By polling Busy Bit in status register, the internal write operation status could be checked to be completed or not. The user may also wait the time lag of TSE, TBE, TPP for Sector-erase, Block-erase or Page-programming. WREN (command "06" is not required to issue before resume. Resume to another suspend operation requires latency time of 1ms.
Please note that, if "performance enhance mode" is executed during suspend operation, the device can not be resume. To restart the write command, disable the "performance enhance mode" is required. After the "performance enhance mode" is disable, the write-resume command is effective.

No Operation (NOP)

The No Operation command only cancels a Reset Enable command. NOP has no impact on any other command.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode.

Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Reset operation is used as a system (software) reset that puts the device in normal operating Ready mode.
This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).
To reset the A25LQ64 the host drives $\overline{S}$ low, sends the Reset-Enable command (66H), and drives $\overline{S}$ high.
Next, the host drives $\overline{S}$ low again, sends the Reset command (99H), and drives $\overline{S}$ high.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode.
The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.
A successful command execution will reset the device to SPI stand-by read mode, which are their respective default states, see Figure 42. A device reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more latency time than recovery from other operations.

Reset Quad I/O (RSTQIO)

The Reset Quad I/O instruction, F5H, resets the device to 1-bit SPI protocol operation. To execute a Reset Quad I/O operation, the host drives $\overline{S}$ low, sends the Reset Quad I/O command cycle (F5h) then, drives $\overline{S}$ high.
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The IO[3:1] are don't care when during SPI mode.

Note:
For EQIO/RSTQIO $\overline{S}$ high width has to follow "write spec" t_{SHSL} as 30ns for next instruction.

POWER-ON STATE

The device is at below states when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the Vcc achieves below correct level:
- Vcc minimum at power-up stage and then after a delay of t_{VSL}
- V_{SS} at power-down

Please note that a pull-up resistor on $\overline{S}$ may ensure a safe and proper power-up/down level.
An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. During power on, when Vcc is lower than V_{WI} (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.
For further protection on the device, after Vcc reaching the V_{WI} level, a t_{PUW} time delay is required before the device is fully accessible for commands like write enable (WREN), page program (PP), quad page program (4PP), sector erase (SE), block erase 32KB (BE32K), block erase (BE), chip erase (CE), WRSCUR and write status register (WRSR). If the Vcc does not reach the Vcc minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:
- t_{PUW} after Vcc reached V_{WI} level
- t_{VSL} after Vcc reached Vcc minimum level

The device can accept read command after Vcc reached Vcc minimum and a time delay of t_{VSL}, even time of t_{PUW} has not passed.
Please refer to the figure of "power-up timing".

Note:
- To stabilize the Vcc level, the Vcc rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1μF)
- At power-down stage, the Vcc drops below V_{WI} level, all operations are disable and device has no response to any write command. The data corruption might occur during the stage while a write, program, erase cycle is in progress.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Rating		Value
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to Vcc +4.6V
Applied Output Voltage		-0.5V to Vcc +4.6V
Vcc to Ground Potential		-0.5V to Vcc +4.6V

Notes:
1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to Vss to -2.0V and Vcc to +2.0V for period up to 20ns.

Figure 9. Maximum Negative Input Overshoot

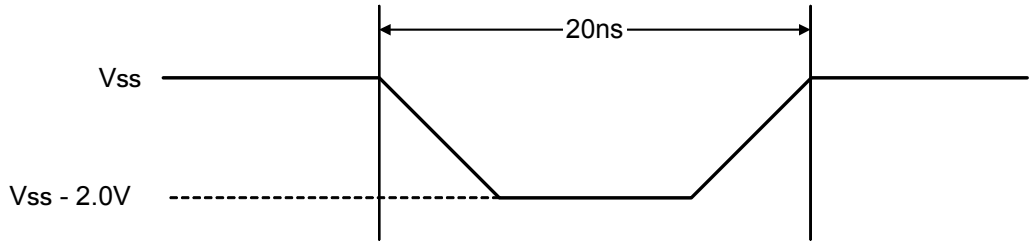
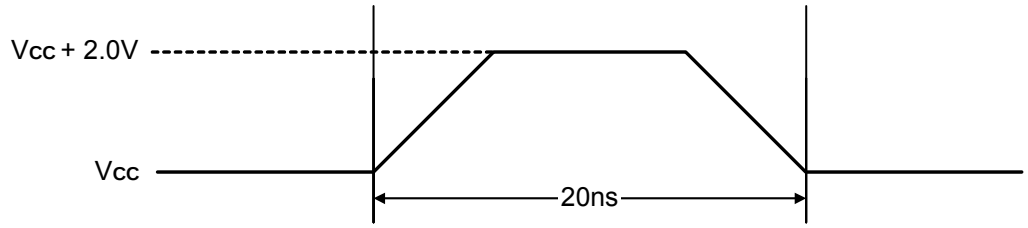


Figure 10. Maximum Positive Input Overshoot



CAPACITANCE (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{OUT}	Output Capacitance (DO)	V_{OUT} = 0V		6	pF
C_{IN}	Input Capacitance (other pins)	V_{IN} = 0V		8	pF

Figure 11. AC Measurement I/O Waveform

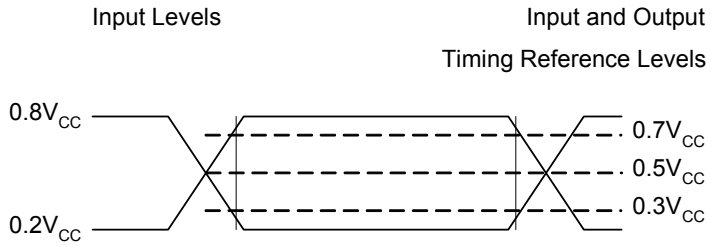


Table 11. DC Characteristics (T_A = -40°C to 85°C, V_{CC} = 2.7V ~ 3.6V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Input Load Current	1			±2	μA	Vcc = Vcc Max, V_{IN} = Vcc or V_{SS}
I_{LO}	Output Leakage Current	1			±2	μA	Vcc = Vcc Max, V_{OUT} = Vcc or V_{SS}
I_{SB1}	Vcc Standby Current	1		2	10	μA	V_{IN} = Vcc or V_{SS}, $\overline{S}$ = Vcc
I_{SB2}	Deep Power-down Current			2	10	μA	V_{IN} = Vcc or V_{SS}, $\overline{S}$ = Vcc
I_{CC1}	Vcc Read	1		15	25	mA	f=104MHz, (4 x I/O read) C=0.1 Vcc /0.9 Vcc, DO=Open
				10	15	mA	f=104MHz, (1 x I/O read) C=0.1 Vcc /0.9 Vcc, DO=Open
				14	20	mA	f_Q =84MHz, (4 x I/O read) C=0.1 Vcc /0.9 Vcc, DO=Open
				10	15	mA	f_T =84MHz, (2 x I/O read) C=0.1 Vcc /0.9 Vcc, DO=Open
				6	8	mA	f =33MHz, C=0.1 Vcc /0.9 Vcc, DO=Open
I_{CC2}	Vcc Program Current (PP)	1		20	25	mA	Program in Progress, $\overline{S}$ = Vcc
I_{CC3}	Vcc Write Status Register (WRSR) Current				20	mA	Program status register in progress, $\overline{S}$ = Vcc
I_{CC4}	Vcc Sector/Block (32K, 64K) Erase Current (SE/BE/BE32K)	1		20	25	mA	Erase in Progress, $\overline{S}$ = Vcc
I_{CC5}	Vcc Chip Erase Current (CE)	1		20	25	mA	Erase in Progress, $\overline{S}$ = Vcc
V_{IL}	Input Low Voltage		-0.5		0.8	V	
V_{IH}	Input High Voltage		0.7 Vcc		Vcc +0.4	V	
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage		Vcc -0.2			V	I_{OH} = -100μA

Notes:

1. Typical values at Vcc = 3.3V, T_A = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 12. AC Characteristics (T_A = -40°C to 85°C, V_{CC} = 2.6V ~ 3.7V)

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
f_C	f_C	Clock Frequency for the following instructions: FAST READ, PP, 4PP, SE, BE, CE, DP, RES, RDP WREN, WRDI, RDID, RDSR, WRSR		D.C.		104	MHz
f_{RC}	f_R	Clock Frequency for READ instructions				66	MHz
f_{TC}	f_T	Clock Frequency for 2READ instructions				84	MHz
	f_Q	Clock Frequency for 4READ instructions (5)				84/104	MHz
t_{CH} (1)(2)	t_{CLH}	Clock High Time	Serial (f_C)	4.5			ns
			4PP and Normal Read (f_{RC})	4.5			ns
t_{CL} (1)(2)	t_{CLL}	Clock Low Time	Serial (f_C)	4.5			ns
			4PP and Normal Read (f_{RC})	4.5			ns
t_{CLCH} (2)		Clock Rise Time (3) (peak to peak)		0.1			V/ns
t_{CHCL} (2)		Clock Fall Time (3) (peak to peak)		0.1			V/ns
t_{SLCH} (2)	t_{CSS}	$\overline{S}$ Active Setup Time (relative to C)		4			ns
t_{CHSL} (2)		$\overline{S}$ Not Active Hold Time (relative to C)		4			ns
t_{DVCH}	t_{DSU}	Data In Setup Time		2			ns
t_{CHDX} (2)	t_{DH}	Data In Hold Time		3			ns
t_{CHSH}		$\overline{S}$ Active Hold Time (relative to C)		5			ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time (relative to C)		5			ns
t_{SHSL} (3)	t_{CSH}	$\overline{S}$ Deselect Time	Read	10			ns
			Write/Erase/Program	30			ns
t_{SHQZ} (2)	t_{DIS}	Output Disable Time				8	ns
t_{CLQV}	t_V	Clock Low to Output Valid Loading: 30pF/15pF	Loading: 30pF			8	ns
			Loading: 15pF			6	ns
t_{CLQX}	t_{HO}	Output Hold Time		0			ns
t_{WHSL}		Write Protect Setup Time		20			ns
t_{SHWL}		Write Protect Hold Time		100			ns
t_{DP} (2)		$\overline{S}$ High to Deep Power-down Mode				10	µs
t_{RES1} (2)		$\overline{S}$ High to Standby Mode without Electronic Signature Read				10	µs
t_{RES2} (2)		$\overline{S}$ High to Standby Mode with Electronic Signature Read				10	µs
t_{RCR}		Recovery Time from Read				20	µs
t_{RCP}		Recovery Time from Program				20	µs
t_{RCE}		Recovery Time from Erase				12	ms
t_W		Write Status Register Cycle Time				40	ms
t_{BP}		Byte-Program			6	30	µs
t_{PP}		Page Program Cycle Time			0.3	0.8/2 (6)	ms
t_{SE}		Sector Erase Cycle Time			40	150	ms
t_{BE32}		Block Erase (32KB) Cycle Time			80	300	ms
t_{BE}		Block Erase (64KB) Cycle Time			120	500	ms
t_{CE}		Chip Erase Cycle Time			12	25	s

Notes:

1. t_{CH} + t_{CL} must be greater than or equal to 1/ Frequency.
2. Value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
4. Test condition is shown as Figure 11.
5. When dummy cycle=4 (In both QPI & SPI mode), clock rate=84MHz; when dummy cycle=6 (In both QPI & SPI mode), clock rate=104MHz.
6. The page program time is 0.8ms(max.) after 10K cycling and 2ms(max.) after 100K cycling.

Timing Analysis

Figure 12. Serial Input Timing

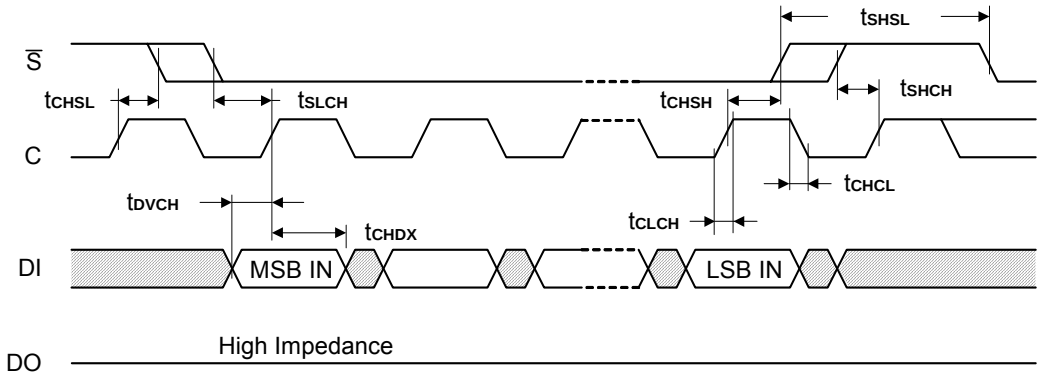


Figure 13. Output Timing

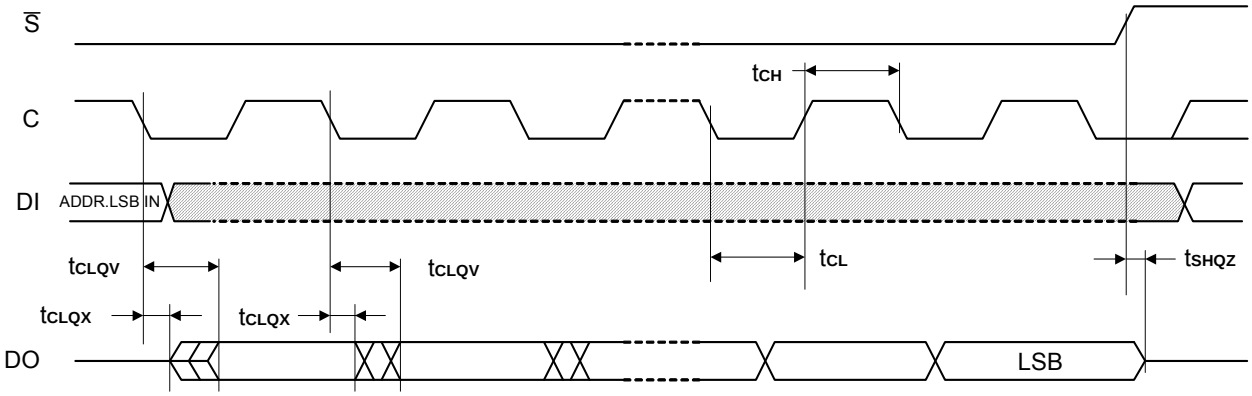


Figure 14. Write Protect Setup and Hold Timing during WRSR when SRWD=1

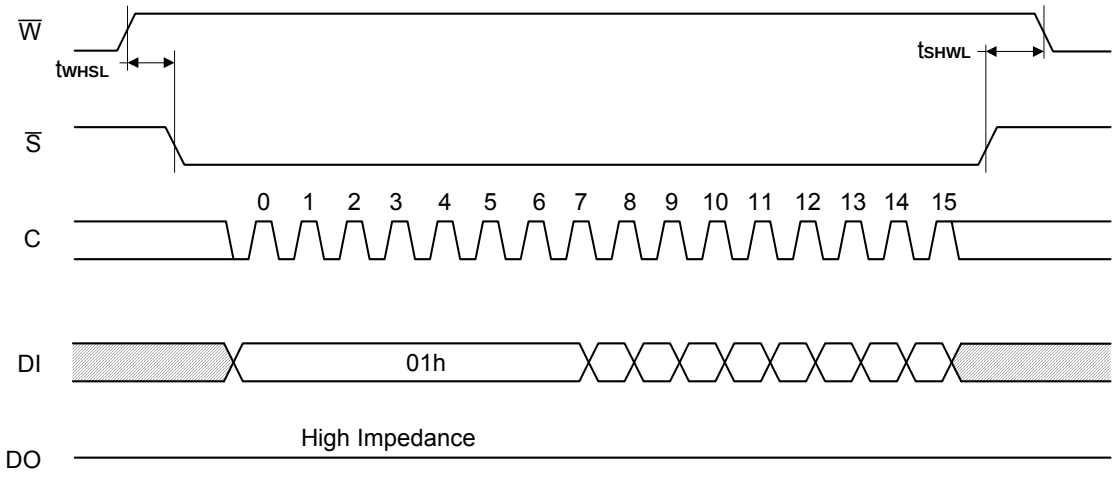


Figure 15-1. Write Enable (WREN) Sequence (Command 06) (SPI Mode)

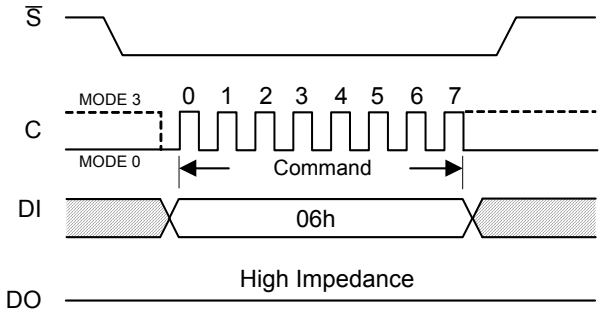


Figure 15-2. Write Enable (WREN) Sequence (Command 06) (QPI Mode)

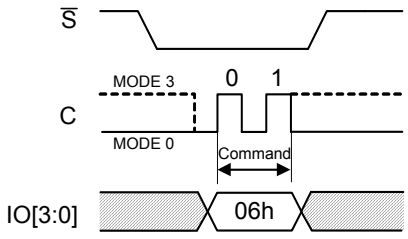


Figure 16-1. Write Disable (WRDI) Sequence (Command 04) (SPI Mode)

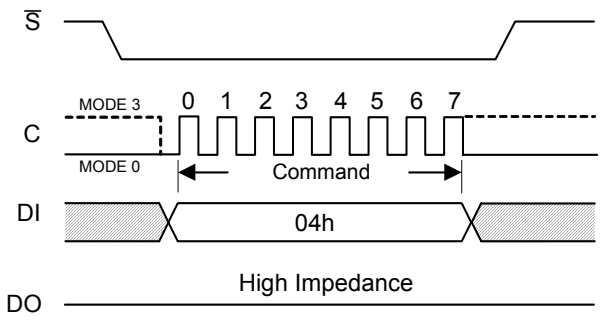


Figure 16-2. Write Disable (WRDI) Sequence (Command 04) (QPI Mode)

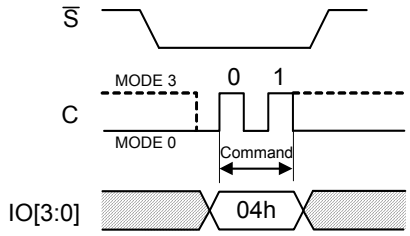


Figure 17. Read Identification (RDID) Sequence (Command 9F) (SPI mode only)

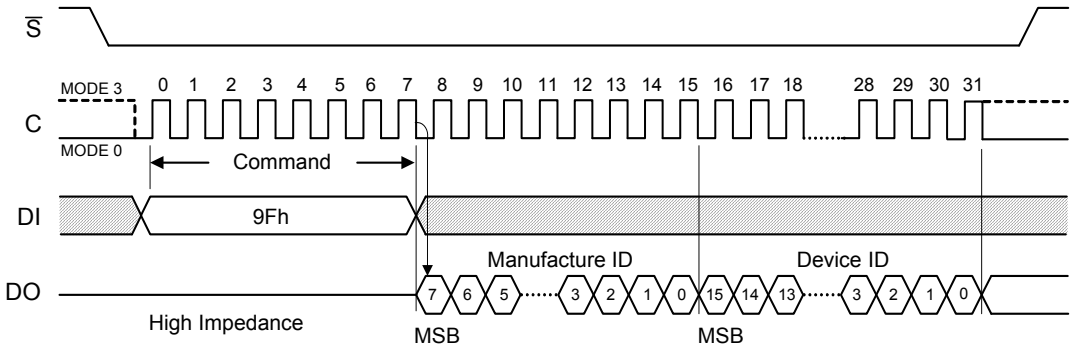


Figure 18-1. Read Status Register (RDSR) Sequence (Command 05) (SPI Mode)

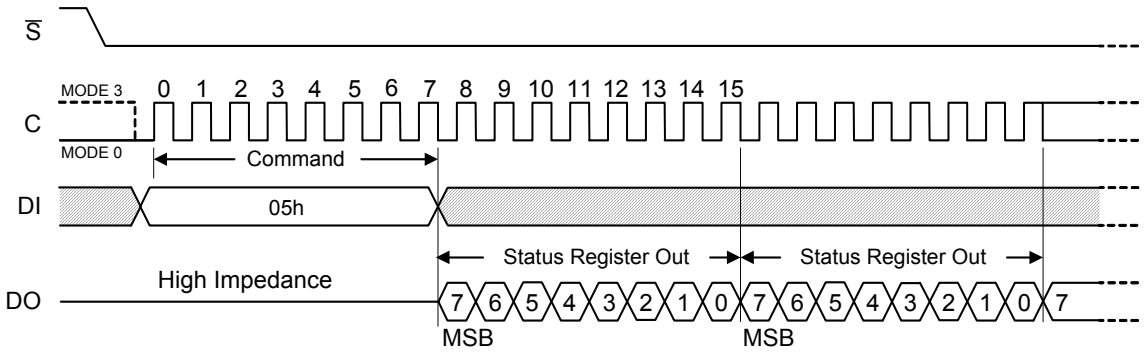


Figure 18-2. Read Status Register (RDSR) Sequence (Command 05) (QPI Mode)

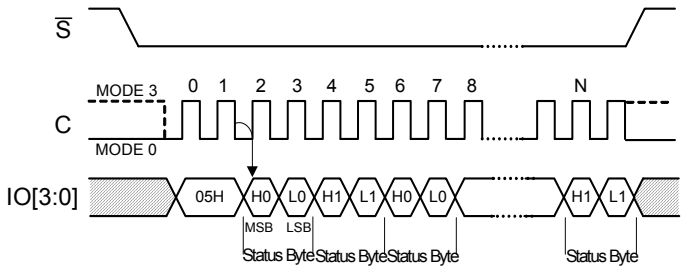
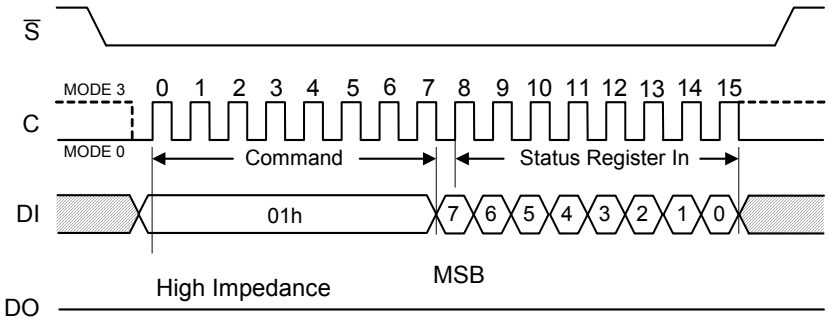


Figure 19-1. Write Status Register (WRSR) Sequence (Command 01) (SPI Mode)



Note: Also supported in QPI mode with command and subsequent input/output in Quad I/O mode.

Figure 19-2. Write Status Register (WRSR) Sequence (Command 01) (QPI Mode)

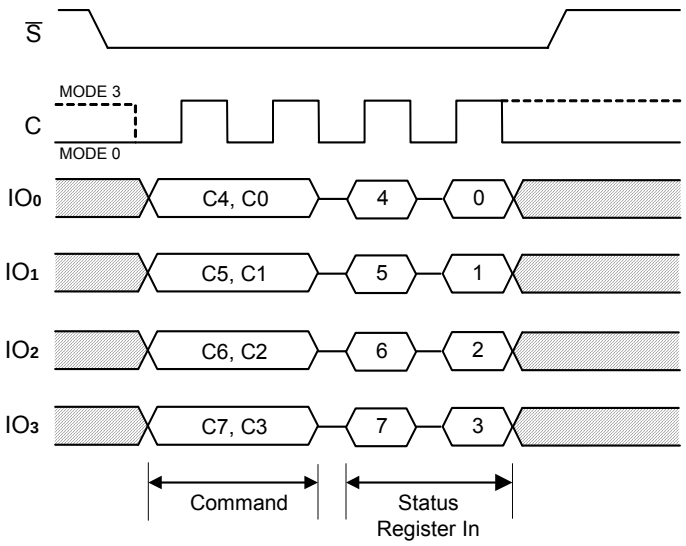


Figure 20. Read Data Bytes (READ) Sequence (Command 03) (SPI Mode only) (66MHz)

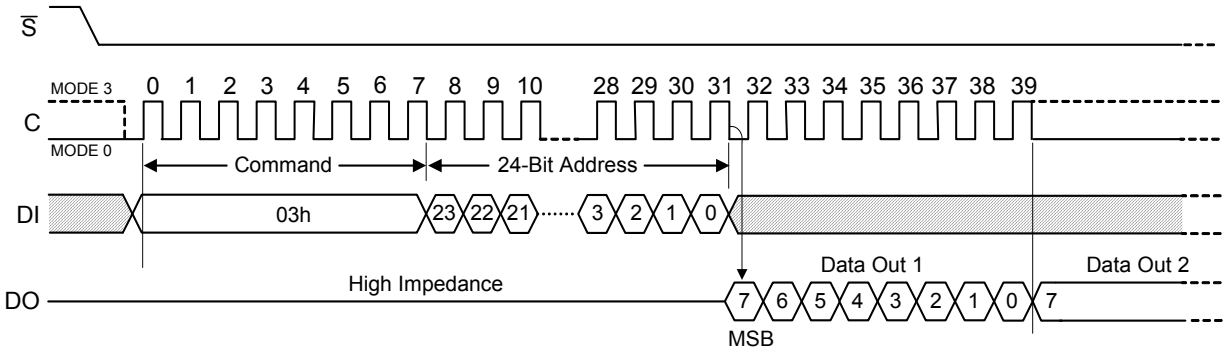


Figure 21-1. Read at Higher Speed (FAST READ) Sequence (Command 0B) (SPI Mode) (104MHz)

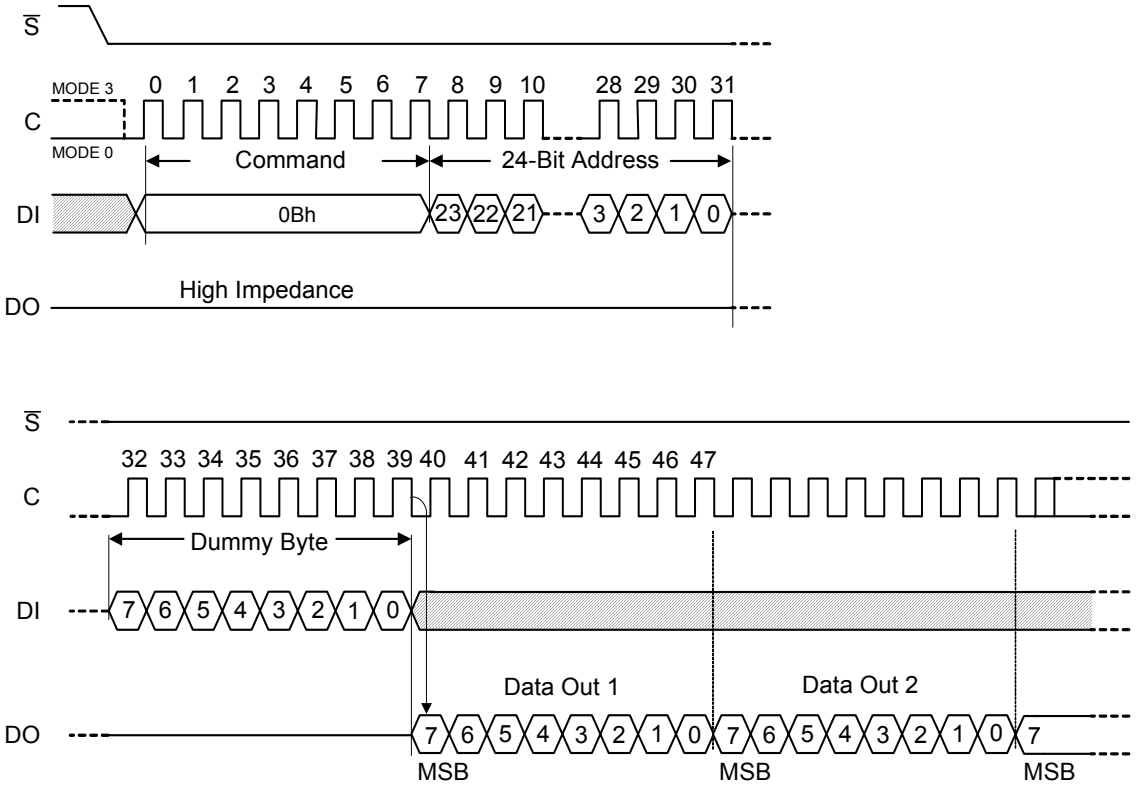


Figure 21-2. Read at Higher Speed (FAST READ) Sequence (Command 0B) (QPI Mode) (84MHz)

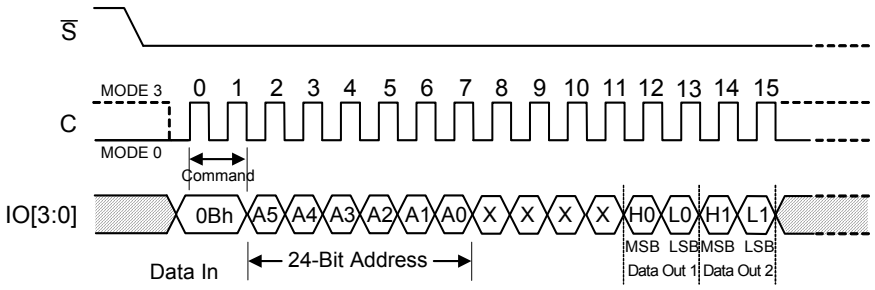


Figure 22. 2 x I/O Read Mode Sequence (Command BB) (SPI Mode only) (84MHz)

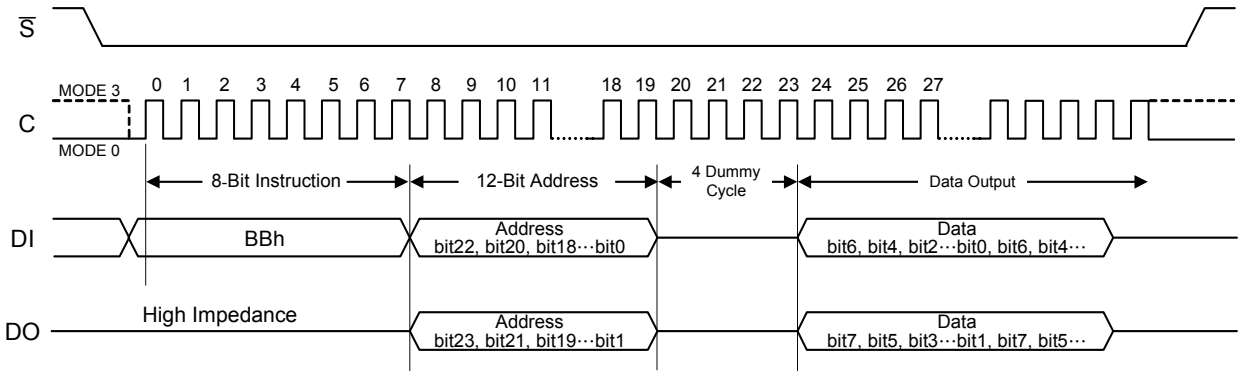
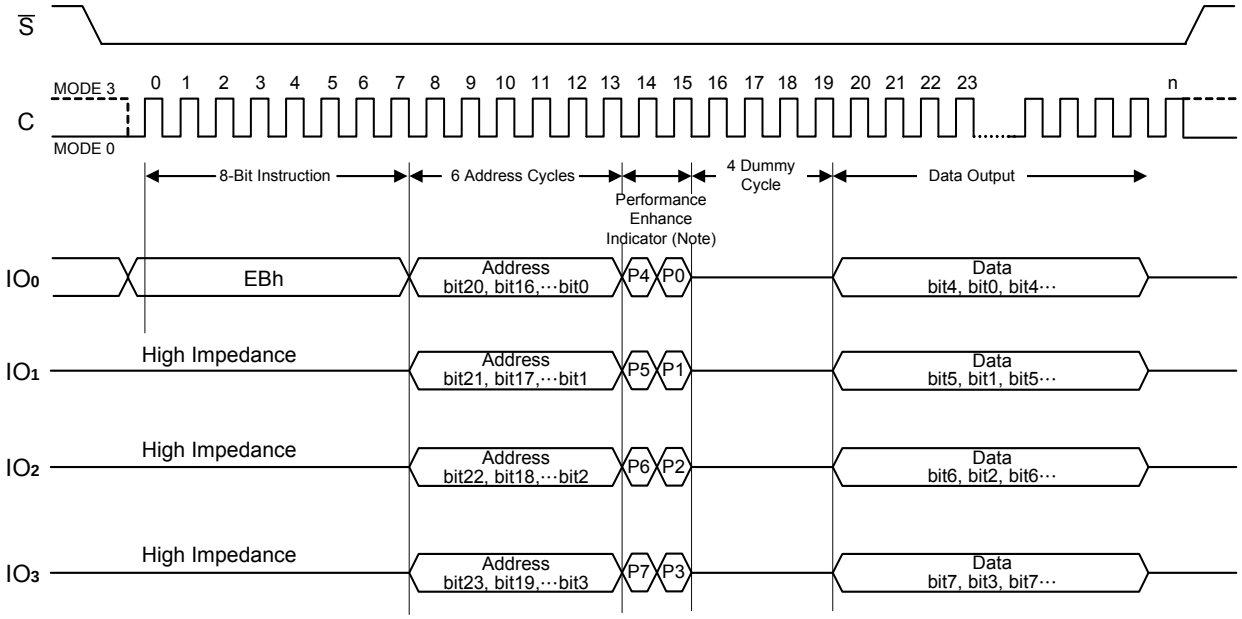


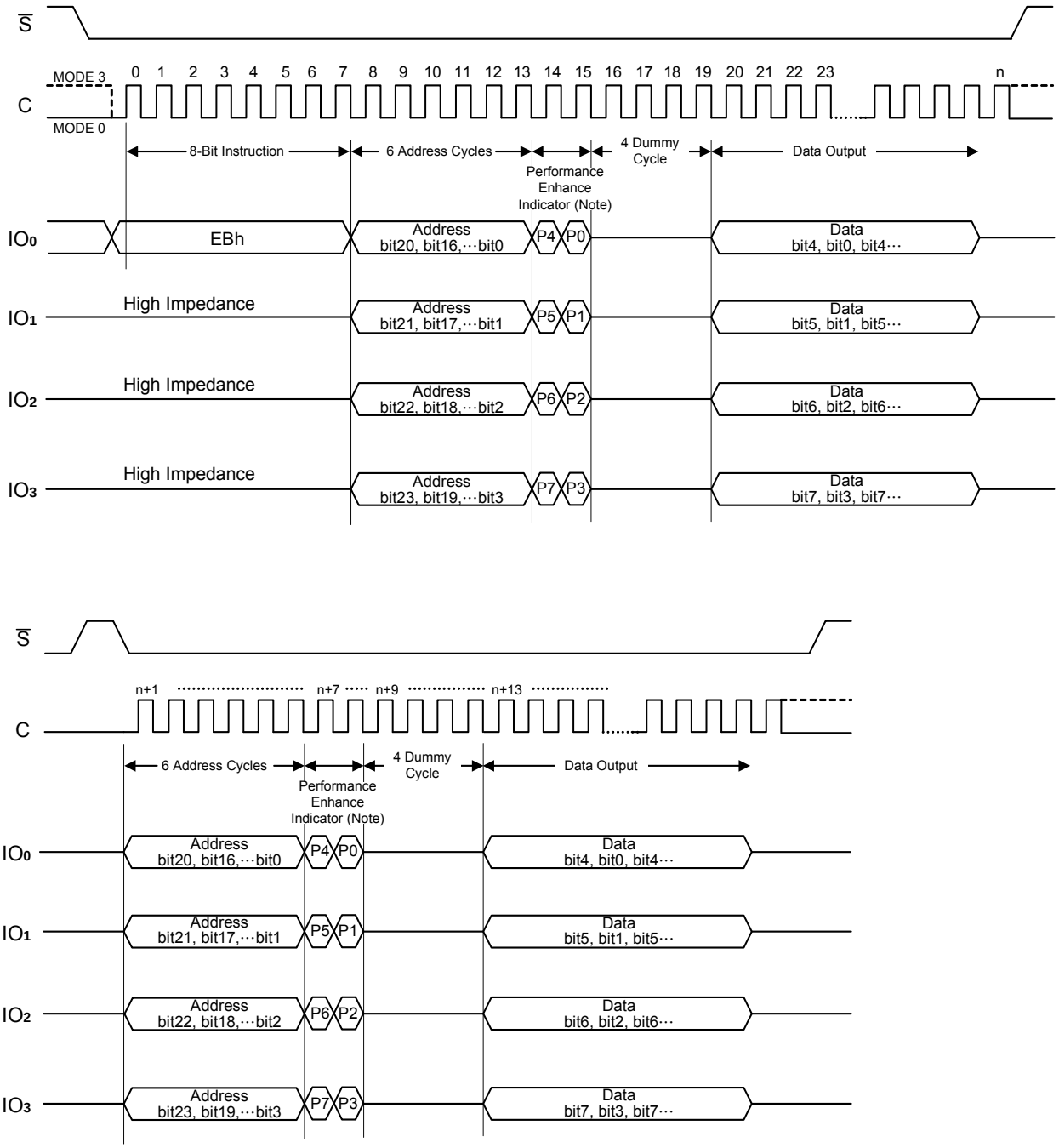
Figure 23. 4 x I/O Read Mode Sequence (Command EB) (SPI Mode) (104MHz)



Notes:

1. Also supported in QPI mode with command and subsequent input/output in Quad I/O mode and runs at 104MHz.
2. Hi-impedance is inhibited for the two clock cycles.
3. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.

Figure 24-1. 4 x I/O Read enhance performance Mode Sequence (Command EB) (SPI Mode) (104MHz)



Notes:

Performance enhance mode, if P7≠P3 & P6≠P2 & P5≠P1 & P4≠P0 (Toggling), ex: A5, 5A, 0F, if not using performance enhance recommend to keep 1 or 0 in performance enhance indicator.

Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF

Figure 24-2. 4 x I/O Read enhance performance Mode Sequence (Command EB) (QPI Mode) (104MHz)

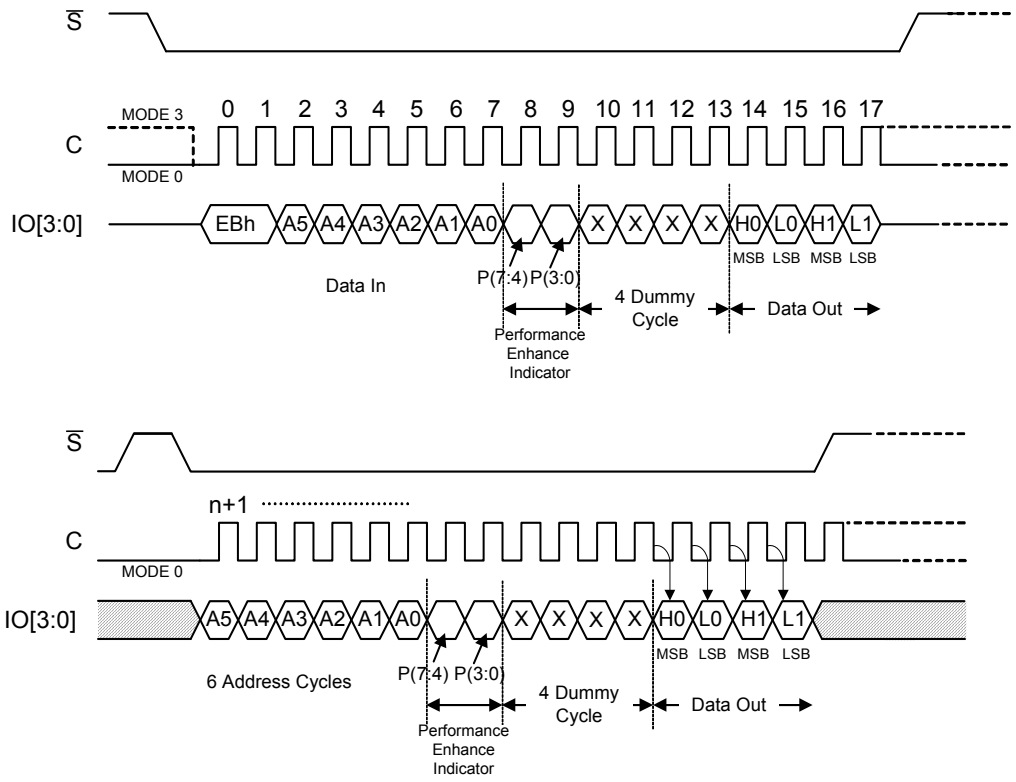


Figure 25-1. Page Program (PP) Sequence (Command 02) (SPI Mode)

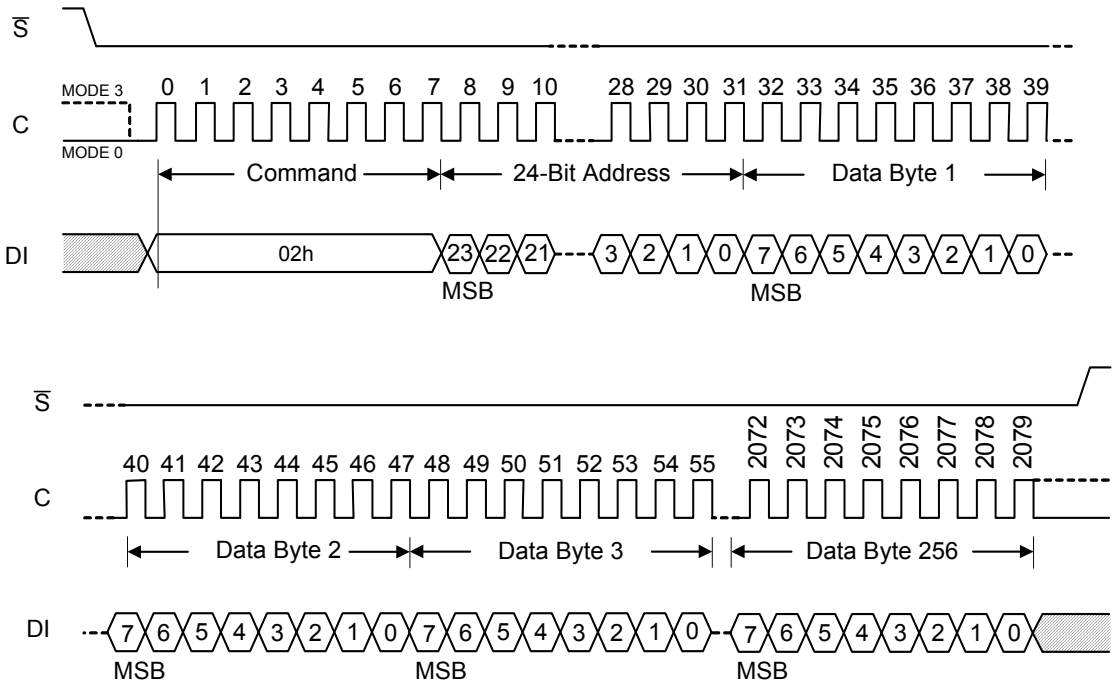


Figure 25-2. Page Program (PP) Sequence (Command 02) (QPI Mode)

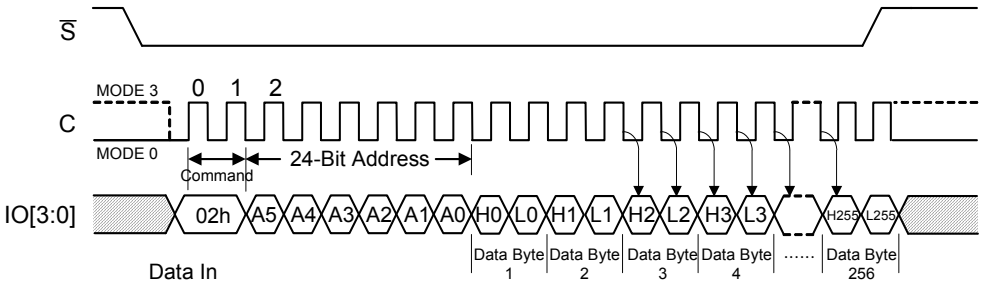


Figure 26. 4 x I/O Page Program (4PP) Sequence (Command 38) (SPI Mode only)

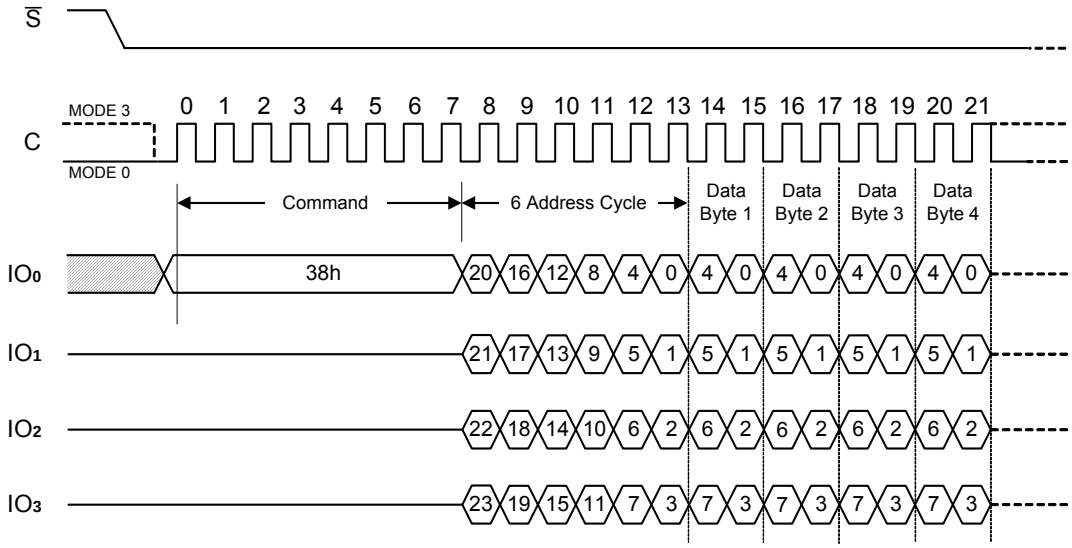


Figure 27-1. Sector Erase (SE) Sequence (Command 20) (SPI Mode)

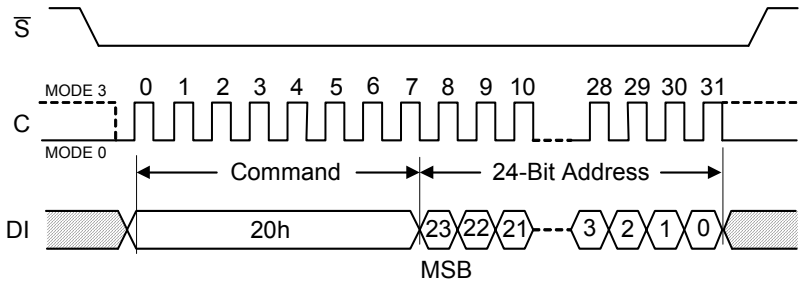


Figure 27-2. Sector Erase (SE) Sequence (Command 20) (QPI Mode)

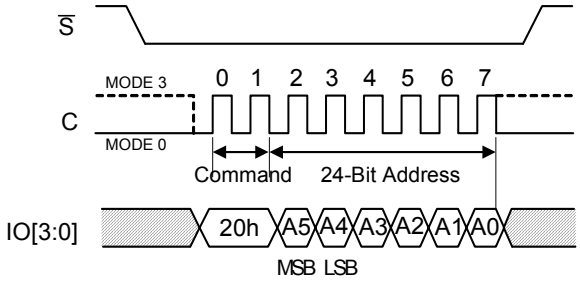


Figure 28-1. Block Erase 32KB (BE32K) Sequence (Command 52) (SPI Mode)

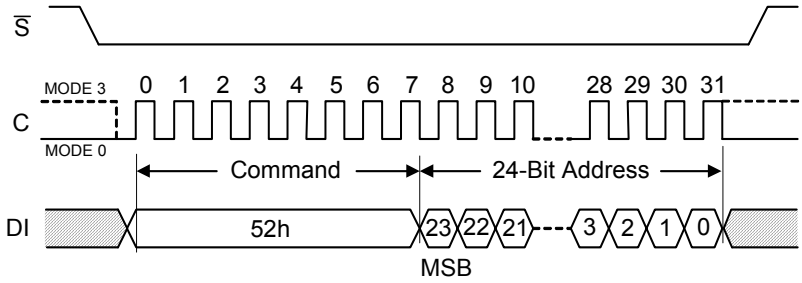


Figure 28-2. Block Erase 32KB (BE32K) Sequence (Command 52) (QPI Mode)

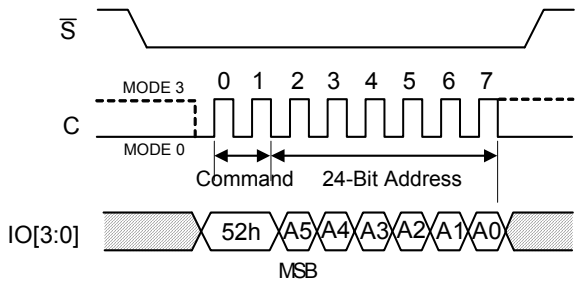


Figure 29-1. Block Erase (BE) Sequence (Command D8) (SPI Mode)

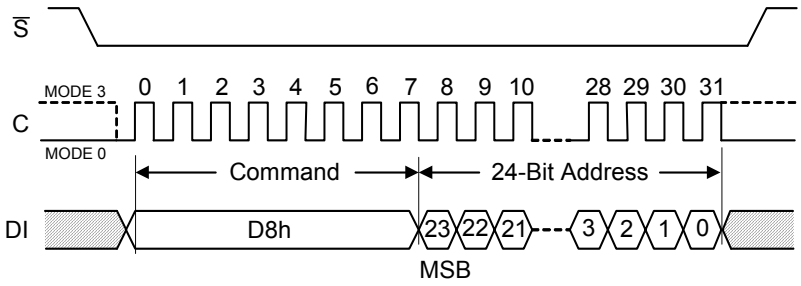


Figure 29-2. Block Erase (BE) Sequence (Command D8) (QPI Mode)

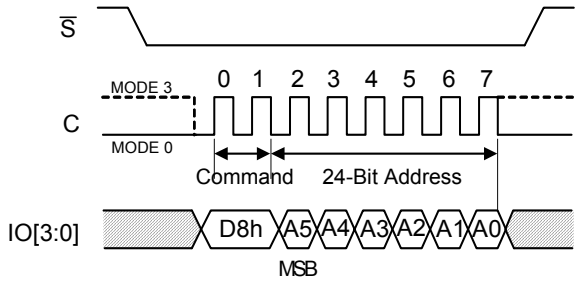


Figure 30-1. Chip Erase (CE) Sequence (Command 60 or C7) (SPI Mode)

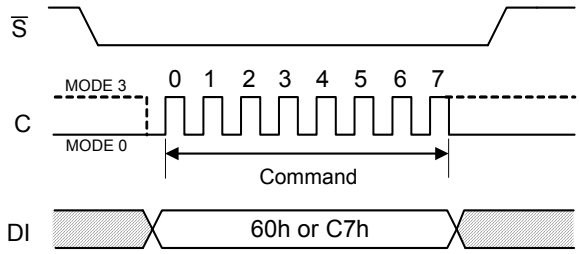


Figure 30-2. Chip Erase (CE) Sequence (Command 60 or C7) (QPI Mode)

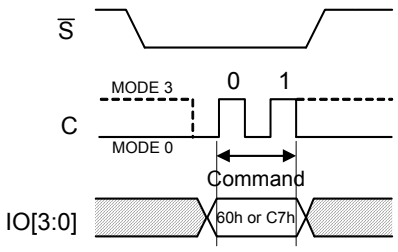


Figure 31-1. Deep Power-down (DP) Sequence (Command B9) (SPI Mode)

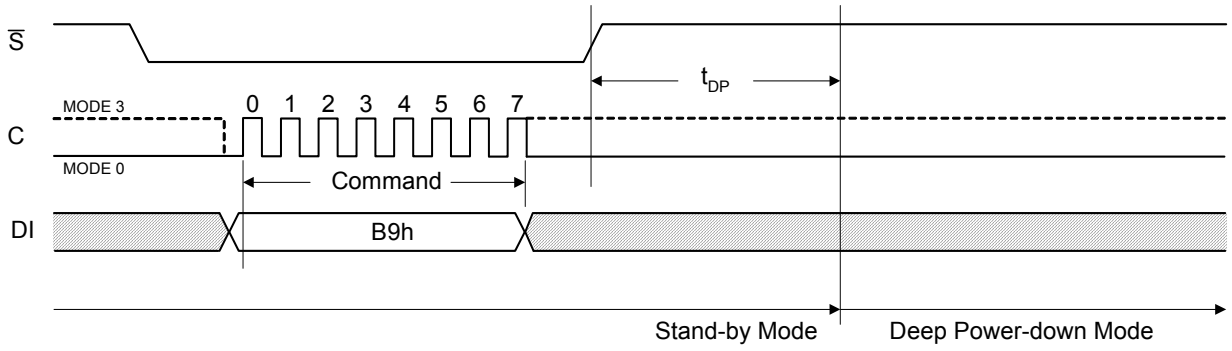


Figure 31-2. Deep Power-down (DP) Sequence (Command B9) (QPI Mode)

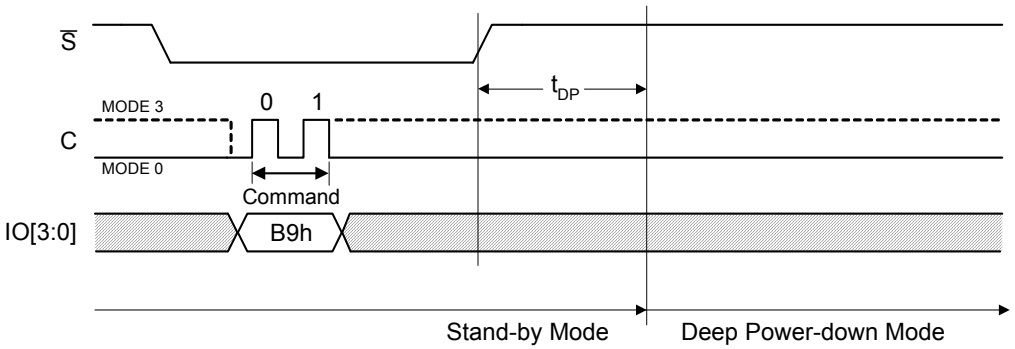


Figure 32. Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Command AB) (SPI Mode Only)

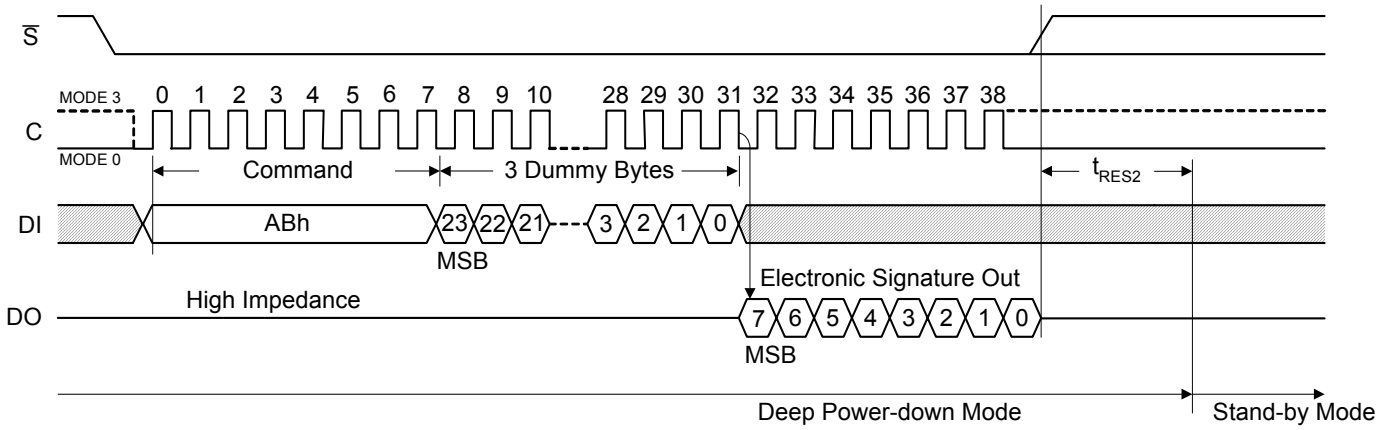


Figure 33-1. Release from Deep Power-down (RDP) Sequence (Command AB) (SPI Mode)

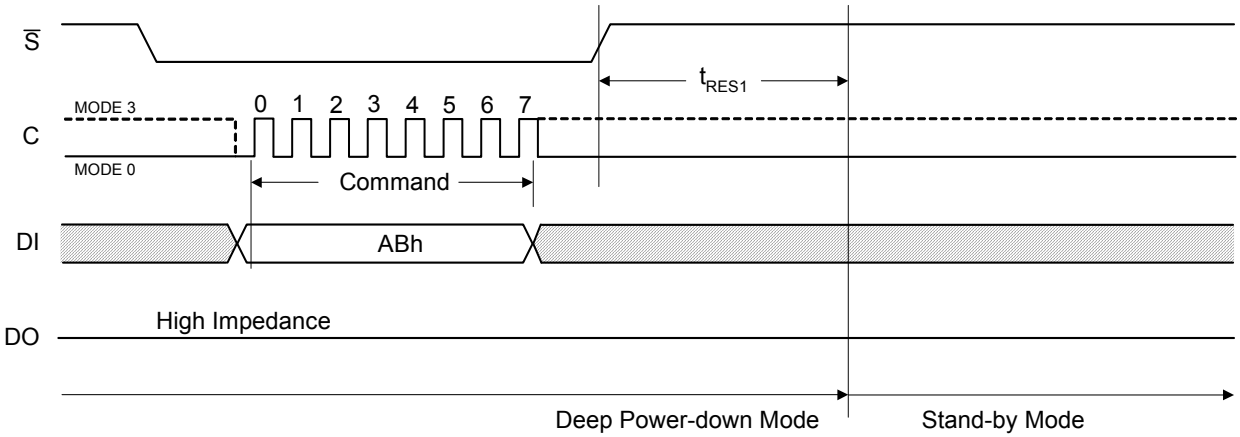


Figure 33-2. Release from Deep Power-down (RDP) Sequence (Command AB) (QPI Mode)

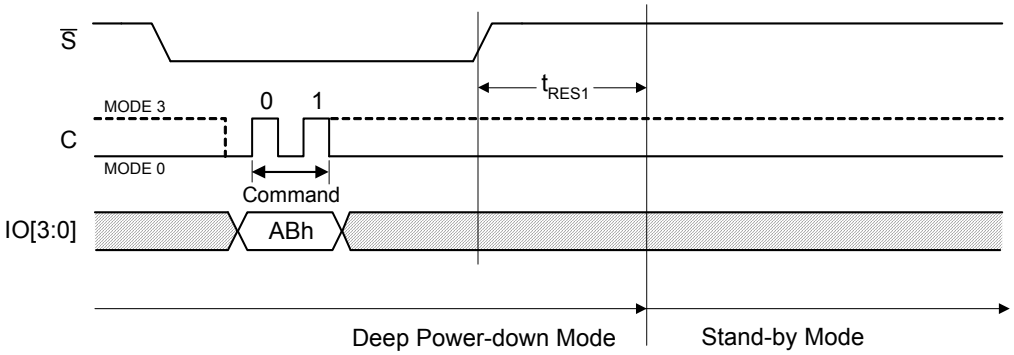
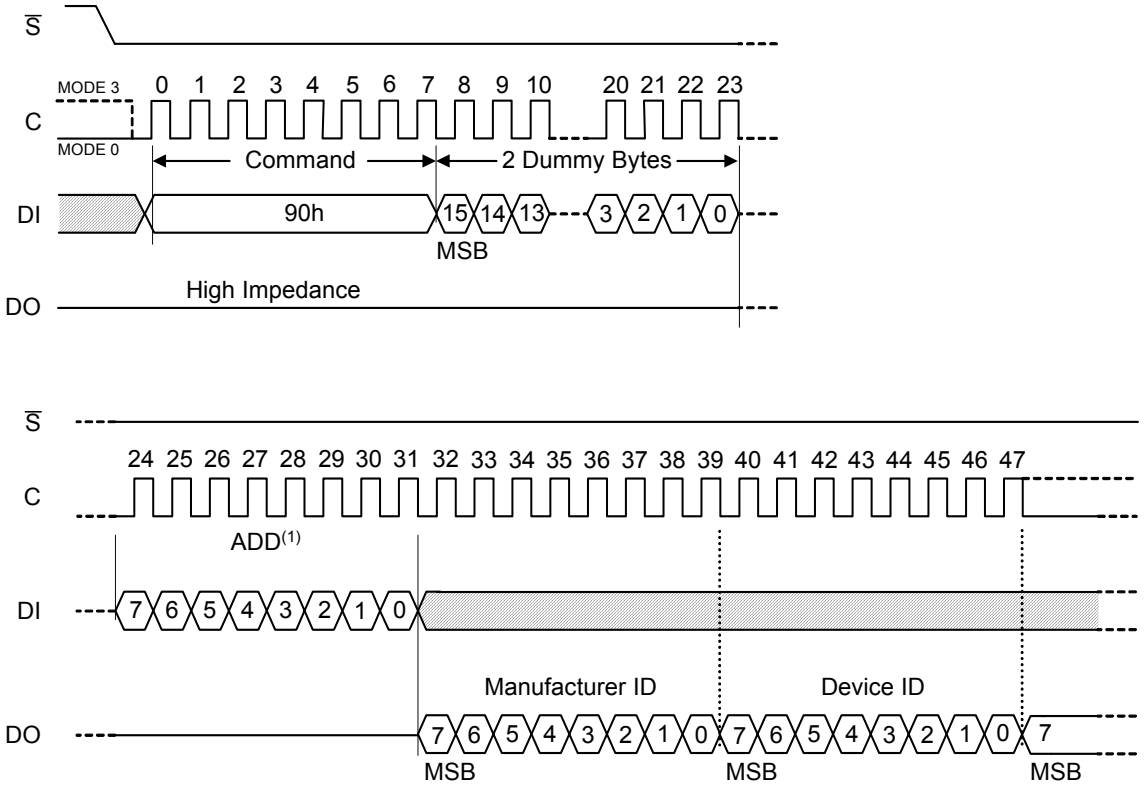


Figure 34. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90) (SPI Mode Only)



Notes:

1. ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

Figure 35-1. Read Security Register (RDSCUR) Sequence (Command 2B) (SPI Mode)

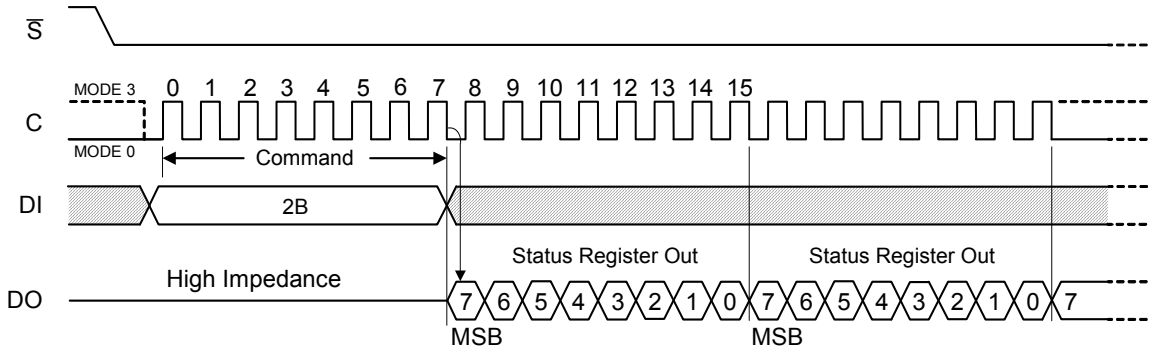


Figure 35-2. Read Security Register (RDSCUR) Sequence (Command 2B) (QPI Mode)

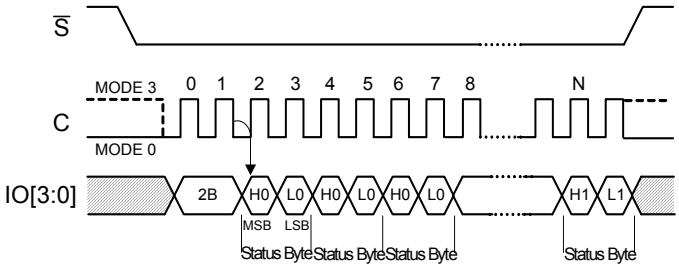
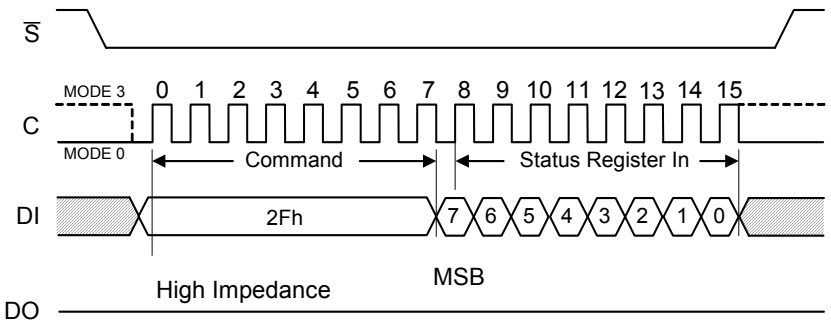


Figure 36-1. Write Security Register (WRSCUR) Sequence (Command 2F) (SPI Mode)



Note: Also supported in QPI mode with command and subsequent input/output in Quad I/O mode.

Figure 36-2. Write Security Register (WRSCUR) Sequence (Command 2F) (QPI Mode)

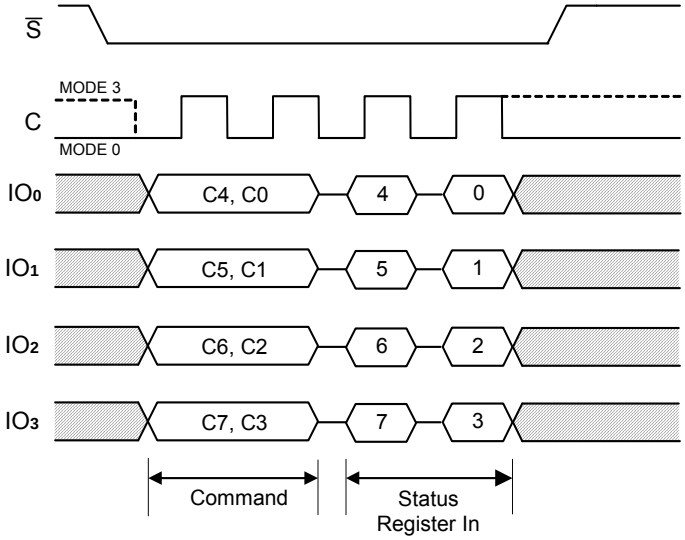


Figure 37. Word Read Quad I/O Instruction Sequence (Initial Word Read Quad I/O instruction or previous P4=P0) (SPI Mode only) (84MHz)

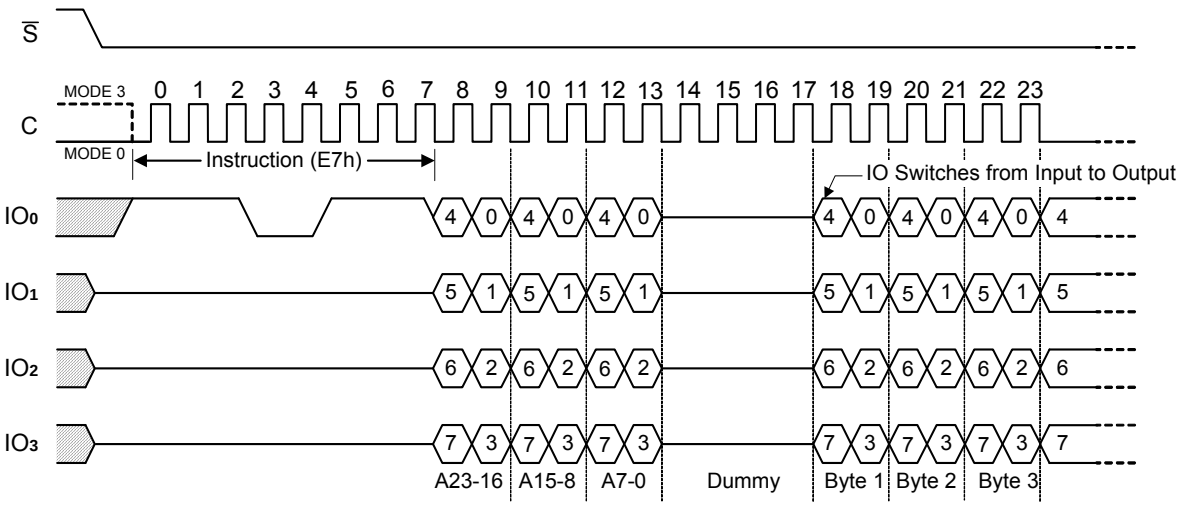


Figure 38. Performance Enhance Mode Reset for Fast Read Quad I/O (SPI and QPI Mode)

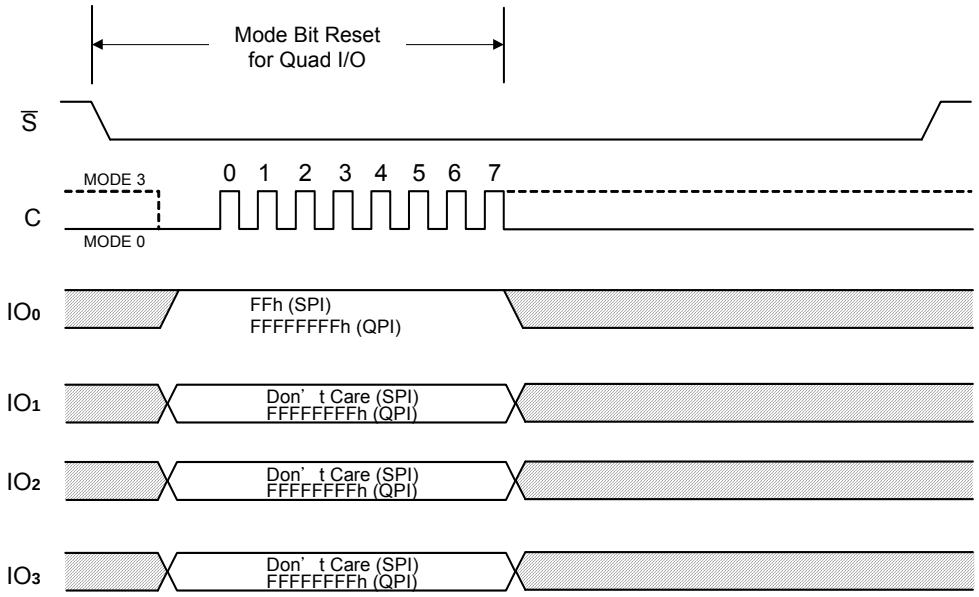


Figure 39-1. Reset Sequence (SPI Mode)

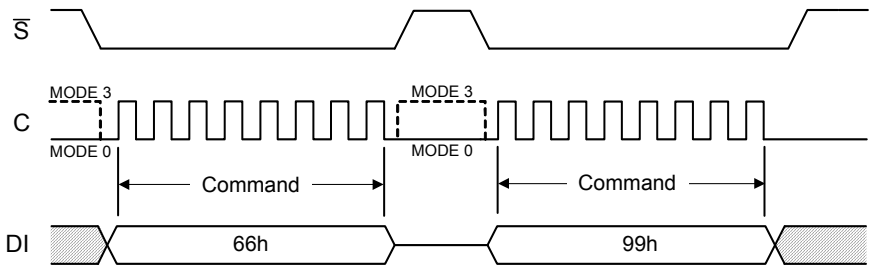


Figure 39-2. Reset Sequence (QPI Mode)

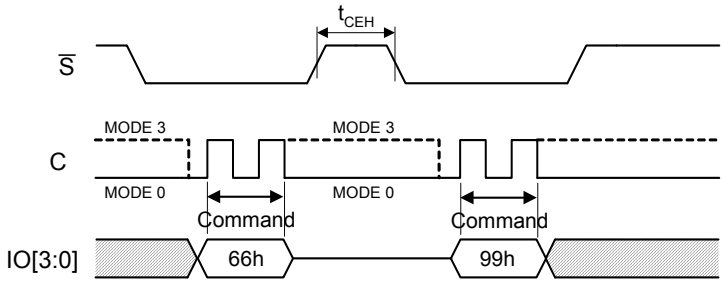


Figure 40. Enable Quad I/O Sequence

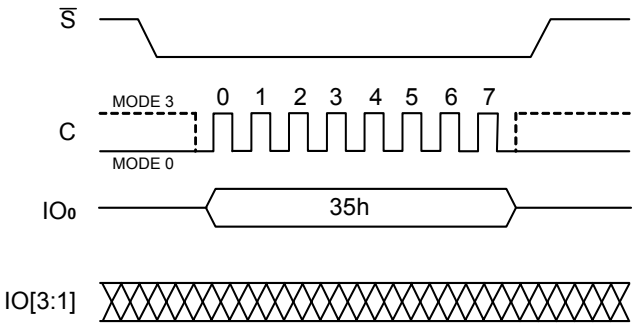


Figure 41-1. Suspend to Read Latency

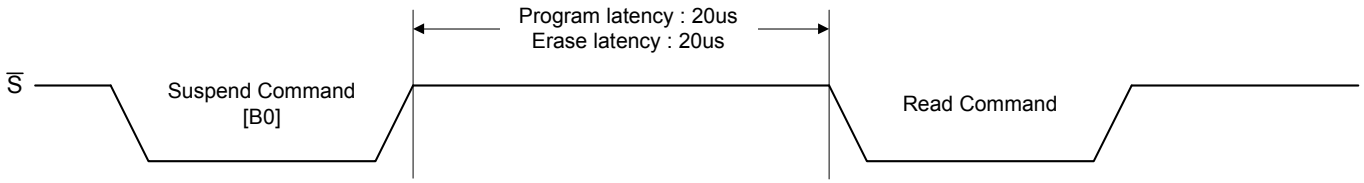


Figure 41-2. Resume to Read Latency

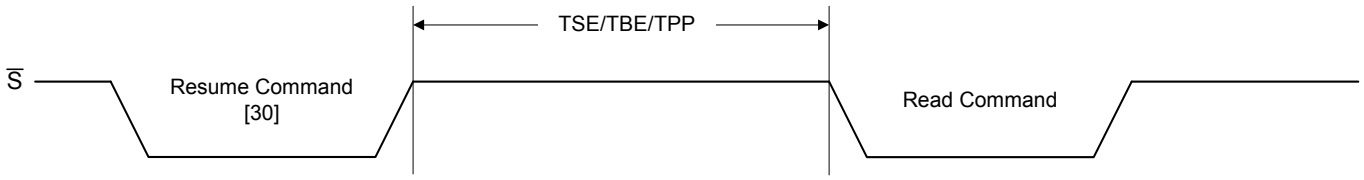


Figure 41-3. Resume to Suspend Latency

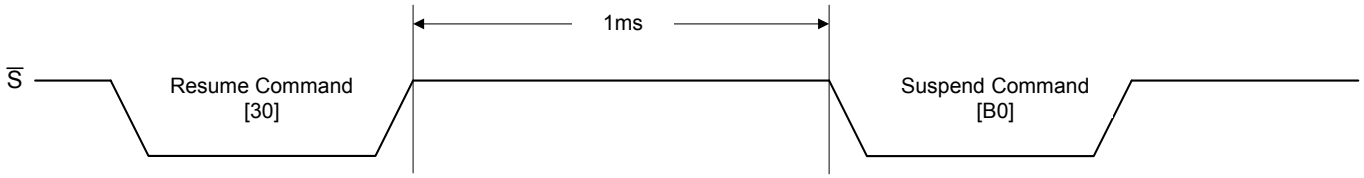
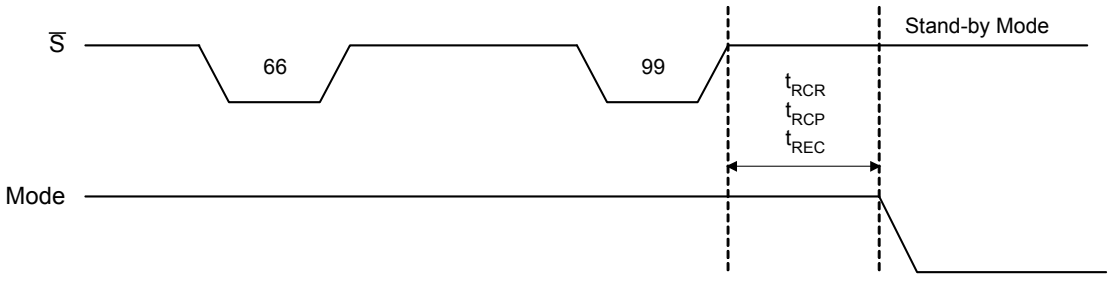
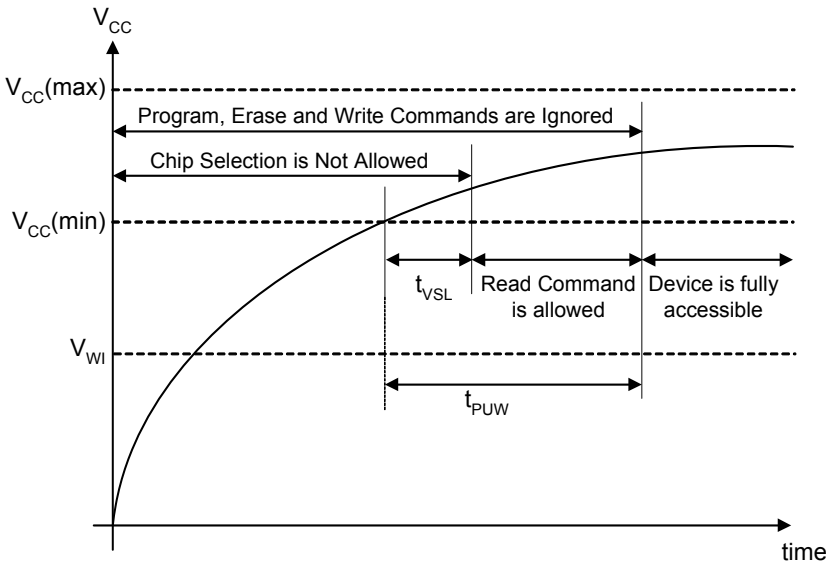


Figure 42. Software Reset Recovery



t_{RCR}: 20us (Recovery Time from Read)
t_{RCP}: 20us (Recovery Time from Program)
t_{REC}: 12ms (Recovery Time from Erase)

Figure 43. Power-up Timing



Note: Vcc (max.) is 3.7V and Vcc (min.) is 2.6V.

Table 13. Power-Up Timing and V_{WI} Threshold

Symbol	Parameter	Min.	Max.	Unit.
t_{VSL}(1)	Vcc(min) to $\overline{S}$ low (Vcc Rise Time)	100		μs
t_{PUW}(1)	Time delay to Write instruction	300		μs
V_{WI}(1)	Command Inhibit Voltage	2.2	2.4	V

Note: 1. These parameters are characterized only.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

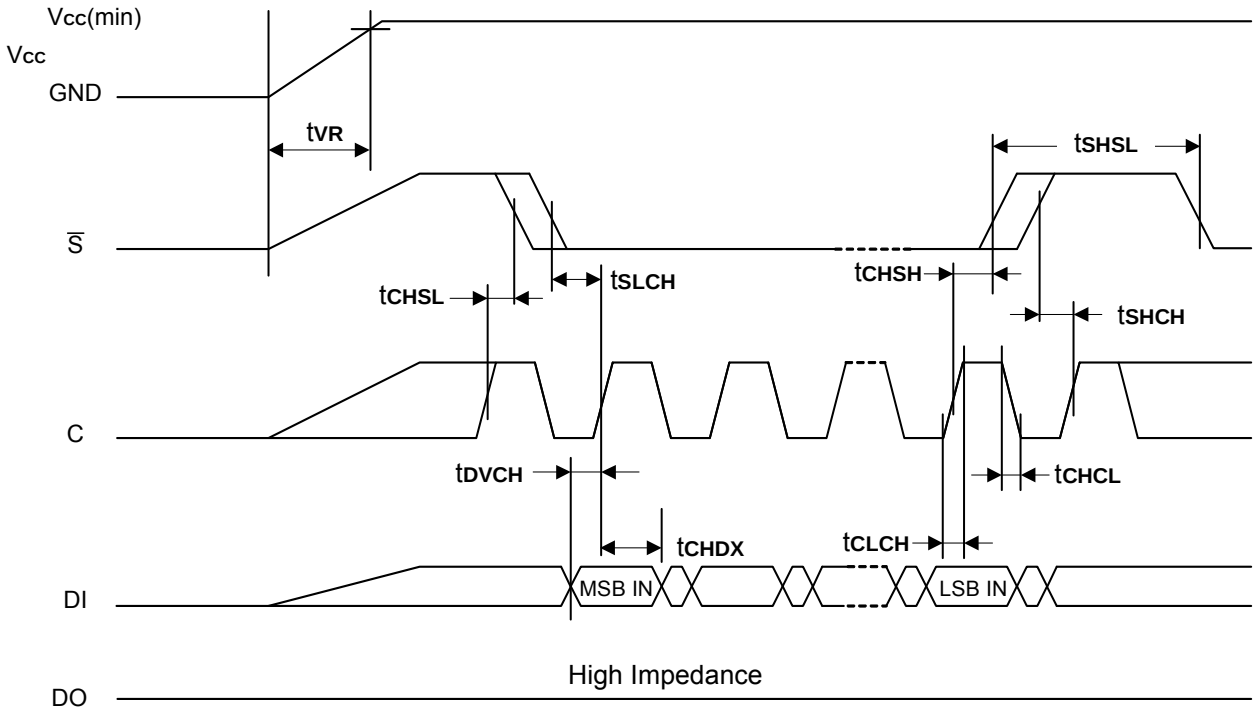
OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in Figure 44 and Figure 45 are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, $\overline{S}$ needs to follow the voltage applied on Vcc to keep the device not to be selected. The $\overline{S}$ can be driven low when V Vcc reach Vcc (min.) and wait a period of t_{VSL}.

Figure 44. AC Timing at Device Power-Up

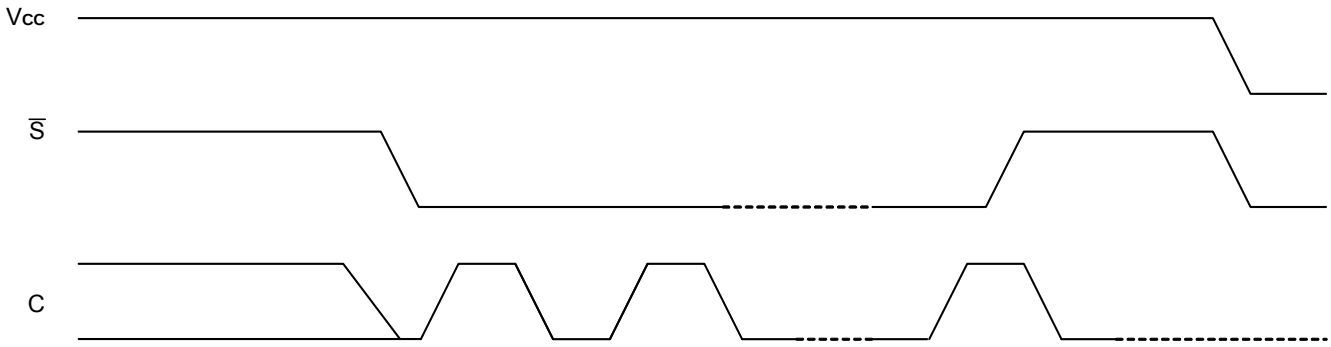


Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	Vcc Rise Time	1	20	500000	μs/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec t_{CHSL}, t_{SLCH}, t_{DVCH}, t_{CHDX}, t_{SHSL}, t_{CHSH}, t_{SHCH}, t_{CHCL}, t_{CLCH} in the figure, please refer to "AC CHARACTERISTICS" table.

Figure 45. Power-Down Sequence

During power-down, $\overline{S}$ needs to follow the voltage drop on VCC to avoid mis-operation.



ERASE AND PROGRAMMING PERFORMANCE

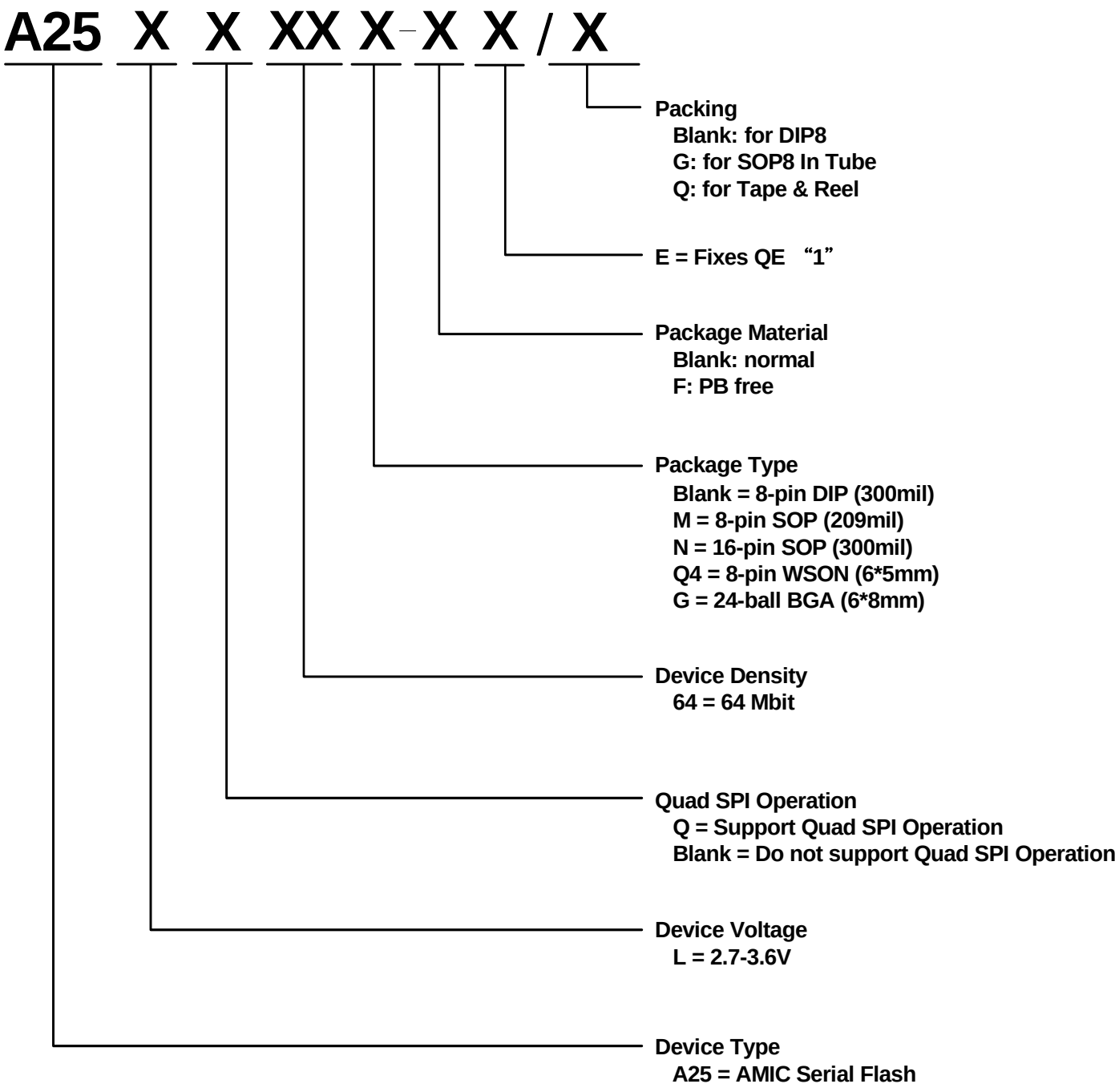
Parameter	Min.	Typ. (1)	Max. (2)	Unit.
Write Status Register Cycle Time			40	ms
Sector Erase Cycle Time (4KB)		40	150	ms
Block Erase Cycle Time (32KB)		80	300	ms
Block Erase Cycle Time (64KB)		120	500	ms
Chip Erase Cycle Time		12	25	s
Byte Program Time (via page program command)		6	30	μs
Page Program Time		0.3	0.8/2(5)	ms
Erase/Program Cycle		100,000		cycles

Notes:
1. Typical program and erase time assumes the following conditions: 25°C, 3.3V, and checker board pattern.
2. Under worst conditions of 85°C and 2.7V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. The maximum chip programming time is evaluated under the worst conditions of 0C, Vcc=3.3V, and 100K cycle with 90% confidence level.
5. The page program time is 0.8ms(max.) after 10K cycling and 2ms(max.) after 100K cycling.

LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all power pins, DI, $\overline{S}$	-1.0V	2 Vcc max
Input Voltage with respect to V_{SS} on DO	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 3V, one pin at a time.		

Part Numbering Scheme



Ordering Information

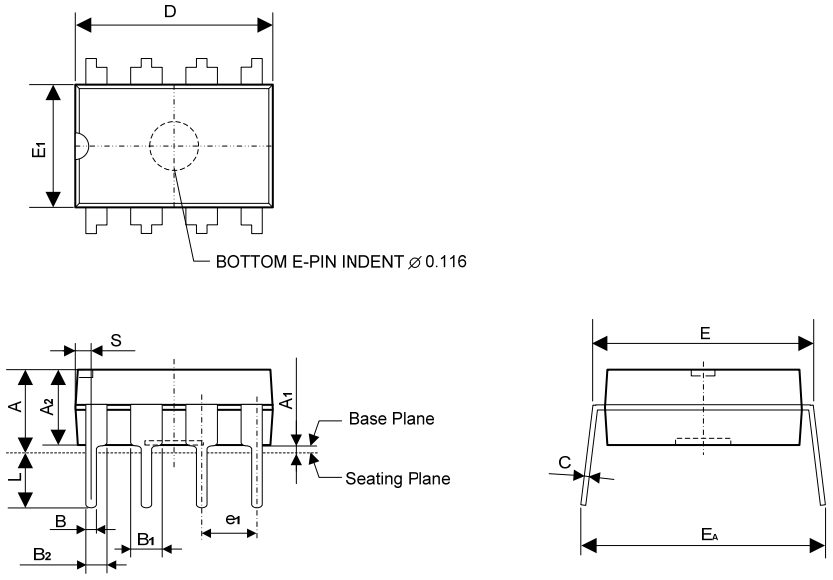
Part No.	Speed (MHz)	Active Read Current Max. (mA)	Program/Erase Current Max. (mA)	Standby Current Max. (μA)	Package
A25LQ64-F	104/84	25/20	25	10	8 Pin Pb-Free DIP (300 mil)
A25LQ64M-F					8-Pin Pb-Free SOP (209mil)
A25LQ64M-FE					8-Pin Pb-Free SOP (209mil)
A25LQ64N-F					16-Pin Pb-Free SOP (300mil)
A25LQ64Q4-F					8-Pin Pb-Free WSON (6*5mm)
A25LQ64G-F					24-Ball Pb-Free BGA (6*8mm)

Operating temperature range: -40°C ~ +85°C

Package Information

P-DIP 8L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.180	-	-	4.57
A_1	0.015	-	-	0.38	-	-
A_2	0.128	0.130	0.136	3.25	3.30	3.45
B	0.014	0.018	0.022	0.36	0.46	0.56
B_1	0.050	0.060	0.070	1.27	1.52	1.78
B_2	0.032	0.039	0.046	0.81	0.99	1.17
C	0.008	0.010	0.013	0.20	0.25	0.33
D	0.350	0.360	0.370	8.89	9.14	9.40
E	0.290	0.300	0.315	7.37	7.62	8.00
E_1	0.254	0.260	0.266	6.45	6.60	6.76
e_1	-	0.100	-	-	2.54	-
L	0.125	-	-	3.18	-	-
E_A	0.345	-	0.385	8.76	-	9.78
S	0.016	0.021	0.026	0.41	0.53	0.66

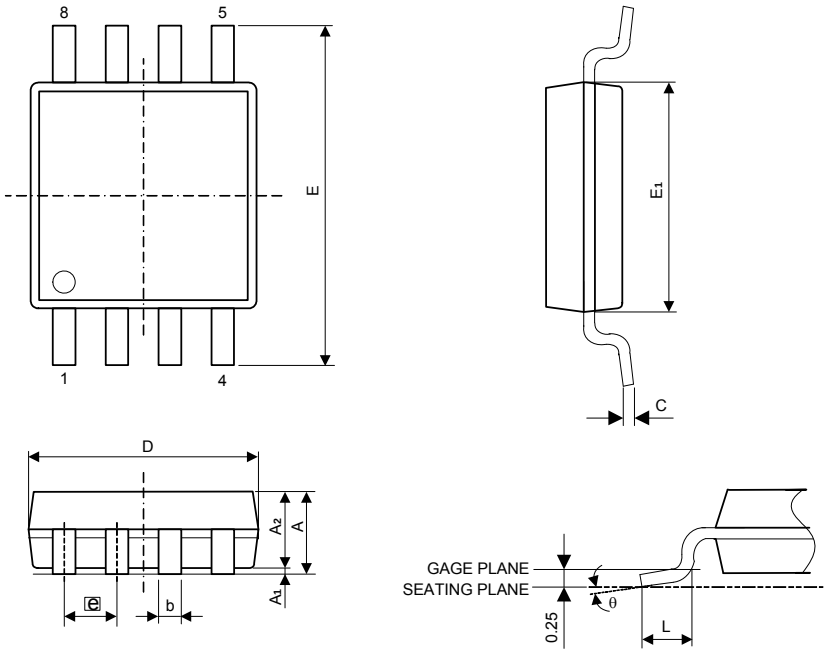
Notes:

1. Dimension D and E_1 do not include mold flash or protrusions.
2. Dimension B_1 does not include dambar protrusion.
3. Tolerance: ±0.010” (0.25mm) unless otherwise specified.

Package Information

SOP 8L (209mil) Outline Dimensions

unit: mm



Symbol	Dimensions in mm		
	Min	Nom	Max
A	1.75	1.95	2.16
A_1	0.05	0.15	0.25
A_2	1.70	1.80	1.91
b	0.35	0.42	0.48
C	0.19	0.20	0.25
D	5.13	5.23	5.33
E	7.70	7.90	8.10
E_1	5.18	5.28	5.38
e	1.27 BSC		
L	0.50	0.65	0.80
θ	0°	-	8°

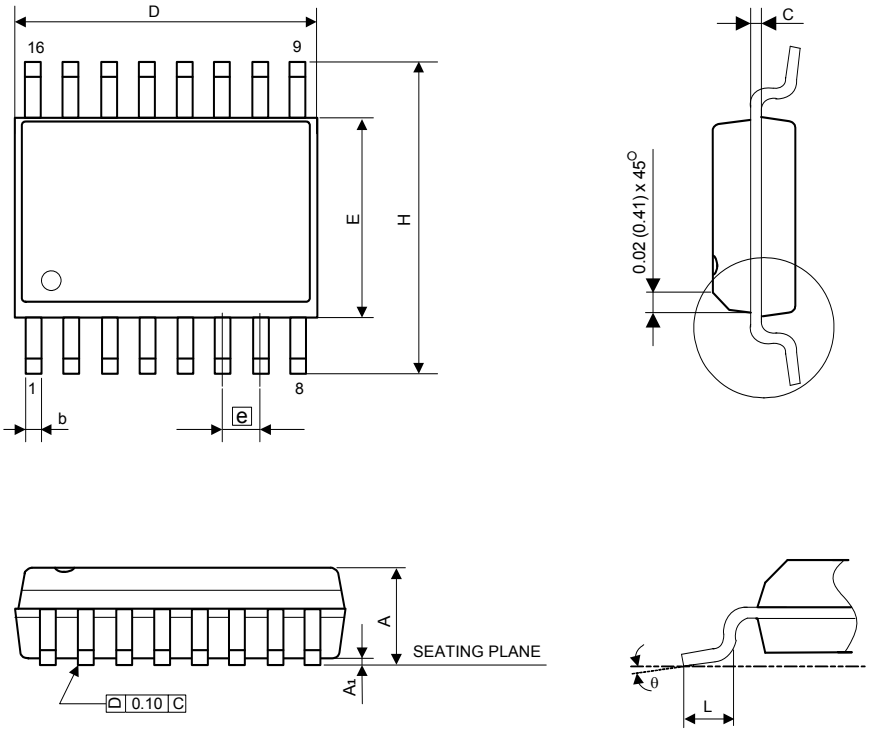
Notes:

Maximum allowable mold flash is 0.15mm at the package ends and 0.25mm between leads

Package Information

SOP 16L (300mil) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inch		Dimensions in mm	
	Min	Max	Min	Max
A	0.093	0.104	2.36	2.65
A1	0.004	0.012	0.10	0.30
b	0.016 Typ.		0.41 Typ.	
C	0.008 Typ.		0.20 Typ.	
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.39	7.60
e	0.050 Typ.		1.27 Typ.	
H	0.394	0.419	10.01	10.64
L	0.016	0.050	0.40	1.27
θ	0°	8°	0°	8°

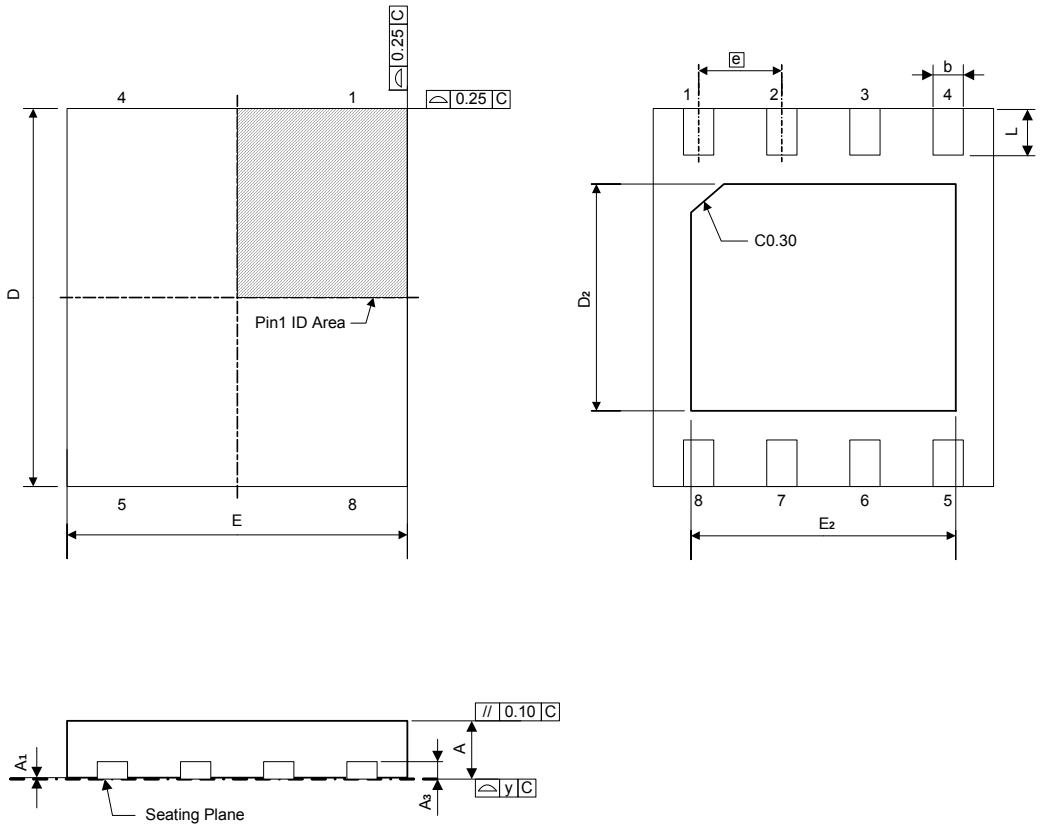
Notes:

1. Dimensions “D” does not include mold flash, protrusions or gate burrs.
2. Dimensions “E” does not include interlead flash, or protrusions.

Package Information

WSON 8L (6 X 5 X 0.8mm) Outline Dimensions

unit: mm/mil



Symbol	Dimensions in mm			Dimensions in mil		
	Min	Nom	Max	Min	Nom	Max
A	0.700	0.750	0.800	27.6	29.5	31.5
A_1	0.000	0.020	0.050	0.0	0.8	2.0
A_3	0.203 REF			8.0 REF		
b	0.350	0.400	0.480	13.8	15.8	18.9
D	5.900	6.000	6.100	232.3	236.2	240.2
D_2	3.200	3.400	3.600	126.0	133.9	141.7
E	4.900	5.000	5.100	192.9	196.9	200.8
E_2	3.800	4.000	4.200	149.6	157.5	165.4
L	0.500	0.600	0.750	19.7	23.6	29.5
e	1.270 BSC			50.0 BSC		
y	0	-	0.080	0	-	3.2

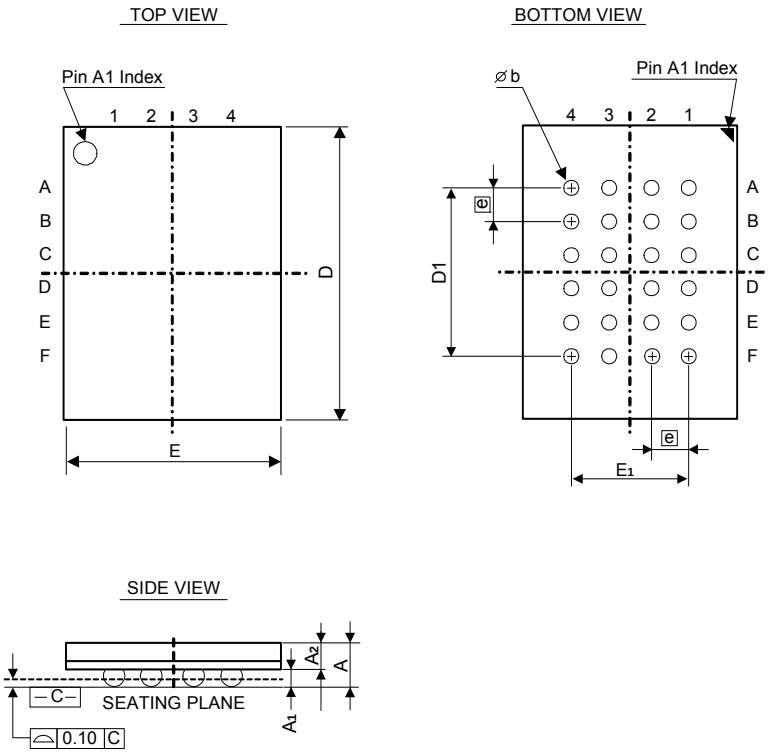
Note:

1. Controlling dimension: millimeters
2. Leadframe thickness is 0.203mm (8mil)

Package Information

Mini BGA 24L (6 X 8mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.047	-	-	1.20
A_1	0.010	0.012	0.014	0.25	0.30	0.35
A_2	-	0.033	-	-	0.85	-
b	0.014	0.016	0.018	0.35	0.40	0.45
D	0.313	0.315	0.317	7.95	8.00	8.05
D_1	0.197 BSC			5.00 BSC		
e	0.039 BSC			1.00 BSC		
E	0.234	0.236	0.238	5.95	6.00	6.05
E_1	0.118 BSC			3.00 BSC		