*Preliminary* *256K X 16 BIT LOW VOLTAGE CMOS SRAM*

## Document Title

**256K X 16 BIT LOW VOLTAGE CMOS SRAM**

## Revision History

| Rev. No. | History | Issue Date | Remark |
|---|---|---|---|
| 0.0 | Initial issue | October 21, 2020 | Preliminary |

# LP62S16256I-I Series

## Preliminary — 256K X 16 BIT LOW VOLTAGE CMOS SRAM

### Features

- Operating voltage: 2.7V to 3.6V
- Access times: 45ns/ 55ns/ 70ns (max.)
- Current:
  Very low power version: Operating: 30mA (max.)
  Standby: 8μA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 1.5V (min.)
- Available in 44-pin TSOP and 48-ball CSP (6×8mm) packages
- All Pb-free (Lead-free) products are RoHS2.0 compliant

### General Description

The LP62S16256I-I is a low operating current 4,194,304-bit static random access memory organized as 262,144 words by 16 bits and operates on low power voltage from 2.7V to 3.6V. It is built using AMIC's high performance CMOS process.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.
The chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.
Data retention is guaranteed at a power supply voltage as low as 1.5V.

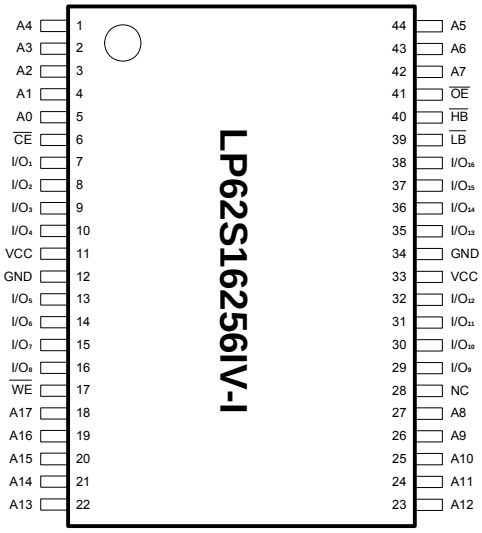
### Product Family

| Product Family | Operating Temperature | VCC Range | Speed | Power Dissipation | | Package Type |
|---|---|---|---|---|---|---|
| | | | | Data Retention ($I_{CCDR}$, Typ.) | Standby ($I_{SB1}$, Typ.) | |
| LP62S16256I-I | -40°C ~ +85°C | 2.7V~3.6V | 45ns/55ns/70ns | 2μA | 2μA | 44L TSOP<br>48B CSP |

1. Typical values are measured at VCC = 3.0V, $T_A$ = 25°C and not 100% tested.
2. Data retention current VCC = 1.5V.

### Pin Configurations

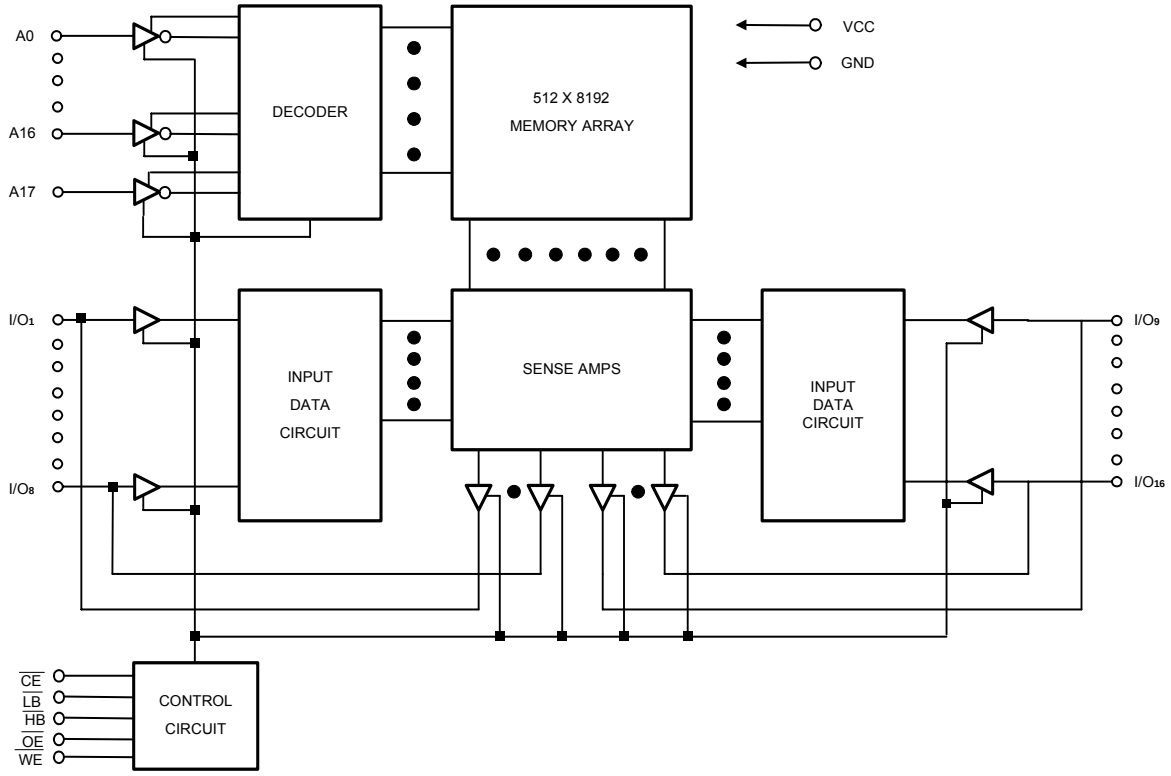
■ **TSOP**




■ **CSP (Chip Size Package)**
**48-pin Top View**

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | $\overline{LB}$ | $\overline{OE}$ | A0 | A1 | A2 | NC |
| B | $I/O_9$ | $\overline{HB}$ | A3 | A4 | $\overline{CE}$ | $I/O_1$ |
| C | $I/O_{10}$ | $I/O_{11}$ | A5 | A6 | $I/O_2$ | $I/O_3$ |
| D | GND | $I/O_{12}$ | A17 | A7 | $I/O_4$ | VCC |
| E | VCC | $I/O_{13}$ | NC | A16 | $I/O_5$ | GND |
| F | $I/O_{15}$ | $I/O_{14}$ | A14 | A15 | $I/O_6$ | $I/O_7$ |
| G | $I/O_{16}$ | NC | A12 | A13 | $\overline{WE}$ | $I/O_8$ |
| H | NC | A8 | A9 | A10 | A11 | NC |

## Block Diagram




## Pin Descriptions - TSOP

| Pin No. | Symbol | Description |
|---|---|---|
| 1 - 5, 18 - 27, 42 - 44 | A0 - A17 | Address Inputs |
| 6 | $\overline{CE}$ | Chip Enable Input |
| 7 - 10, 13 - 16, 29 - 32, 35 - 38 | $I/O_1$ - $I/O_{16}$ | Data Inputs/Outputs |
| 17 | $\overline{WE}$ | Write Enable Input |
| 39 | $\overline{LB}$ | Lower Byte Enable Input ($I/O_1$ to $I/O_8$) |
| 40 | $\overline{HB}$ | Higher Byte Enable Input ($I/O_9$ to $I/O_{16}$) |
| 41 | $\overline{OE}$ | Output Enable Input |
| 11, 33 | VCC | Power |
| 12, 34 | GND | Ground |
| 28 | NC | No Connection |

### Pin Description - CSP

| Symbol | Description | Symbol | Description |
|---|---|---|---|
| A0 - A17 | Address Inputs | $\overline{HB}$ | Higher Byte Enable Input ($I/O_9$ - $I/O_{16}$) |
| $\overline{CE}$ | Chip Enable | $\overline{OE}$ | Output Enable |
| $I/O_1$ - $I/O_{16}$ | Data Input/Output | VCC | Power Supply |
| $\overline{WE}$ | Write Enable Input | GND | Ground |
| $\overline{LB}$ | Byte Enable Input ($I/O_1$ - $I/O_8$) | NC | No Connection |

### Recommended DC Operating Conditions

($T_A$ = -40°C to + 85°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VCC | Supply Voltage | 2.7 | 3 | 3.6 | V |
| GND | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | - | VCC + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | -0.3 | - | +0.8 | V |
| $C_L$ | Output Load | - | - | 30 | pF |
| TTL | Output Load | - | - | 1 | - |

### Absolute Maximum Ratings*

VCC to GND ..... -0.5V to +4.0V
IN, IN/OUT Volt to GND..... -0.5V to VCC + 0.5V
Operating Temperature, Topr .....-40°C to +85°C
Storage Temperature, Tstg.....-55°C to +125°C
Power Dissipation, $P_T$.....1.0W

### *Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

### DC Electrical Characteristics ($T_A$ = -40°C to + 85°C, VCC = 2.7V to 3.6V, GND = 0V)

| Symbol | Parameter | LP62S16256I-45LLI / 55LLI / 70LLI | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $\lvert I_{LI} \rvert$ | Input Leakage Current | - | - | 1 | μA | $V_{IN}$ = GND to VCC |
| $\lvert I_{LO} \rvert$ | Output Leakage Current | - | - | 1 | μA | $\overline{CE}$ = $V_{IH}$<br>$\overline{HB}$ = $V_{IH}$ or $\overline{OE}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IH}$<br>$V_{I/O}$ = GND to VCC |
| $I_{CC}$ | Active Power Supply Current | - | - | 10 | mA | $\overline{CE}$ = $V_{IL}$, $I_{I/O}$ = 0mA |
| $I_{CC1}$ | Dynamic Operating Current | - | - | 30 | mA | Min. Cycle, Duty = 100%<br>$\overline{CE}$ = $V_I$, $I_{I/O}$ = 0mA |
| $I_{SB}$ | Standby Current | - | - | 0.3 | mA | $\overline{CE}$ = $V_{IH}$<br>VCC ≤ 3.3V |
| $I_{SB1}$ | | - | 2 | 8 | μA | $\overline{CE}$ ≥ VCC - 0.2V,<br>VCC ≤ 3.3V<br>$V_{IN}$ ≥ 0V |
| $V_{OL}$ | Output Low Voltage | - | - | 0.4 | V | $I_{OL}$ = 2.1 mA |
| $V_{OH}$ | Output High Voltage | 2.2 | - | - | V | $I_{OH}$ = -1.0 mA |

**Truth Table**

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{HB}$ | I/O1 to I/O8 Mode | I/O9 to I/O16 Mode | VCC Current |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | Not selected | Not selected | $I_{SB1}$, $I_{SB}$ |
| L | L | H | L | L | Read | Read | $I_{CC1}$, $I_{CC2}$, $I_{CC}$ |
| | | | L | H | Read | High - Z | $I_{CC1}$, $I_{CC2}$, $I_{CC}$ |
| | | | H | L | High - Z | Read | $I_{CC1}$, $I_{CC2}$, $I_{CC}$ |
| L | X | L | L | L | Write | Write | $I_{CC1}$, $I_{CC2}$, $I_{CC}$ |
| | | | L | H | Write | High - Z | $I_{CC1}$, $I_{CC2}$, $I_{CC}$ |
| | | | H | L | High - Z | Write | $I_{CC1}$, $I_{CC2}$, $I_{CC}$ |
| L | H | H | L | X | High - Z | High - Z | $I_{CC1}$, $I_{CC2}$, $I_{CC}$ |
| L | H | H | X | L | High - Z | High - Z | $I_{CC1}$, $I_{CC2}$, $I_{CC}$ |

Note: X = H or L

**Capacitance** ($T_A$ = 25°C, f = 1.0MHz)

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| $C_{IN}$* | Input Capacitance | | 6 | pF | $V_{IN}$ = 0V |
| $C_{I/O}$* | Input/Output Capacitance | | 8 | pF | $V_{I/O}$ = 0V |

* These parameters are sampled and not 100% tested.

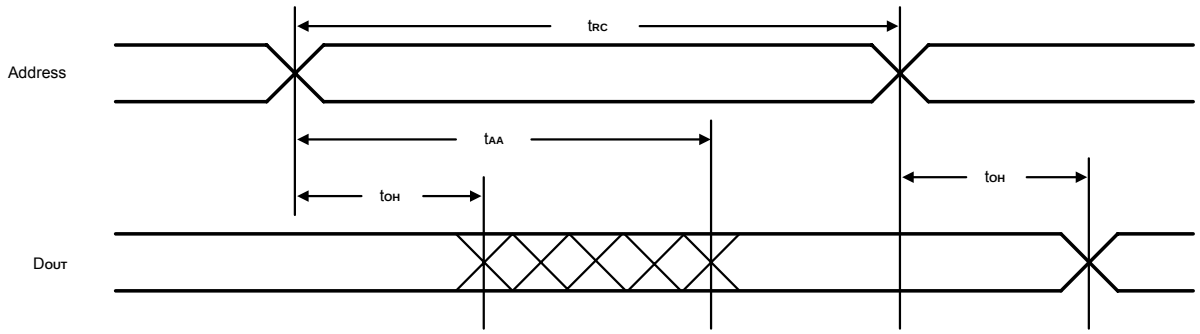
**AC Characteristics** ($T_A$ = -40°C to +85°C, VCC = 2.7V to 3.6V)

| Symbol | Parameter | LP62S16256I-45LLI | | LP62S16256I-55LLI | | LP62S16256I-70LLI | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 45 | - | 55 | - | 70 | - | ns |
| $t_{AA}$ | Address Access Time | - | 45 | - | 55 | - | 70 | ns |
| $t_{ACE}$ | Chip Enable Access Time | - | 45 | - | 55 | - | 70 | ns |
| $t_{BE}$ | Byte Enable Access Time | - | 45 | - | 55 | - | 70 | ns |
| $t_{OE}$ | Output Enable to Output Valid | - | 22 | - | 25 | - | 35 | ns |
| $t_{CLZ}$ | Chip Enable to Output in Low Z | 10 | - | 10 | - | 10 | - | ns |
| $t_{BLZ}$ | Byte Enable to Output in Low Z | 5 | - | 5 | - | 5 | - | ns |
| $t_{OLZ}$ | Output Enable to Output in Low Z | 5 | - | 5 | - | 5 | - | ns |
| $t_{CHZ}$ | Chip Disable to Output in High Z | - | 18 | - | 20 | - | 25 | ns |
| $t_{BHZ}$ | Byte Disable to Output in High Z | - | 18 | - | 20 | - | 25 | ns |
| $t_{OHZ}$ | Output Disable to Output in High Z | - | 18 | - | 20 | - | 25 | ns |
| $t_{OH}$ | Output Hold from Address Change | 10 | - | 10 | - | 10 | - | ns |
| Write Cycle | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 45 | - | 55 | - | 70 | - | ns |
| $t_{CW}$ | Chip Enable to End of Write | 35 | - | 45 | - | 60 | - | ns |
| $t_{BW}$ | Byte Enable to End of Write | 35 | - | 45 | - | 60 | - | ns |
| $t_{AS}$ | Address Setup Time | 0 | - | 0 | - | 0 | - | ns |
| $t_{AW}$ | Address Valid to End of Write | 35 | - | 45 | - | 60 | - | ns |
| $t_{WP}$ | Write Pulse Width | 35 | - | 40 | - | 50 | - | ns |
| $t_{WR}$ | Write Recovery Time | 0 | - | 0 | - | 0 | - | ns |
| $t_{WHZ}$ | Write to Output in High Z | - | 18 | - | 20 | - | 25 | ns |
| $t_{DW}$ | Data to Write Time Overlap | 25 | - | 25 | - | 30 | - | ns |
| $t_{DH}$ | Data Hold from Write Time | 0 | - | 0 | - | 0 | - | ns |
| $t_{OW}$ | Output Active from End of Write | 5 | - | 5 | - | 5 | - | ns |

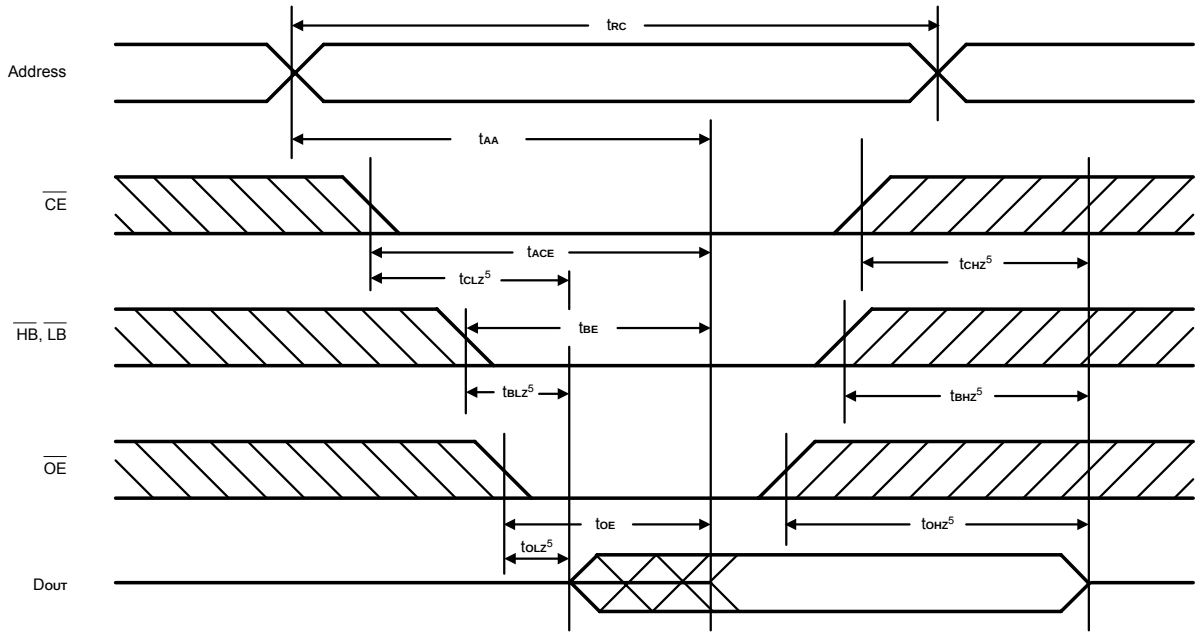
Note: $t_{CHZ}$, $t_{BHZ}$ and $t_{OHZ}$ and $t_{WHZ}$ are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

## Timing Waveforms

### Read Cycle 1 (1, 2, 4)



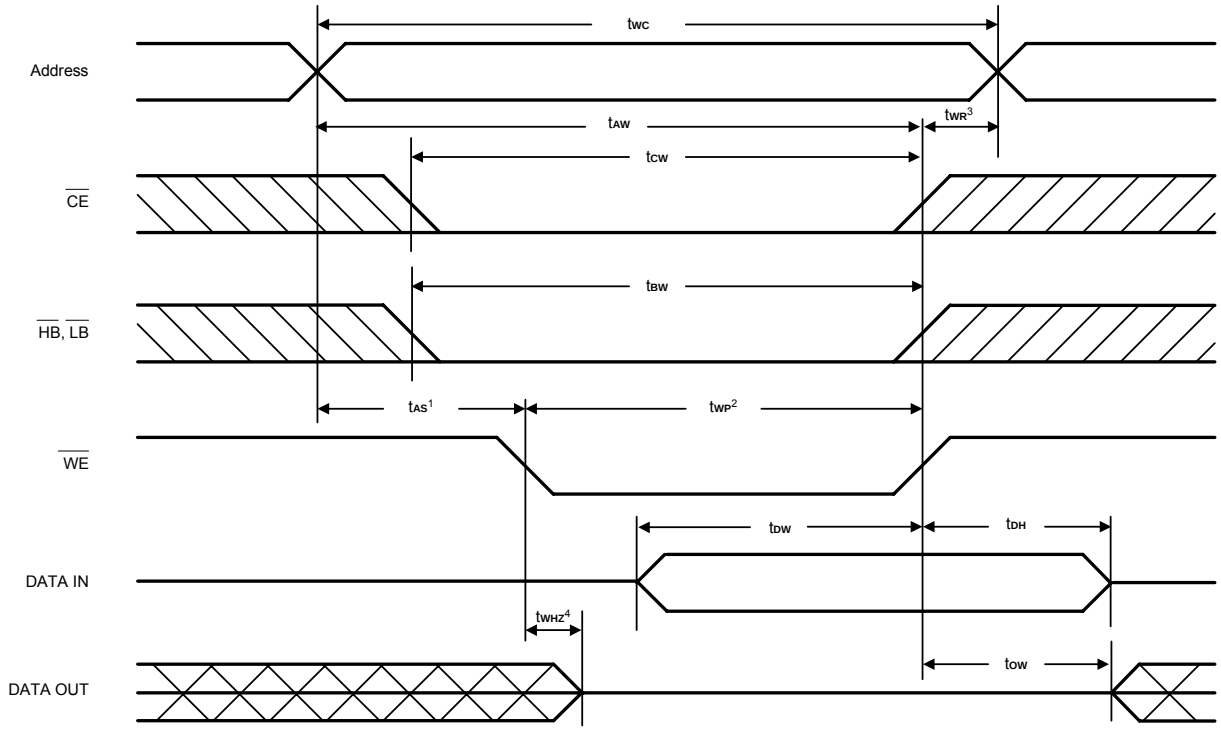

### Read Cycle 2 (1, 2, 3)



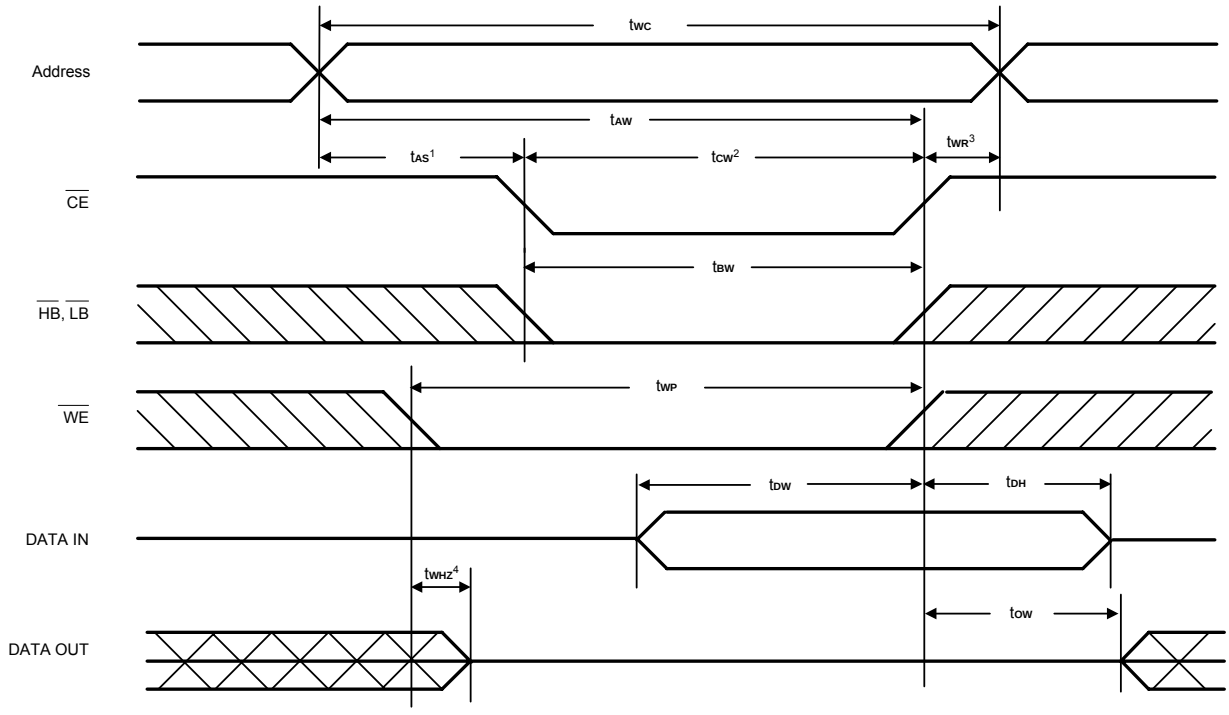

Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE}$ = $V_{IL}$, $\overline{HB}$ = $V_{IL}$ and, or $\overline{LB}$ = $V_{IL}$.
3. Address valid prior to or coincident with $\overline{CE}$ and ($\overline{HB}$ and, or $\overline{LB}$) transition low.
4. $\overline{OE}$ = $V_{IL}$.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

## Timing Waveforms (continued)

### Write Cycle 1
### (Write Enable Controlled)

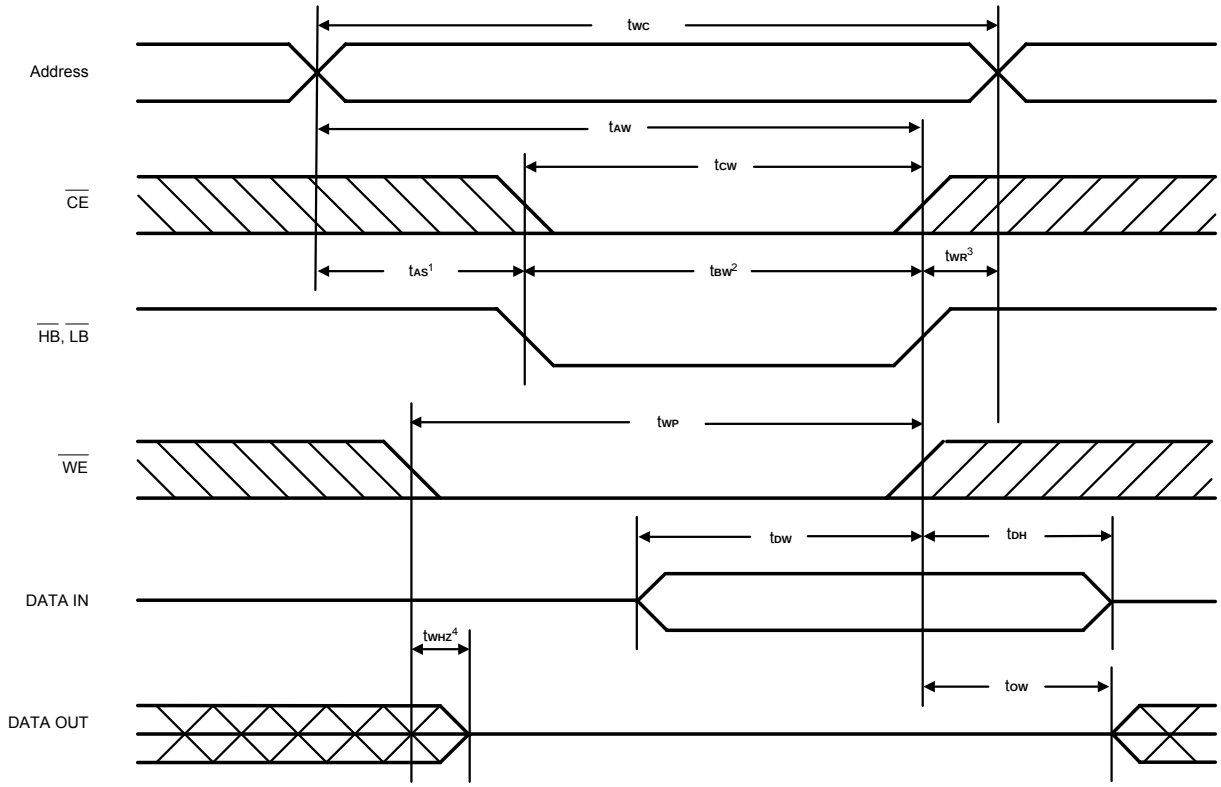



### Write Cycle 2
### (Chip Enable Controlled)



## Timing Waveforms (continued)

### Write Cycle 3
### (Byte Enable Controlled)




Notes: 1. $t_{AS}$ is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap ($t_{WP}$, $t_{BW}$) of a low $\overline{CE}$ , $\overline{WE}$ and ($\overline{HB}$ and , or $\overline{LB}$ ).
3. $t_{WR}$ is measured from the earliest of $\overline{CE}$ or $\overline{WE}$ or ($\overline{HB}$ and , or $\overline{LB}$ ) going high to the end of the Write cycle.
4. $\overline{OE}$ level is high or low.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

### AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | 0.4V to 2.4V |
| Input Rise And Fall Time | 5ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See Figures 1 and 2 |

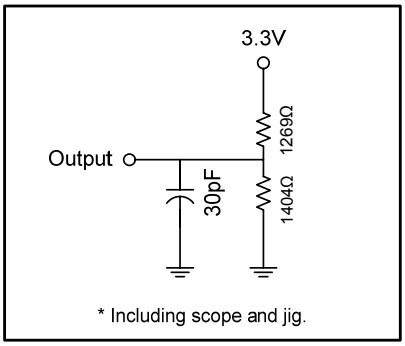



**Figure 1**

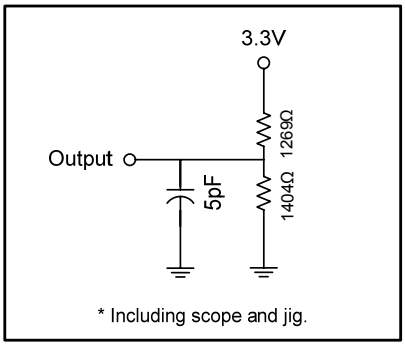
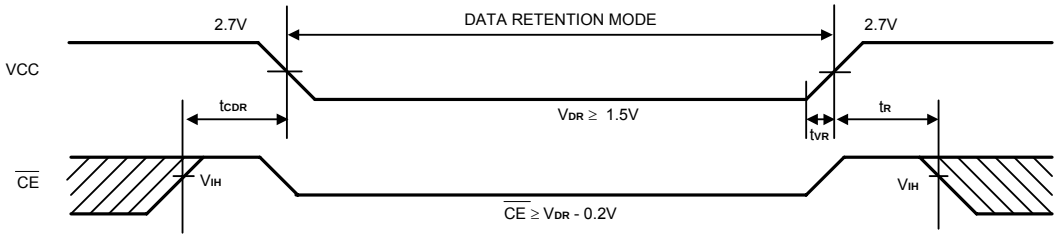



**Figure 2**

### Data Retention Characteristics ($T_A$ = -40°C to 85°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| $V_{DR}$ | VCC for Data Retention | 1.5 | - | 3.6 | V | $\overline{CE} \geq$ VCC - 0.2V |
| $I_{CCDR}$ | Data Retention Current | - | 2.0 | 6 | µA | VCC = 2.0V,<br>$\overline{CE} \geq$ VCC – 0.2V<br>$V_{IN} \geq$ 0V |
| $t_{CDR}$ | Chip Disable to Data Retention Time | 0 | - | - | ns | See Retention Waveform |
| $t_R$ | Operation Recovery Time | $t_{RC}$ | - | - | ns | |
| $t_{VR}$ | VCC Rising Time from Data Retention Voltage to Operating Voltage | 5 | - | - | ms | |

### Low VCC Data Retention Waveform

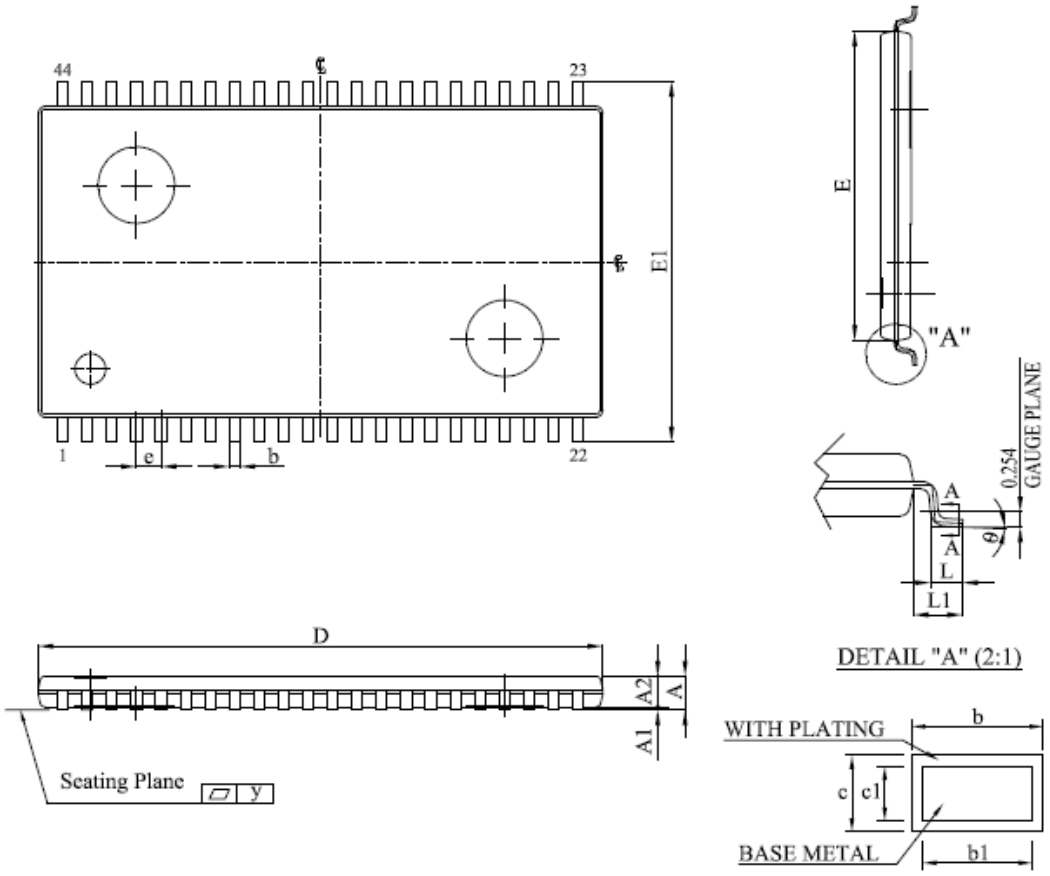



### Ordering Information

| Part No. | Access Time (ns) | Operating Current Max. (mA) | Standby Current Max. (μA) | Package |
|---|---|---|---|---|
| LP62S16256IV-45LLIF | 45 | 30 | 8 | 44L Pb-Free TSOP |
| LP62S16256IU-45LLIF | | | | 48L Pb-Free CSP |
| LP62S16256IV-55LLIF | 55 | 30 | 8 | 44L Pb-Free TSOP |
| LP62S16256IU-55LLIF | | | | 48L Pb-Free CSP |
| LP62S16256IV-70LLIF | 70 | 30 | 8 | 44L Pb-Free TSOP |
| LP62S16256IU-70LLIF | | | | 48L Pb-Free CSP |

**Package Information**

**TSOP 44L TYPE II Outline Dimensions** unit: mm/inches

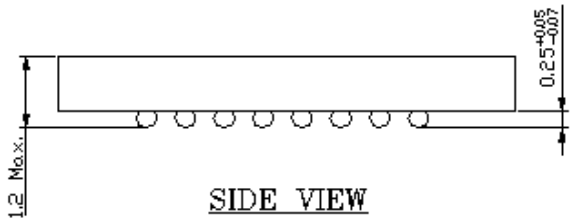



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

| SYMBOL / UNIT | | A | A1 | A2 | b | b1 | c | c1 | D | E | E1 | e | L | L1 | y | Θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | 1.00 | 0.05 | 0.95 | 0.30 | 0.30 | 0.12 | 0.12 | 18.31 | 10.06 | 11.56 | 0.70 | 0.40 | 0.70 | – | 0° |
| | Nom. | 1.10 | 0.10 | 1.00 | – | – | – | – | 18.41 | 10.16 | 11.76 | 0.80 | 0.50 | 0.80 | – | – |
| | Max. | 1.20 | 0.15 | 1.05 | 0.45 | 0.40 | 0.21 | 0.16 | 18.51 | 10.26 | 11.96 | 0.90 | 0.60 | 0.90 | 0.1 | 8° |
| inch | Min. | 0.0393 | 0.002 | 0.037 | 0.012 | 0.012 | 0.005 | 0.005 | 0.721 | 0.396 | 0.455 | 0.0275 | 0.0157 | 0.0275 | – | 0° |
| | Nom. | 0.0433 | 0.004 | 0.039 | – | – | – | – | 0.725 | 0.400 | 0.463 | 0.0315 | 0.0197 | 0.0315 | – | – |
| | Max. | 0.0473 | 0.006 | 0.041 | 0.018 | 0.016 | 0.008 | 0.006 | 0.729 | 0.404 | 0.471 | 0.0355 | 0.0237 | 0.0355 | 0.004 | 8° |

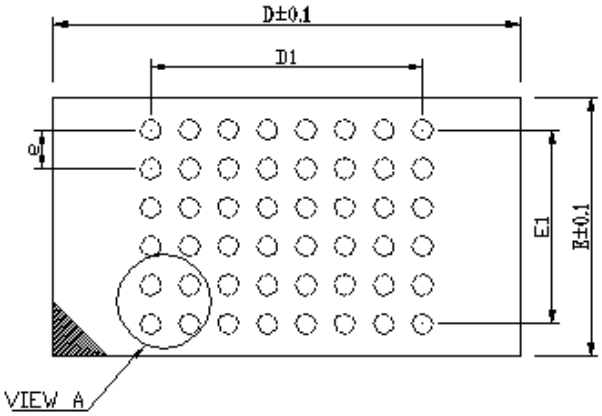
**Package Information**

**48LD CSP (6 x 8 mm) Outline Dimensions** unit: mm
**(48TFBGA)**

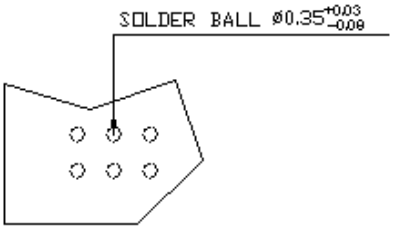



SIDE VIEW

| BALL PITCH e = 0.75 | | | | |
|---|---|---|---|---|
| D | E | N | D1 | E1 |
| 8.0 | 6.0 | 48 | 5.25 | 3.75 |




TOP VIEW




VIEW A

NOTES
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL 'N' IS THE NUMBER OF SOLDER BALLS.