Preliminary *8M BIT (512K x 16 / 1M x 8) LOW VOLTAGE CMOS SRAM*

Document Title

8M BIT (512K x 16 / 1M x 8) LOW VOLTAGE CMOS SRAM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	November 13, 2014	Preliminary
0.1	Add 48-ball CSP (8 x 10mm) package type	October 12, 2015	
0.2	Modify 48-ball CSP (8 x 10mm) outline dimensions	November 18, 2015	
0.3	Add -45 speed grade and 44-pin TSOPII package type	December 21, 2015	

AMIC

LP62S16512A Series

Preliminary 8M BIT (512K x 16 / 1M x 8) LOW VOLTAGE CMOS SRAM

Features

- Operating voltage: 2.7V to 3.6V
- Access times: 45/55/70 ns (max.)
- Current:
  Very low power version: Operating: 50mA (max.)
  Standby: 20μA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 2.0V (min.)
- Available in 48-pin TSOP (I), 44-pin TSOP(II) and 48-ball CSP (6 x 8 mm) / (8 x 10mm) packages
- All Pb-free (Lead-free) products are RoHS2.0 compliant
- The TSOP (I) package configurable as 512K x 16 or 1M x 8 Static RAM
  - $\overline{BYTE}$ fixed to HIGH, $\overline{LB}$ controlled I/O_0 - I/O_7, $\overline{HB}$ controlled I/O_8 - I/O_{15}
  - $\overline{BYTE}$ fixed to LOW, I/O_{15} used as address pin, while I/O_8 - I/O_{14} pins not used

General Description

The LP62S16512A is a low operating current 8,388,608-bit static random access memory organized as 524,288 words by 16 bits and operates on low power voltage from 2.7V to 3.6V. It is built using AMIC's high performance CMOS process.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.
Two chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.
Data retention is guaranteed at a power supply voltage as low as 2.0V.

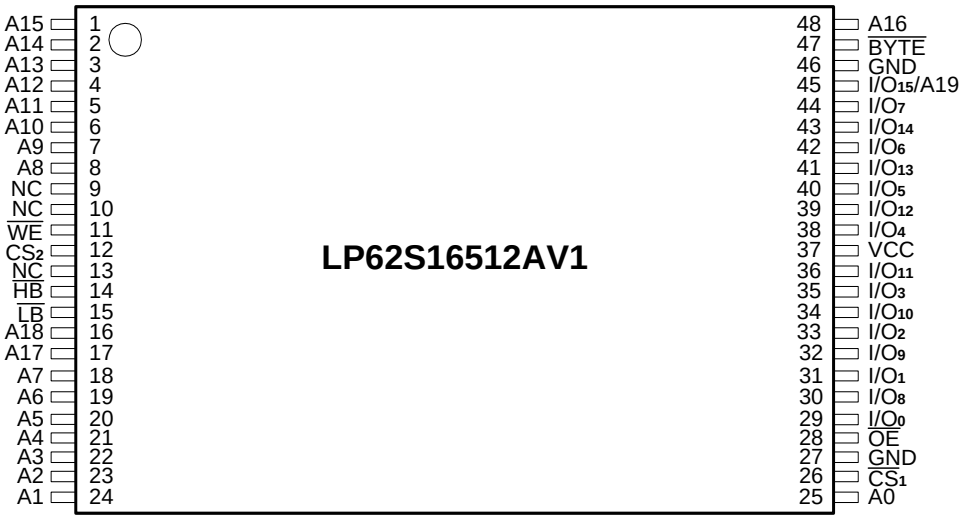
Product Family

Product Family	Operating Temperature	VCC Range	Speed	Power Dissipation			Package Type
				Data Retention (I_{CCDR}, Typ.)	Standby (I_{SB1}, Typ.)	Operating (I_{CC2}, Typ.)	
LP62S16512A	0°C ~ +70°C	2.7V~3.6V	45ns / 55ns / 70ns	0.3μA	0.5μA	4mA	48-pin TSOP (I) 44-pin TSOP (II) 48-ball CSP
LP62S16512A(I)	-40°C ~ +85°C	2.7V~3.6V	45ns / 55ns / 70ns	0.3μA	0.5μA	4mA	48-pin TSOP (I) 44-pin TSOP (II) 48-ball CSP

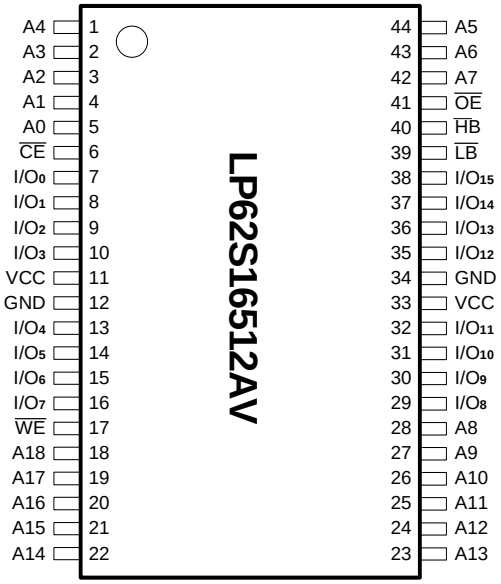
1. Typical values are measured at VCC = 3.0V, T_A = 25°C and not 100% tested.
2. Data retention current VCC = 2.0V.

Pin Configurations

■ TSOP (I)



■ TSOP (II)



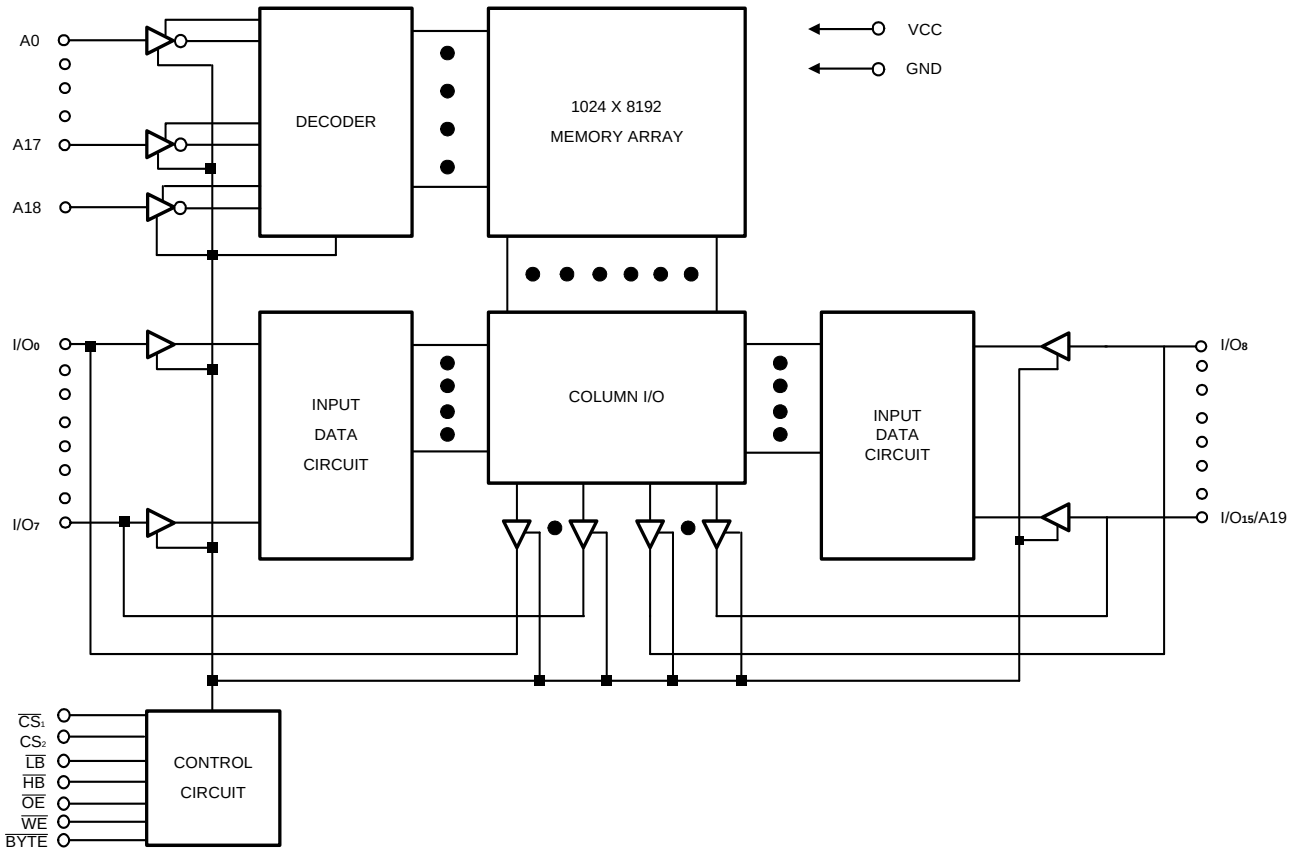
■ CSP (Chip Size Package) 48-pin Top View

	1	2	3	4	5	6
A	LB	OE	A0	A1	A2	CS2
B	I/O8	HB	A3	A4	CS1	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	GND	I/O11	A17	A7	I/O3	VCC
E	VCC	I/O12	NC	A16	I/O4	GND
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	NC	A12	A13	WE	I/O7
H	A18	A8	A9	A10	A11	NC

Note:

The pin in the 48-pin TSOP (I) package must be tied HIGH to use the device as a 512K x 16 SRAM. The 48-pin TSOP (I) package can also be used as a 1M x 8 SRAM by tied the signal LOW. In the 1M x 8 configuration, pin 45 is A19, while, and I/O8 to I/O14 pins are not used (NC).

Block Diagram



Pin Descriptions

Symbol	Description	Symbol	Description
A0 - A18	Address Inputs (Word Mode)	$\overline{HB}$	Higher Byte Enable Input (I/O_8 - I/O_{15})
A0 - A19	Address Inputs (Byte Mode)	$\overline{BYTE}$	Byte Enable
$\overline{CS_1}$, CS_2	Chip Enable	$\overline{OE}$	Output Enable
I/O_0 - I/O_{15}	Data Input/Output	VCC	Power Supply
$\overline{WE}$	Write Enable Input	GND	Ground
$\overline{LB}$	Byte Enable Input (I/O_0 - I/O_7)	NC	No Connection

Recommended DC Operating Conditions

(T_A = 0°C to +70°C or -40°C to +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	+0.6	V
C_L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND ..... -0.5V to +4.0V
IN, IN/OUT Volt to GND..... -0.5V to VCC + 0.5V
Operating Temperature, Topr .....
.....0°C to +70°C or -40°C to +85°C
Storage Temperature, Tstg.....-55°C to +125°C
Power Dissipation, P_T..... 0.7W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to +70°C or -40°C to +85°C, VCC = 2.7V to 3.6V, GND = 0V)

Symbol	Parameter	LP62S16512A-45/55/70LL(I)		Unit	Conditions
		Min.	Max.		
$\lvert I_{LI} \rvert$	Input Leakage Current	-	1	μA	V_{IN} = GND to VCC
$\lvert I_{LO} \rvert$	Output Leakage Current	-	1	μA	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL} or $\overline{LB}$ = $\overline{HB}$ = V_{IH} $V_{I/O}$ = GND to VCC
I_{CC}	Active Power Supply Current	-	5	mA	$\overline{CS_1}$ = V_{IL} , CS_2 = V_{IH} , $\overline{LB}$ = V_{IL} or $\overline{HB}$ = V_{IL} , $I_{I/O}$ = 0mA
I_{CC1}	Dynamic Operating Current	-	50	mA	Min. Cycle, Duty = 100%, $\overline{CS_1}$ = V_{IL} , CS_2 = V_{IH} , $\overline{LB}$ = V_{IL} or $\overline{HB}$ = V_{IL} $I_{I/O}$ = 0mA
I_{CC2}		-	8	mA	$\overline{CS_1}$ ≤ 0.2V , CS_2 ≥ VCC-0.2V , $\overline{LB}$ ≤ 0.2V or $\overline{HB}$ ≤ 0.2V f = 1MHz , $I_{I/O}$ = 0mA
I_{SB}	Standby Current	-	1	mA	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL} or $\overline{LB}$ = $\overline{HB}$ = V_{IH}
I_{SB1}		-	20	μA	$\overline{CS_1}$ ≥ VCC - 0.2V or CS_2 ≤ 0.2V or $\overline{LB}$ = $\overline{HB}$ ≥ VCC-0.2V V_{IN} ≥ VCC-0.2V or V_{IN} ≤ 0.2V
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.2	-	V	I_{OH} = -1.0 mA

Truth Table

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{HB}$	I/O_0 to I/O_7 Mode	I/O_8 to I/O_{15} Mode	VCC Current
H	X	X	X	X	X	High - Z	High - Z	I_{SB1}, I_{SB}
X	L	X	X	X	X	High - Z	High - Z	I_{SB1}, I_{SB}
X	X	X	X	H	H	High - Z	High - Z	I_{SB1}, I_{SB}
L	H	L	H	L	L	Read	Read	I_{CC1}, I_{CC2}, I_{CC}
				L	H	Read	High - Z	I_{CC1}, I_{CC2}, I_{CC}
				H	L	High - Z	Read	I_{CC1}, I_{CC2}, I_{CC}
L	H	X	L	L	L	Write	Write	I_{CC1}, I_{CC2}, I_{CC}
				L	H	Write	High - Z	I_{CC1}, I_{CC2}, I_{CC}
				H	L	High - Z	Write	I_{CC1}, I_{CC2}, I_{CC}
L	H	H	H	L	X	High - Z	High - Z	I_{CC1}, I_{CC2}, I_{CC}
L	H	H	H	X	L	High - Z	High - Z	I_{CC1}, I_{CC2}, I_{CC}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

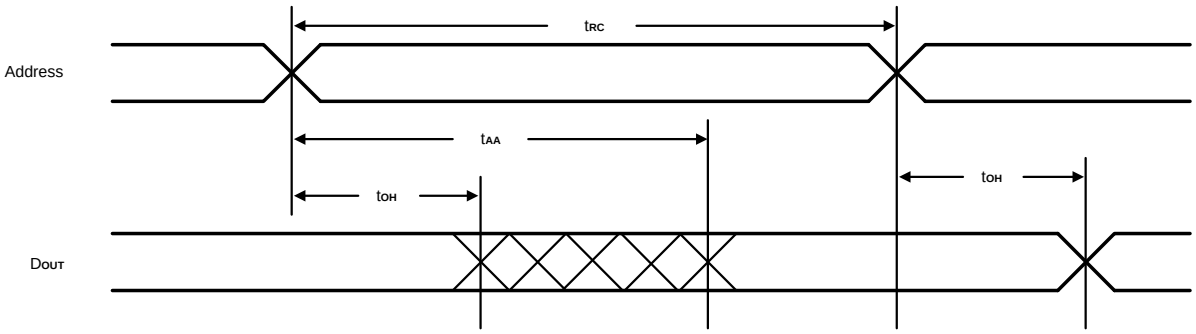
AC Characteristics (T_A = 0°C to +70°C or -40°C to +85°C, VCC = 2.7V to 3.6V)

Symbol	Parameter	LP62S16512A-45LL(I)		LP62S16512A-55LL(I)		LP62S16512A-70LL(I)		Unit
		Max.	Min.	Max.	Min.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	45	-	55	-	70	-	ns
t_{AA}	Address Access Time	-	45	-	55	-	70	ns
t_{ACS1} , t_{ACS2}	Chip Enable Access Time	-	45	-	55	-	70	ns
t_{BE}	Byte Enable Access Time	-	45	-	55	-	70	ns
t_{OE}	Output Enable to Output Valid	-	25	-	25	-	35	ns
t_{CLZ1} , t_{CLZ2}	Chip Enable to Output in Low Z	10	-	10	-	10	-	ns
t_{BLZ}	Byte Enable to Output in Low Z	10	-	10	-	10	-	ns
t_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
t_{CHZ1} , t_{CHZ2}	Chip Disable to Output in High Z	-	20	-	20	-	25	ns
t_{BHZ}	Byte Disable to Output in High Z	-	20	-	20	-	25	ns
t_{OHZ}	Output Disable to Output in High Z	-	20	-	20	-	25	ns
t_{OH}	Output Hold from Address Change	5	-	5	-	5	-	ns
Write Cycle								
t_{WC}	Write Cycle Time	45	-	55	-	70	-	ns
t_{CW1} , t_{CW2}	Chip Enable to End of Write	45	-	50	-	60	-	ns
t_{BW}	Byte Enable to End of Write	45	-	50	-	60	-	ns
t_{AS}	Address Setup Time	0	-	0	-	0	-	ns
t_{AW}	Address Valid to End of Write	45	-	50	-	60	-	ns
t_{WP}	Write Pulse Width	35	-	40	-	50	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{WHZ}	Write to Output in High Z	-	25	-	25	-	25	ns
t_{DW}	Data to Write Time Overlap	25	-	25	-	30	-	ns
t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
t_{OW}	Output Active from End of Write	5	-	5	-	5	-	ns

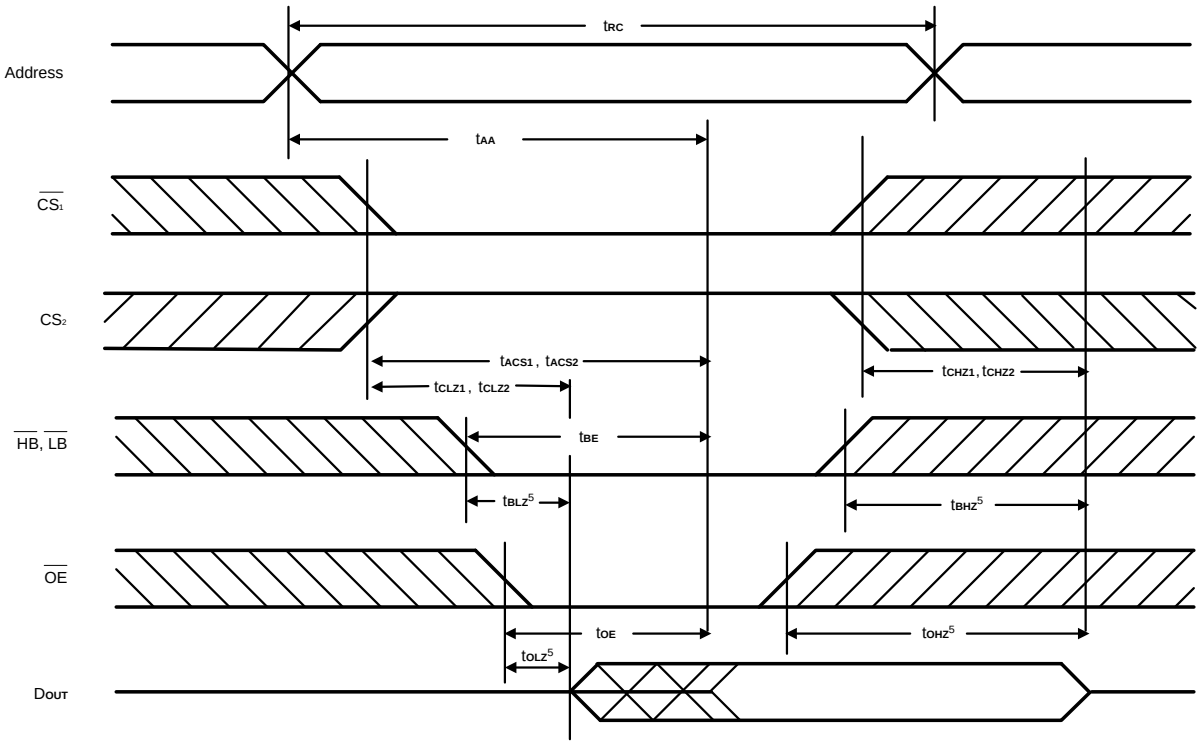
Note: t_{CLZ1} , t_{CLZ2} , t_{BLZ} , t_{OLZ} , t_{CHZ1}, t_{CHZ2} , t_{BHZ} and t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

Read Cycle 1[1, 2, 4]



Read Cycle 2[1, 2, 3]

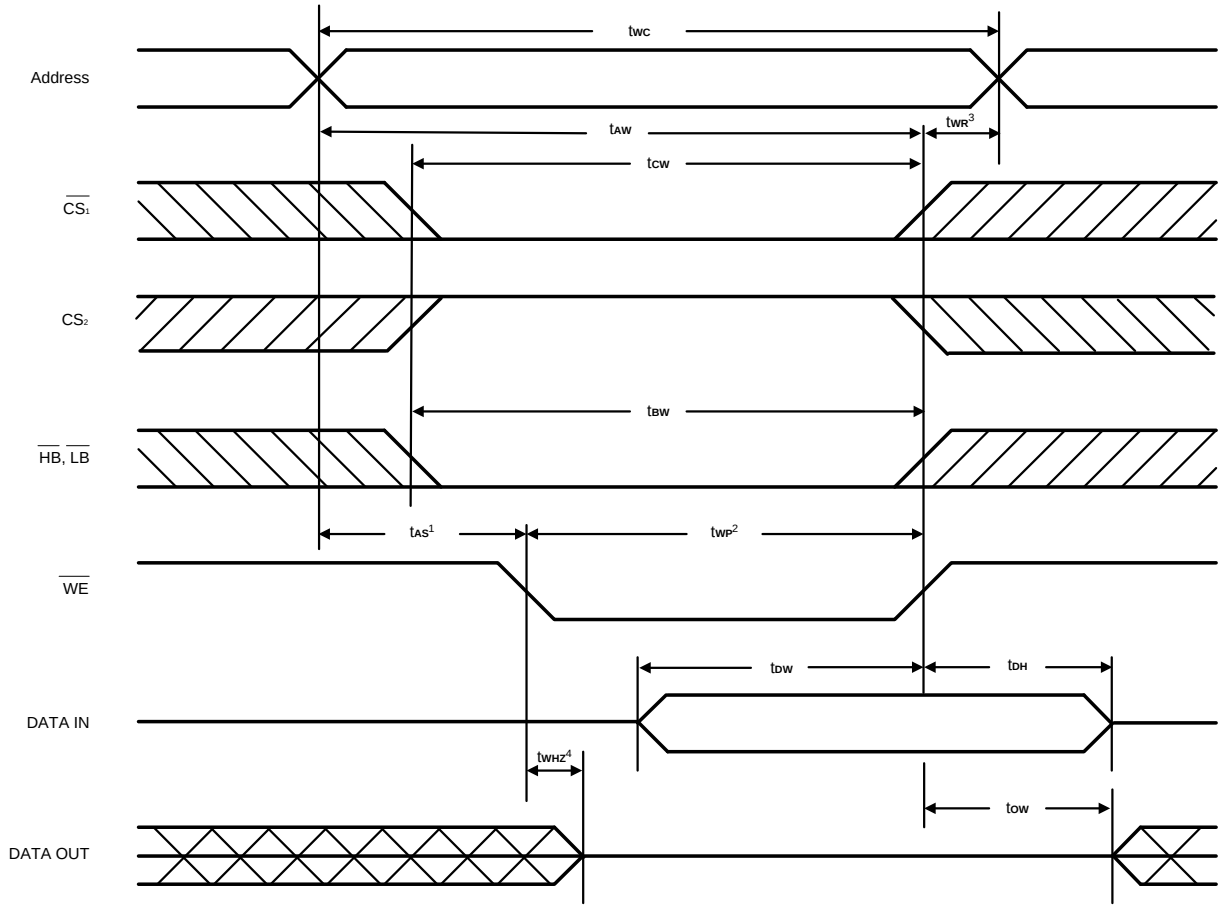


Notes: 1. $\overline{WE}$ is high for Read Cycle.

2. Device is continuously enabled $\overline{CS_1}$ = V_{IL}, or CS_2 = V_{IH} , $\overline{HB}$ = V_{IL} and, or $\overline{LB}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS_1}$ and ($\overline{HB}$ and, or $\overline{LB}$) transition low or CS_2 transition High.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

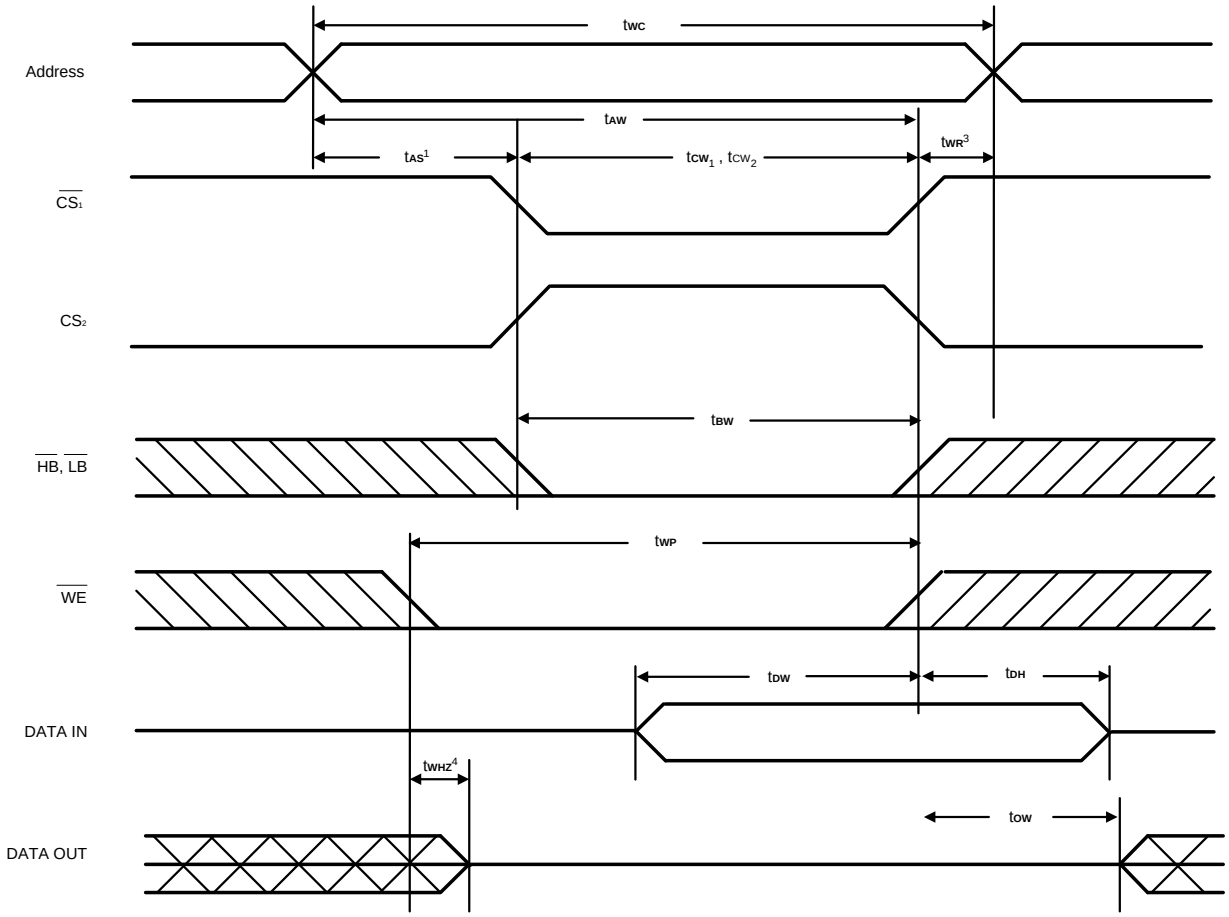
Timing Waveforms (continued)

Write Cycle 1
(Write Enable Controlled)



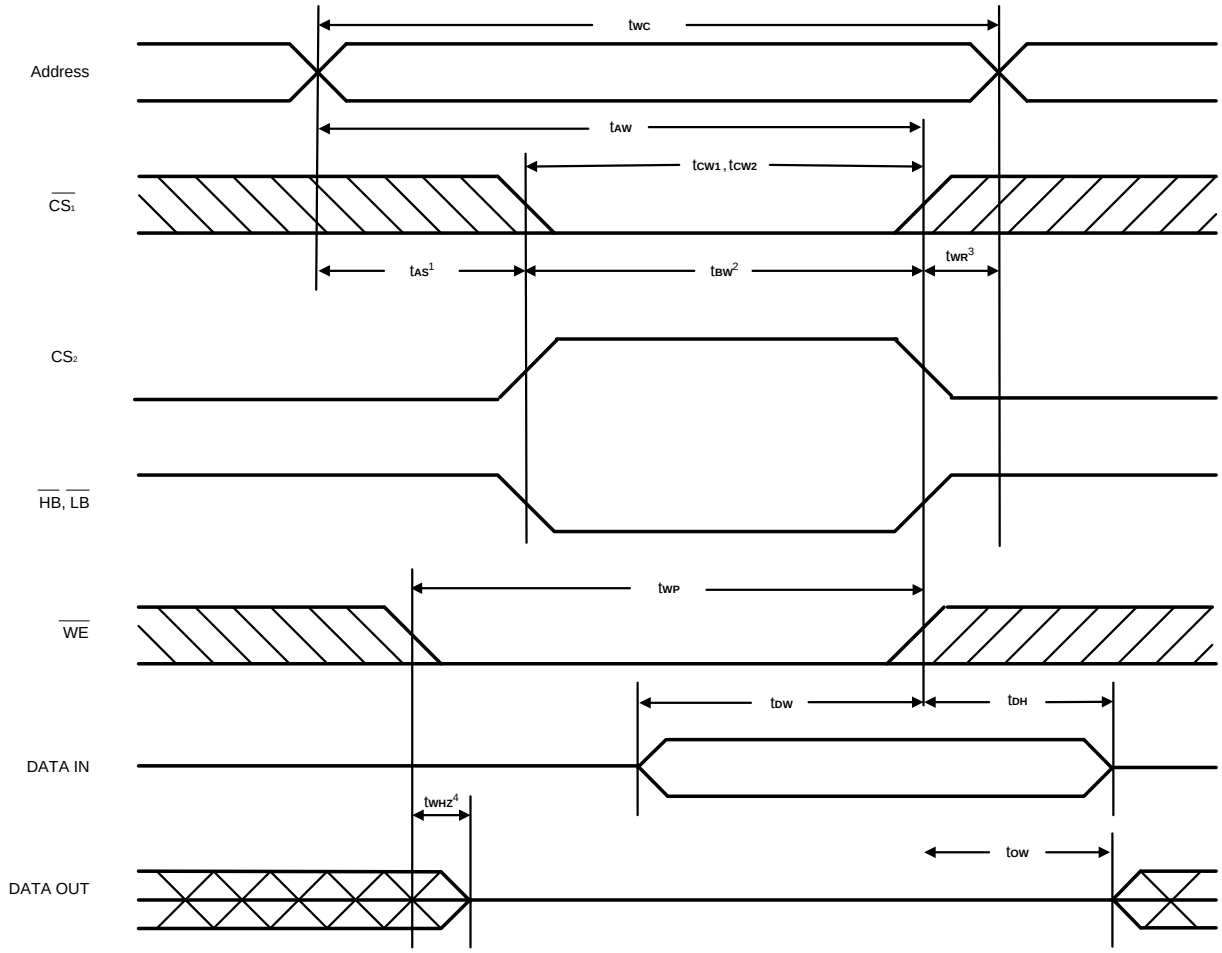
Timing Waveforms (continued)

Write Cycle 2
(Chip Enable Controlled)



Timing Waveforms (continued)

Write Cycle 3
(Byte Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.

2. A Write occurs during the overlap (t_{WP}, t_{BW}) of a low $\overline{CS_1}$, $\overline{WE}$ and ($\overline{HB}$ and , or $\overline{LB}$) or a high CS_2.
3. t_{WR} is measured from the earliest of $\overline{CS_1}$ or $\overline{WE}$ or ($\overline{HB}$ and , or $\overline{LB}$) going high or CS_2 going Low to the end of the Write cycle.
4. $\overline{OE}$ level is high or low.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 3V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

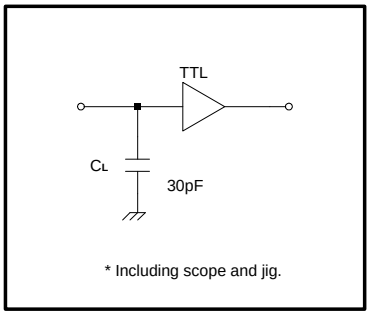


Figure 1. Output Load

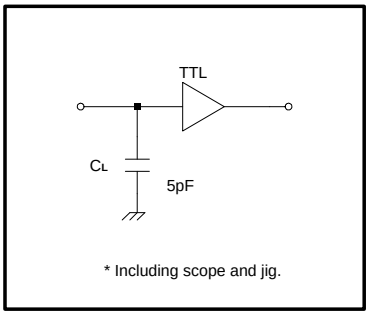


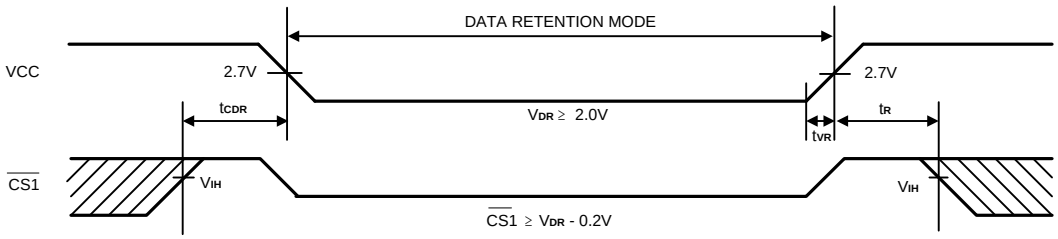
Figure 2. Output Load for t_{CLZ1}, t_{CLZ2} , t_{BHZ} , t_{BLZ} , t_{OLZ}, t_{CHZ1}, t_{CHZ2} , t_{OHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (T_A = 0°C to +70°C or -40°C to 85°C)

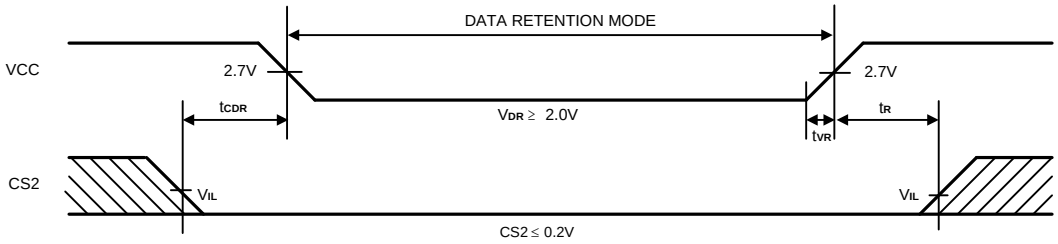
Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention	2.0	3.6	V	$\overline{CS_1} \geq$ VCC - 0.2V or $CS_2 \leq$ 0.2V or $\overline{LB}$ = $\overline{HB}$ ≥ VCC-0.2V
I_{CCDR}	Data Retention Current	-	6*	µA	VCC = 2.0V, $\overline{CS_1} \geq$ VCC - 0.2V or $CS_2 \leq$ 0.2V or $\overline{LB}$ = $\overline{HB}$ ≥ VCC-0.2V $V_{IN} \geq$ VCC-0.2V or $V_{IN} \leq$ 0.2V
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}	-	ns	
t_{VR}	VCC Rising Time from Data Retention Voltage to Operating Voltage	5	-	ms	

* LP62S16512A-45/55/70LL(I) I_{CCDR}: max. 1µA at T_A = 25°C
(3µA at T_A = 0°C to +40°C)

Low VCC Data Retention Waveform (1) ($\overline{CS1}$ Controlled)



Low VCC Data Retention Waveform (2) (CS2 Controlled)



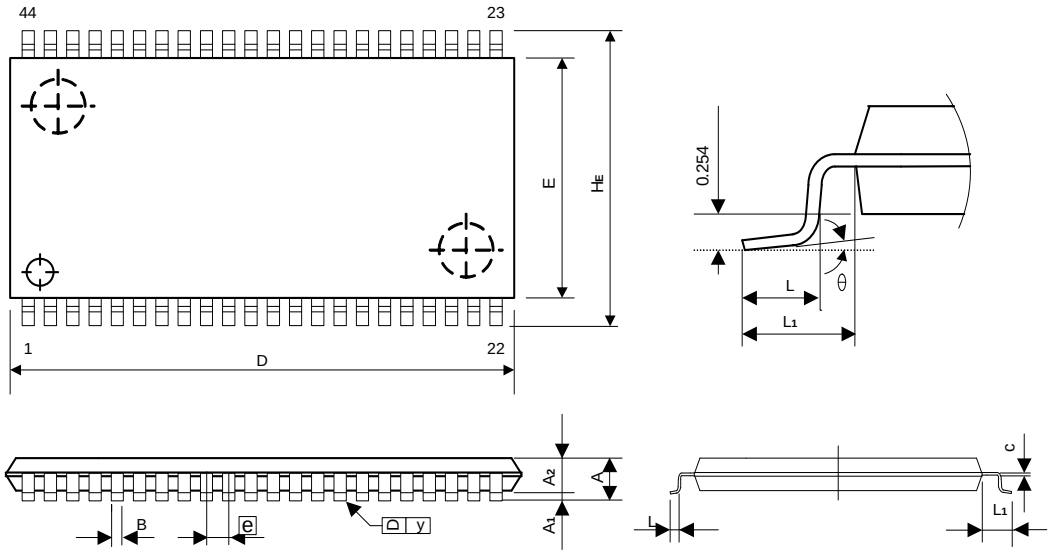
Ordering Information

Part No.	Access Time (ns)	Operating Current Max.(mA)	Standby Current Max.(uA)	Package
LP62S16512AV-45LL(I)F	45	50	20	44L Pb-Free TSOP (II)
LP62S16512AV1-45LL(I)F				48L Pb-Free TSOP (I)
LP62S16512AG-45LL(I)F				48L Pb-Free CSP (6 x 8mm)
LP62S16512AU-45LL(I)F				48L Pb-Free CSP (8 x 10mm)
LP62S16512AV-55LL(I)F	55	50	20	44L Pb-Free TSOP (II)
LP62S16512AV1-55LL(I)F				48L Pb-Free TSOP (I)
LP62S16512AG-55LL(I)F				48L Pb-Free CSP (6 x 8mm)
LP62S16512AU-55LL(I)F				48L Pb-Free CSP (8 x 10mm)
LP62S16512AV-70LL(I)F	70	50	20	44L Pb-Free TSOP (II)
LP62S16512AV1-70LL(I)F				48L Pb-Free TSOP (I)
LP62S16512AG-70LL(I)F				48L Pb-Free CSP (6 x 8mm)
LP62S16512AU-70LL(I)F				48L Pb-Free CSP (8 x 10mm)

Package Information

TSOP 44L TYPE II Outline Dimensions

unit: inches/mm



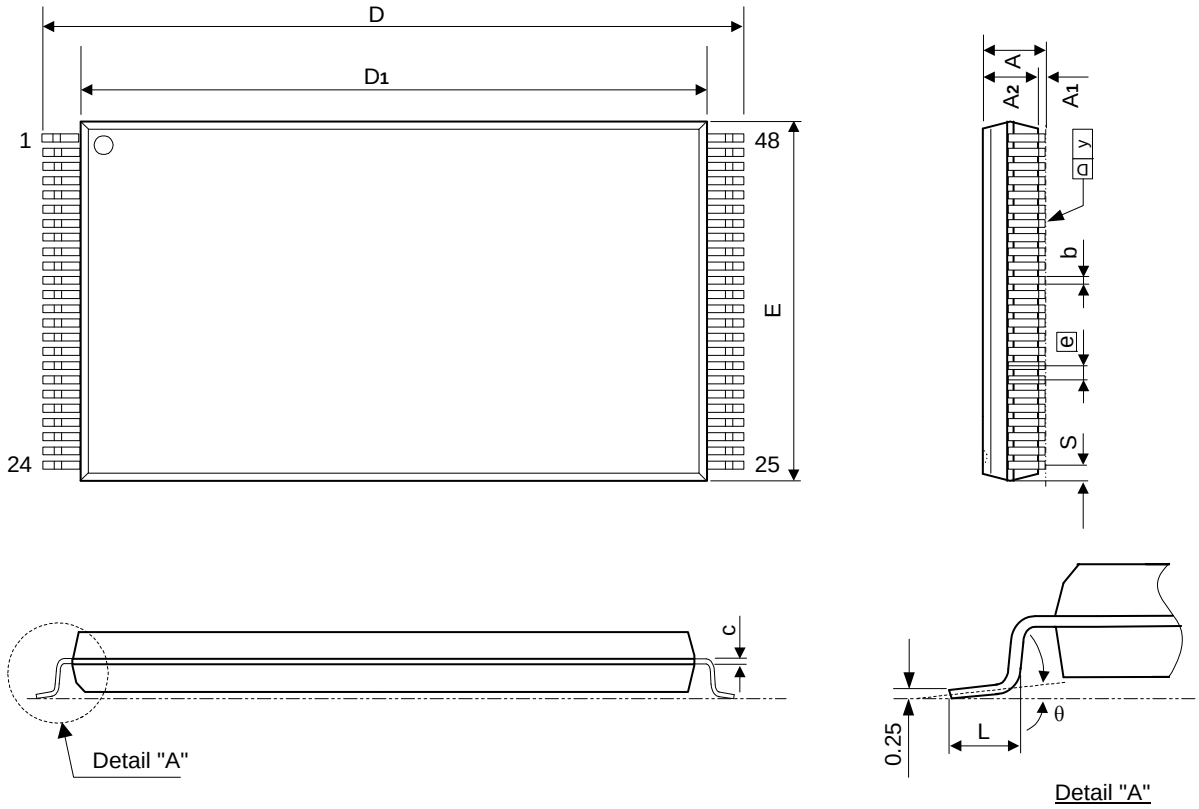
Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.039	0.043	0.047	1.00	1.10	1.20
A_1	0.002	0.004	0.006	0.05	0.10	1.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.012	-	0.018	0.30	-	0.45
c	0.005	-	0.008	0.12	-	0.21
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
e	0.027	0.031	0.035	0.70	0.80	0.90
H_E	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	0.027	0.031	0.035	0.70	0.80	0.90
y	-	-	0.004	-	-	0.10
θ	0°	-	8°	0°	-	8°

Notes:
1. Dimension D&E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.

Package Information

TSOP 48L (Type I) Outline Dimensions

unit: inches/mm



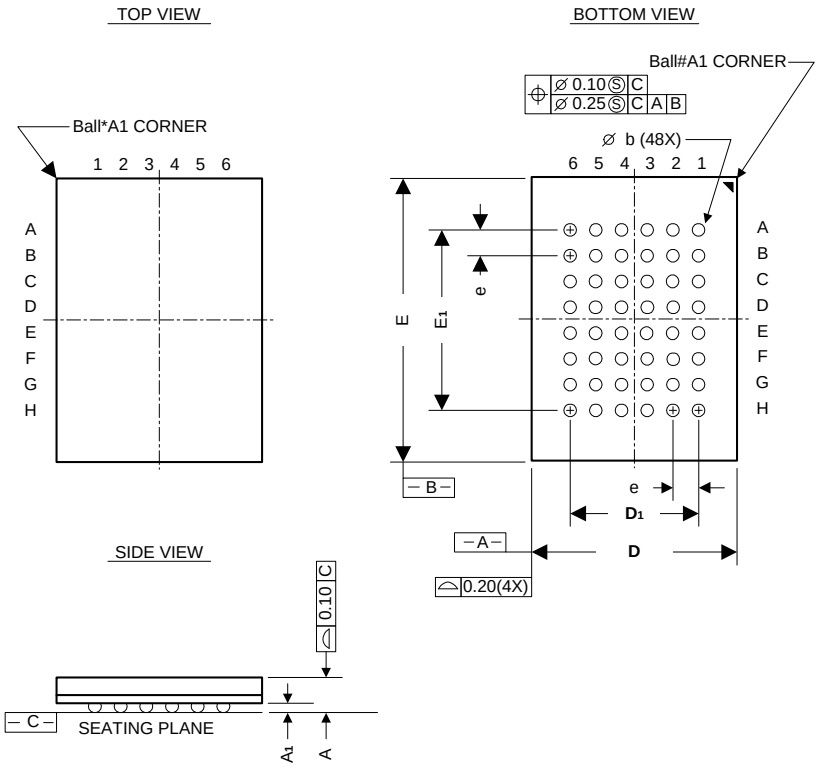
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.037	0.039	0.042	0.94	1.00	1.06
b	0.007	0.009	0.011	0.18	0.22	0.27
c	0.004	-	0.008	0.12	-	0.20
D	0.779	0.787	0.795	19.80	20.00	20.20
D1	0.720	0.724	0.728	18.30	18.40	18.50
E	-	0.472	0.476	-	12.00	12.10
e	0.020 BASIC			0.50 BASIC		
L	0.020	0.024	0.0275	0.50	0.60	0.70
S	0.011 Typ.			0.28 Typ.		
y	-	-	0.004	-	-	0.10
θ	0°	-	8°	0°	-	8°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information

48LD CSP (6 x 8 mm) Outline Dimensions
(48TFBGA)

unit: mm



Symbol	Dimensions in mm		
	MIN.	NOM.	MAX.
A	---	---	1.20
A_1	0.20	0.25	0.30
D	5.90	6.00	6.10
E	7.90	8.00	8.10
D_1	---	3.75	---
E_1	---	5.25	---
e	---	0.75	---
b	0.30	0.35	0.40

Note:

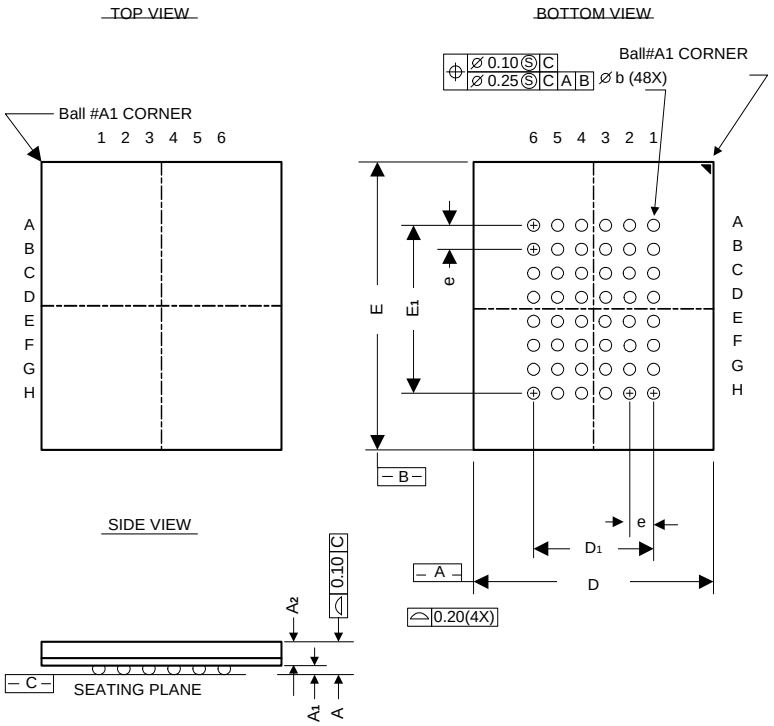
1. THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC MO192 (LOW PROFILE BGA FAMILY).
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM.

   THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
4. BALL PAD OPENING OF SUBSTRATE IS Φ 0.3mm (SMD)
   SUGGEST TO DESIGN THE PCB LAND SIZE AS Φ 0.3mm (NSMD)

Package Information

48LD CSP (8 x 10 mm) Outline Dimensions (48TFBGA)

unit: mm



Symbol	Dimensions in mm		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A_1	0.20	0.25	0.30
A_2	0.60	0.65	0.70
D	7.90	8.00	8.10
E	9.90	10.00	10.10
D_1	---	3.75	---
E_1	---	5.25	---
e	---	0.75	---
b	0.30	0.35	0.40

Notes:

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