AX58100
EtherCAT Slave Controller

Features

Document No: AX58100/V1.09/12/12/24

- **2/3-port EtherCAT Slave Controller (ESC) with 2 Integrated Fast Ethernet PHYs**
- **Standard EtherCAT Slave Controller (ESC)**
  - 8 Fieldbus Memory Management Units (FMMUs)
  - 8 Sync Managers
  - 64-bit distributed clock
  - 9K bytes RAM
- **Integrated Fast Ethernet PHYs**
  - Compliant with IEEE 802.3/802.3u 100BASE-TX/100BASE-FX
  - PHY loopback mode
  - Supports twisted pair crossover detection and auto-correction (HP Auto-MDIX)
  - Automatic polarity detection and correction
- **3rd Ethernet MII Port for Flexible EtherCAT Network Configurations**
- **Up to 32 Digital/General Purpose IOs**
  - Each IO is configurable individually and mapped to FMMU directly
- **SPI Slave Interface**
  - Supports Mode 3 timing modes
  - Supports MSB first transfer fashion
- **Local Bus Interface**
  - Supports 8-bit or 16-bit data bus width
  - Supports Asynchronous Local Bus
  - Supports BHE with 16-bit data bus width
- **Bridge**
  - Supports function and ESC registers mirror with selectable synchronous conditions
- **3-channel PWM Controller**
  - Adjustable frequency, phase align and BBM (Break Before Make) for all channels
  - Adjustable duty cycle, phase shift, and signal polarity per channel
- **Step & Direction Controller**
  - Adjustable step pulse width, polarity and the delay time for direction change
- **Incremental and Hall Encoder Interface**
  - Support single ended ABZ with configurable counting constant, polarity and Multiple Z-signal functions support
  - Supports clockwise/counter clockwise (CW/CCW) and direction-count (DIR/CLK) Inputs
  - Supports Hall sensor
- **Emergency Stop Input**
- **Configurable Watchdog for Outputs and Inputs Monitoring**
- **IRQ Event Output**
  - Interrupts for EtherCAT related events
  - Interrupts for Application related events
  - Interrupts for Watchdog Timeout
- **SPI Master Interface**
  - Programmable SPI clock frequency up to 50MHz
  - Supports 4 timing modes
  - Supports MSB/LSB first transfer fashion
  - Supports up to 8 SPI devices selection
  - Supports up to 8 channels, each channel with 8 bytes read/write buffer
  - Supports ADC Data Ready and DAC Data Loaded indication
  - Supports periodic data acquisition
  - Supports late sample for high latency device
  - Supports external interrupt input
- **Supports I^2C Master Interface**
- **Integrates On-chip Power-on Reset Circuit**
- **80-pin LQFP RoHS Compliant Package**
- **Operating Temperature Range: -40 to +105°C**

Target Applications

- Industrial Automation
- Motion/Motor Control
- Digital I/O Control
- Communication Module
- DAC/ADC Converters Control
- Sensors Data Acquisition
- Robotics
- Operator HMI Interfaces

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Typical Applications Diagram

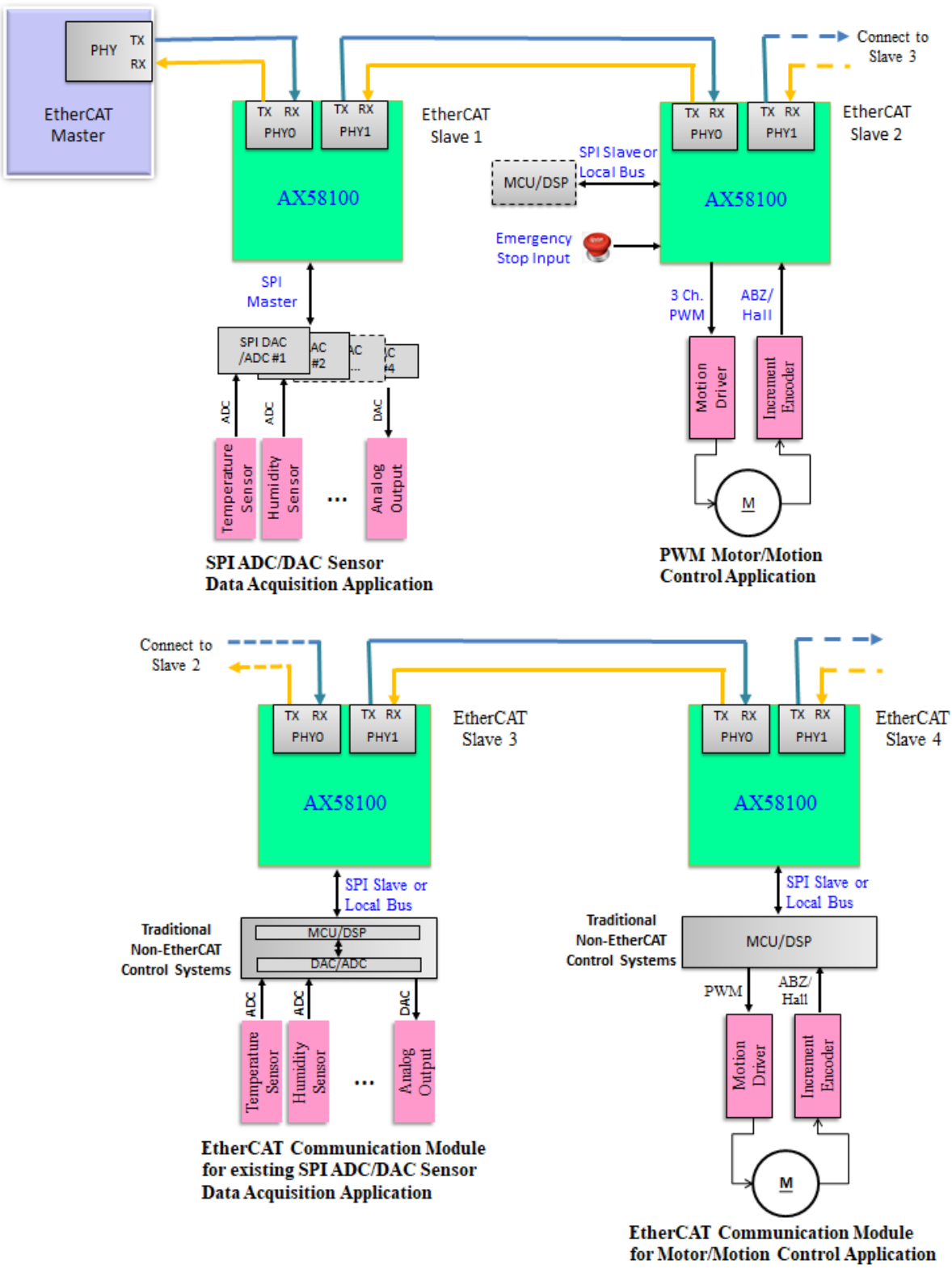

Figure 0-1: AX58100 Typical Applications Diagram

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1 Introduction

1.1 General Description

The AX58100 is a 2/3-port EtherCAT Slave Controller (ESC), licensed from Beckhoff Automation, with two integrated Fast Ethernet PHYs which support 100Mbps full-duplex operation and HP Auto-MDIX. The AX58100 supports the CANopen over EtherCAT (CoE), File Access over EtherCAT (FoE), Vendor Specific-protocol over EtherCAT (VoE), etc. Standard EtherCAT protocols provide a cost-effective solution for industrial automation applications, such as motion/motor/digital I/O control, Digital to Analog (DAC)/Analog to Digital (ADC) converters control, sensors data acquisition, and robotics, to be applied in industrial fieldbus.

The AX58100 provides either a three-channel PWM controller or a Step/Direction controller, and also provides an Increment/Hall encoder interface for closed-loop motor control, a SPI master controller for DAC/ADC converter control and sensors data acquisition, 32 DIOs for industrial I/O control and an I/O watchdog for functional safety.

The AX58100 provides two Process Data Interfaces (PDI), SPI slave and Local Bus, which support the connection with most popular MCU and DSP on those non-EtherCAT fieldbus applications. The AX58100 also provides two memory spaces, ESC and Function, users can decide which to access by using chip select. The bridge will synchronize two memory spaces' contents for EtherCAT Master to remotely control AX58100 functions (PWM, SPI master etc.). The AX58100 reports the ESC and Functions interrupt events to interrupt status registers and supports level or edge interrupt trigger mode to inform external MCU/DSP to manage these ESC and Functions interrupt events. AX58100 supports a configurable individual function SPI slave interface to enhance SPI slave bandwidth.

The AX58100, in 80-pin LQFP with EPAD, supports the RoHS compliant package and industrial grade operating temperature, which range from -40 to 105°C.

1.2 Block Diagram

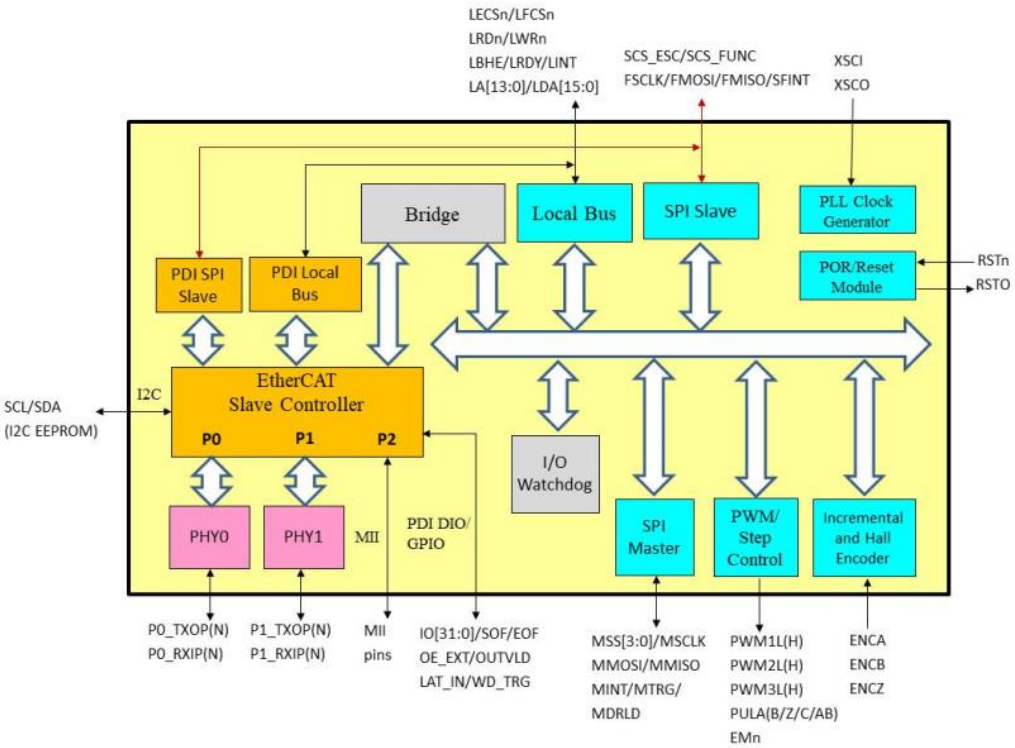


Figure 1-1: AX58100 Block Diagram

1.3 Pinout Diagram

AX58100 is housed in an 80-pin E-PAD LQFP package.

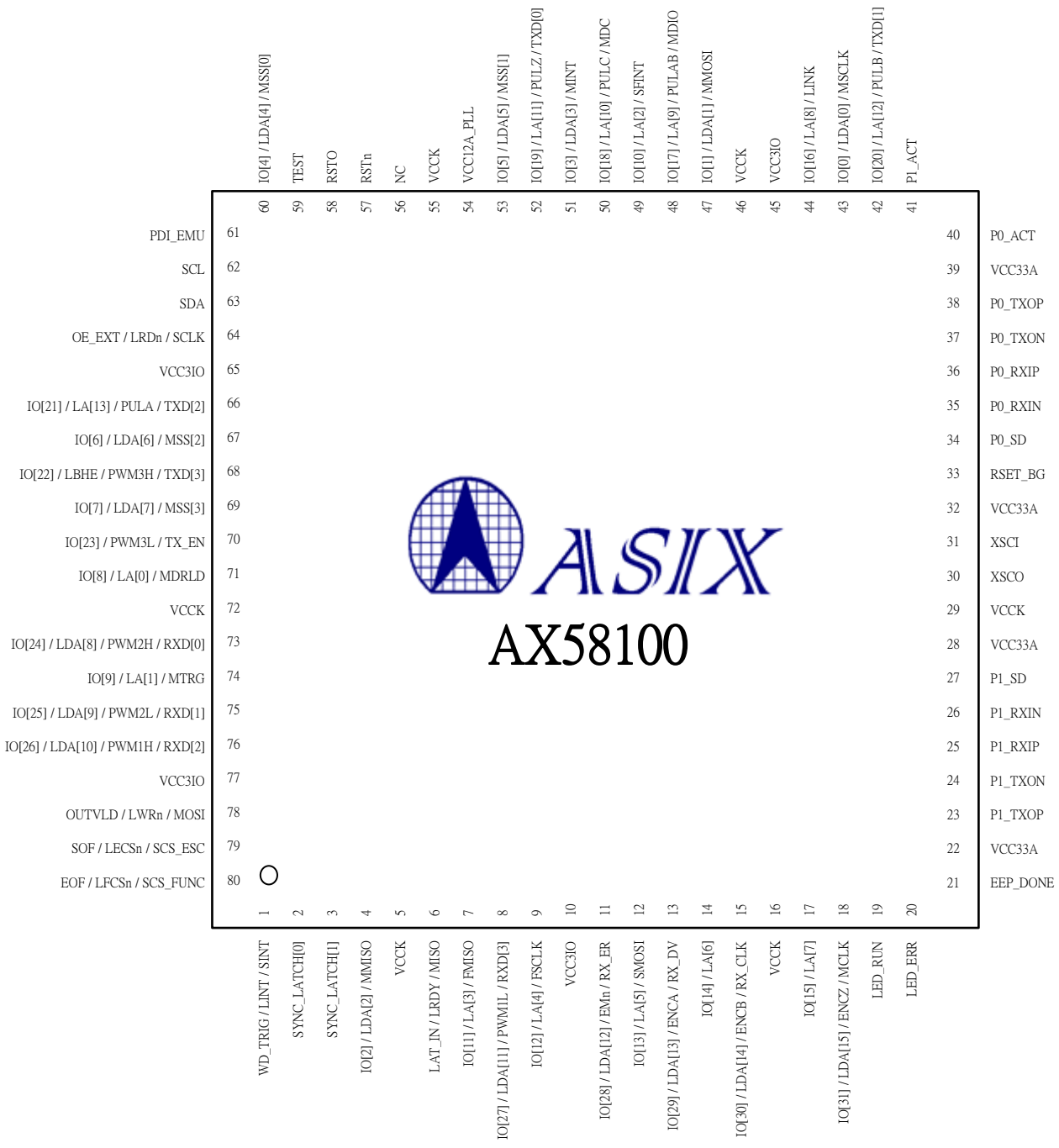


Figure 1-2: AX58100 Pinout Diagram

1.4 Signal Description

Following abbreviations are used in "Type" column of below pin description tables. Note that some I/O pins with multiple signal definitions on the same pin may have different attributes in "Type" column for different signal definition.

AB	Analog Bi-directional I/O	**PU**	Internal Pull-Up (75K)
AI	Analog Input	**PD**	Internal Pull-Down (75K)
AO	Analog Output	**P**	Power/Ground pin
B5	Bi-directional I/O, 3.3V with 5V tolerant	**S**	Schmitt Trigger
I5	Input, 3.3V with 5V tolerant	**T**	Tri-state
O5	Output, 3.3V with 5V tolerant	**4m**	4mA driving strength
I3	Input, 3.3V	**8m**	8mA driving strength
O3	Output, 3.3V		

For example, pin 6 in AX58100 package can be LAT_IN, MISO or LRDY. If LAT_IN is selected, its Type is I5; if MISO or LRDY is selected, its Type is O5 or O5/T. In other words, the T (tri-state) only takes effect in LRDY signal mode while LAT_IN and MISO signal mode don't. Users should refer to the table specific to the desired function for exact pin type definition.

The multi-function pin settings are configured by the I^2C Hardware Configuration EEPROM (HWCFGEE). Please refer to Section 3.2 for details.

1.4.1 General

Pin Name	Type	Pin No	Pin Description
TEST	I5/PD/S	59	Test mode enable For normal operation, please always tie to logic low or NC.
RSTn	I5/PU/S	57	Reset Input, active low RST_N is the hardware reset input used to reset this chip. This input is AND with internal Power-On-Reset (POR) circuit, which generates the main system reset for this chip.
RSTO\ RSTO_POL	O5/8m	58	Reset Output This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the RSTO polarity, please refer to Section 3.1.
XSCI	AI	31	Crystal 25MHz Input
XSCO	AB	30	Crystal 25MHz Output
SCL	O5/T/4m/S	62	I^2C Serial Clock line for I^2C master controller SCL is a tri-stateable output, which requires an external pull-up resistor.
SDA	B5/T/4m/S	63	I^2C Serial Data line for I^2C master controller. SDA is a tri-stateable output, which requires an external pull-up resistor.
PDI_EMU	I5	61	PDI Emulation enable
EEP_DONE	O5/8m	21	This pin asserted high indicates that the EEPROM is successfully loaded (Checksum matched) and the PDI can be used.
LED_RUN\ EEP_SIZE	B5/4m	19	LED_RUN is input direction during chip reset stage used to bootstrap the mode setting to decide the EEPROM size configuration, please refer to Section 3.1.
LED_ERR\ 3PORT_MODE	B5/4m	20	LED_ERR is input direction during chip reset stage used to bootstrap the mode setting to decide the Port 2 MII enable configuration, please refer to Section 3.1.
SYNC_LATCH[0]	B5/8m	2	Distributed Clocks SyncSignal output or LatchSignal input 0
SYNC_LATCH[1]	B5/8m	3	Distributed Clocks SyncSignal output or LatchSignal input 1
NC	I3	56	Reserved. Please connect to GND.

Table 1-1: Common Pin Description

Pin Name	Type	Pin No	Pin Description
P0_TXOP	AB	38	PHY 0 differential Transmitted Positive signal In the copper mode, the differential data is transmitted to the media on the TXOP/TXON signal pair in the MDI mode. In the fiber mode, the signal pair should be connected to the TX+/TX- pin of the fiber transceiver.
P0_TXON	AB	37	PHY 0 differential Transmitted Negative signal
P0_RXIP	AB	36	PHY 0 differential Received Positive signal In the copper mode, the differential data from the media is received on the RXIP/RXIN signal pair in the MDI mode. In the fiber mode, the signal pair should be connected to the RX+/RX- pin of the fiber transceiver.
P0_RXIN	AB	35	PHY 0 differential Received Negative signal
P0_SD	AB	34	PHY 0 fiber mode Signal Detect SD < 0.2V, Copper mode- 1.0V < SD < 1.8V, Fiber mode without detected signal. Generate far-end fault SD > 2.4V, Fiber mode with detected signal
P0_ACT\ P0_FIBER	B5/4m	40	PHY 0 Link/Activity LED This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the PHY 0 media mode, please refer to Section 3.1.
P1_TXOP	AB	23	PHY 1 differential Transmitted Positive signal Same as PHY0 TXOP/ON description
P1_TXON	AB	24	PHY 1 differential Transmitted Negative signal
P1_RXIP	AB	25	PHY 1 differential Received Positive signal Same as PHY0 RXIP/IN description
P1_RXIN	AB	26	PHY 1 differential Received Negative signal
P1_SD	AB	27	PHY 1 fiber mode Signal Detect Same P0_SD description
P1_ACT\ P1_FIBER	B5/4m	41	PHY 1 Link/Activity LED This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the PHY 1 media mode, please refer to Section 3.1.
RSET_BG	AO	33	PHY off-chip Bias Resistor Connects an external resistor of 12 KΩ ± 1% to the PCB analog ground.

Table 1-2: Ethernet PHY Pin Description

Pin Name	Type	Pin No	Pin Description
VCC3IO	P	10, 45, 65, 77	Digital Power for I/O pins, 3.3V Please add a 0.1uF bypass capacitor between each VCC3IO and GND.
VCCK	P	5, 16, 29, 46, 55, 72	Digital Power for core, 1.2V Please add a 0.1uF bypass capacitor between each VCCK and GND.
VCC33A	P	22, 28, 32, 39	Analog Power for Ethernet PHY, 3.3V Please add a 0.1uF bypass capacitor between VCC33A and GND.
VCC12A_PLL	P	54	Analog Power for PLL, 1.2V. Please add a 0.1uF bypass capacitor between VCC12A_PLL and GND.
GND	P	EPAD	Ground for all Analog and Digital Power.

Table 1-3: Power/Ground Pin Description

1.4.2 PDI Digital IO / GPIO

Pin Name	Type	Pin No	Pin Description
IO[31:24]	B5/8m	18, 15, 13, 11, 8, 76, 75, 73	Digital/General Purpose I/O[31:24]
IO[23:16]	B5/8m	70, 68, 66, 42, 52, 50, 48, 44	Digital /General Purpose I/O[23:16]
IO[15:8]	B5/8m	17, 14, 12, 9, 7, 49, 74, 71	Digital /General Purpose I/O[15:8]
IO[7:0]	B5/8m	69, 67, 53, 60, 51, 4, 47, 43	Digital /General Purpose I/O[7:0]
SOF	O5/8m	79	Start-of-Frame
EOF	O5/8m	80	End-of-Frame
OE_EXT	I5	64	Output Enable
OUTVLD	O5/8m	78	Output data Valid/Output event
LAT_IN	I5	6	external data Latch
WD_TRIG	O5/8m	1	Watchdog Trigger

Note: The IO[31:0] in PDI Digital mode is for DIO[31:0], in PDI SPI slave mode is for GPIO[31:0]

Table 1-4: PDI Digital I/O, GPIO Pin Description

1.4.3 ESC PDI / Function SPI Slave Interface

Pin Name	Type	Pin No	Pin Description
SCS_ESC	I5	79	SPI Chip Select for ESC
SCS_FUNC	I5	80	SPI Chip Select for Function
SCLK	I5	64	SPI Clock
MOSI	I5	78	SPI data MOSI
MISO	O5	6	SPI data MISO
SINT	O5/T	1	SPI Interrupt
FSCLK	I5	9	Function SPI Clock
FMOSI	I5	12	Function SPI data MOSI
FMISO	O5	7	Function SPI data MISO
SFINT	O5/T	49	SPI Function Interrupt

Note 1: The Function SPI slave could share pin with ESC or use independent pin, please refer to Section 3.2.

Note 2: “Function” means the design for PWM, Incremental/Hall Encoder, SPI Master, I/O Watchdog and Bridge function, excluding ESC.

Table 1-5: PDI SPI Slave Interface Pin Description

1.4.4 ESC PDI / Function Local Bus Interface

Pin Name	Type	Pin No	Pin Description
LECSn	I5	79	Local bus ESC Chip Select
LFCSn	I5	80	Local bus Function Chip Select
LRDn	I5	64	Local bus Read
LWRn	I5	78	Local bus Write
LBHE	I5	68	Local bus Byte High Enable (16-bit width only)
LRDY	O5/T	6	Local bus Ready
LINT	O5/T	1	Local bus Interrupt
LA[13:0]	I5	66, 42, 52, 50, 48, 44, 17, 14, 12, 9, 7, 49, 74, 71	Local bus Address bus
LDA[15:8]	B5	18, 15, 13, 11, 8, 76, 75, 73	Local bus Data bus [15:8]
LDA[7:0]	B5	69, 67, 53, 60, 51, 4, 47, 43	Local bus Data bus [7:0]

Note: “Function” means the design for PWM, Incremental/Hall Encoder, SPI Master, I/O Watchdog and Bridge function, excluding ESC.

Table 1-6: PDI Local Bus Interface Pin Description

1.4.5 PWM Motor Controller

Pin Name	Type	Pin No	Pin Description
PWM1L	O5/T	8	PWM 1 Low pin or STEP pin
PWM1H	O5/T	76	PWM 1 High pin or DIR pin
PWM2L	O5/T	75	PWM 2 Low pin
PWM2H	O5/T	73	PWM 2 High pin
PWM3L	O5/T	70	PWM 3 Low pin
PWM3H	O5/T	68	PWM 3 High pin
PULA	O5	66	Pulse A, programmable point A
PULB	O5	42	Pulse B, programmable point B
PULZ	O5	52	Pulse Z, PWM period start point
PULC	O5	50	Pulse C, PWM period central point
PULAB	O5	48	Pulse AB, toggle when programmable point A and B
EMn	I5	11	Emergency input, active low

Table 1-7: PWM Motor Controller Pin Description

1.4.6 Incremental / Hall Encoder Interface

Pin Name	Type	Pin No	Pin Description
ENCA	I5	13	ENC input A, Sin., CW, CLK, or HALL A
ENCB	I5	15	ENC input B, Cos., CCW, DIR, or HALL B
ENCZ	I5	18	ENC input Z, Zero point or HALL C

Table 1-8: Incremental/Hall Encoder Interface Pin Description

1.4.7 SPI Master

Pin Name	Type	Pin No	Pin Description
MSS[3:0]	O5	69, 67, 53, 60	SPI Master Slave Select
MSCLK	O5	43	SPI Master SCLK
MMOSI	O5	47	SPI Master MOSI
MMISO	I5	4	SPI Master MISO
MINT	I5	51	SPI Master Interrupt in
MTRG	I5	74	SPI Master Trigger in
MDRLD	B5	71	SPI Master ADC Data Ready / DAC Data Loaded

Table 1-9: SPI Master Pin Description

1.4.8 Port 2 MII

Pin Name	Type	Pin No	Pin Description
MCLK	O5	18	MII Clock 25 MHz clock source for Ethernet PHYs
LINK	I5	44	LINK Provided by the PHY if a 100 Mbps (Full Duplex) link is established.
MDC	O5	50	PHY Management Interface clock
MDIO	B5	48	PHY Management Interface data
TXD[3]	O5	68	Transmit data [3]
TXD[2:1] \ TX_SH[1:0]	O5	66, 42	Transmit data [2:1] This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the external PHY's TXD phase shift, please refer to Section 3.1.
TXD[0] \ LINK_POL	O5	52	Transmit data [0] These pins are input direction during chip reset use to bootstrap the mode setting to decide external PHY's LINK polarity, please refer to Section 3.1.
TX_EN	O5	70	Transmit enable
RX_CLK	I5	15	Receive Clock
RXD[3:0]	I5	8, 76, 75, 73	Receive data
RX_ER	I5	11	Receive error
RX_DV	I5	13	Receive data valid

Table 1-10: Port 2 MII Pin Description

2 Function Description

2.1 Clocks/Resets

The AX58100 requires a crystal (25MHz, ±25 PPM at room temperature) as the clock source. Internal PLL generates the 100MHz clock for EtherCAT Slave Controller (ESC) and also for other functions.

The AX58100 has three reset sources. First, during the VCCK power-on, the internal Power-On-Reset (POR) can generate a reset pulse to reset all the function blocks when the VCCK power pin rises to a certain threshold voltage level. The second reset is RSTn pin, which is to do the fundamental reset. And third, EtherCAT command reset, the EtherCAT master can send reset sequence to force AX58100 reset. AX58100 also supports a reset output RSTO polarity bootstrap configuration (RSTO_POL).

2.2 EtherCAT Slave Controller (ESC)

The AX58100 implements a 3-port EtherCAT slave controller (ESC), licensed from Beckhoff Automation, with 9 Kbytes Process Data RAM, 8 Fieldbus Memory Management Units (FMMUs), 8 Sync-Managers and a 64-bit Distributed Clock.

Port 0 and 1 integrate embedded Ethernet PHYs, and port 2 is an optional MII interface which are multi-function pins shared with other interfaces (i.e. PWM, Hall, Local Bus, Digital I/O). Packets are forwarded in the following order: **Port 0->EtherCAT Processing Unit->Port 1->Port 2**.

The Process Data Interface (PDI, also named host interface) provides SPI slave, asynchronous 8/16-bit microcontroller interface (also named Asynchronous Local Bus) and Digital I/O. The SPI slave and asynchronous 8/16-bit Local Bus interface will be used when external MCU in employed the slave system, and the Digital I/O is used for when direct I/O control.

The AX58100 supports function register mirror from/to ESC memory space. The mirror registers located at process data memory address from 0x3000 to 0x33FF.

For detailed information about the EtherCAT technology, the EtherCAT core mechanisms, and major features, we refer to the official standard documentations and guidelines available from ETG (www.ethercat.org, ETG.1000), IEC (http://www.iec.ch, IEC61158, IEC61784-2, IEC 61800-7), and Beckhoff (http://www.beckhoff.de, technical specification) web sites.

2.3 Ethernet PHY

The AX58100 is embedded two DSP-based Ethernet PHYs, which are fully compliant with the 100BASE-TX and 100BASE-FX Ethernet standards such as IEEE 802.3u, and ANSI X3.263-1995 (FDDI-TP-PMD). In copper mode, it supports the MDI/MDIX auto-crossover function (HP Auto-MDIX).

2.4 Bridge Function

The AX58100 has two memory spaces, one for ESC and another for AX58100 specific functions. The bridge handles data synchronization between ESC's memory and function registers, and uses EthterCAT packet's SOF, EOF, ESC control signal: SYNCx and LATx, PDI chip select (ESC and function) asserts and de-assert, the PWM cycle starts, register writes and register data change, total 13 sources to synchronize two space's register content. Each function mirror could be enabled independent, the interrupt related registers mirror (INTCR and INTSR) are also enabled when any function mirror is enabled.

2.5 I/O Watchdog

The I/O Watchdog is for AX58100 safety engine and used to monitor I/O signals toggle status and an emergency stop input (EMn) pin. When I/O signals don't match a pattern or keep over excepted time, the watchdog will be triggered, or EMn input pin asserted which would force I/O pads to enter default level. The default level is configurable which could be driven low, high or Tristate.

2.6 PWM Controller

The PWM control module provides Pulse Width Modulation (PWM) and STEP / DIR to control motor driving. The PWM mode has eight pins. There are three pairs of control signal. Each control signal pair has a high pulse pin (PWMxH) and low pulse pin (PWMxL) control power drive circuit. Others are two alignment pins, PULZ and PULC point cycle start and central time, and three programmable trigger pins, PULA PULB and PULAB. The step pulse mode has 2 pins, step (STEP) and direction (DIR), which connect to step motor controller and share PWM1H/L pins.

The PWM supports up to 12.5MHz output frequency, and programmable polarity, timing adjustment.

2.7 Incremental and Hall Encoder Interface

The AX58100 provides an interface with a linear or rotary incremental encoder to get position information, and supports four input modes, including the Sin/Cos mode (A / B / Z pins), Clock-Wise mode (CW / CCW / Z pins), Direction-Clock mode (DIR / CLK / Z pins) and the Hall mode (A / B / C pins). It can accumulate positions in three modes, Sin/Cos, Clock-Wise and Direction-Clock modes, and calculate the GAP time in Hall mode.

The Sin/Cos mode supports input frequency up to 8.33MHz, CW/CCW and DIR/CLK up to 16.66MHz, and the Hall mode up to 2.77MHz respectively.

2.8 SPI Master Controller

The Serial Peripheral Interface (SPI) master controller provides a full-duplex, synchronous serial communication interface (4 wires) to flexibly work with numerous SPI peripheral devices or microcontroller with the SPI slave. The SPI master controller supports 4 types of interface timing modes, namely, mode 0, 1, 2, and 3 to allow working with most SPI devices available. It also supports MSB/LSB first data transfer.

The SPI master controller supports 8 channels, which could sequentially access per device, and supports variable transfer length up to 8 bytes each channel. It also supports multi-channel access to the same device, and the data length could be up to 64bytes. For high performance applications, the SPI master controller supports continuous transfer data between the SPI device and data registers.

The SPI master controller provides 4 chip select, supports one-cold encode output (up to 4 devices), or uses binary encode output (use an external binary decoder) up to 8 devices.

The SPI master controller supports standard SPI device access without glue logic circuit. Besides, it supports “trigger data ready input” for ADC application, and also supports “data loaded indication out” and “data path daisy chain” for DAC application.

The MSCLK (SPI clock) is programmable by software and can run up to 50MHz.

3 Chip Configuration and Memory Map Description

3.1 Bootstrap Pins for Chip Configuration

The AX58100 supports five multi-function bootstrap pins (pin 19, 20, 58, 40, and 41) for five hardware configurations, i.e. external I^2C EEPROM size, ESC supported port number, RSTO polarity and integrated port 0/1 PHY media mode; and it also supports other three multi-function bootstrap pins (pin 42, 52, 66) for the configuration of port 2 MII signals. User needs to utilize an external resistor to pull up / down these bootstrap pins.

Pins	Signal Name	Description
19	EEP_SIZE	I^2C EEPROM Size 0: 1 Kbit to 16Kbit 1: 32Kbit to 4Mbit
20	3PORT_MODE	ESC port number 0: 2 ports mode 1: 3 ports mode
58	RSTO_POL	RSTO Reset Output Polarity 0: Active Low 1: Active High
61	PDI_EMU	Device emulation (0x0141.0) 0: Device status register is controlled by PDI 1: Device status register is identical to device control register
40	P0_FIBER	Port 0 PHY media mode 0: Copper mode 1: Fiber mode
41	P1_FIBER	Port 1 PHY Media mode 0: Copper mode 1: Fiber mode
66	TX_SH [1]	Port 2 MII TXD Align position 2‘b00: Align with MCLK, 2’b01: Delay 1/4 phase with MCLK 2’b10: Delay 1/2 phase with MCLK 2’b11: Delay 3/4 phase with MCLK
42	TX_SH [0]	
52	LINK_POL	Port 2 MII LINK Polarity 0: Active Low 1: Active High

Table 3-1: Bootstrap Pins Configuration

3.2 Hardware Configuration EEPROM (HWCFGEE)

The AX58100 I²C master controller supports the communication to external I²C devices and an I²C Hardware Configuration EEPROM Loader to support loading the EtherCAT Slave Information (ESI) from external I²C EEPROM during chip reset. The AX58100 supports I²C EEPROM with EEPROM size from 1 Kbit (128 bytes) to 4 Mbit (500Kbytes).

The AX58100 I2C Hardware Configuration EEPROM layout is shown in following figure.

EEPROM Byte Offset	EEPROM Word Offset	Parameter	ESC Register Offset
ESC Configuration Area			
0x00	0x00	PDI Control	0x0140
0x01		ESC Configuration (bit 2 is also mapped to ESC register 0x0110.2)	0x0141
0x02	0x01	PDI Configuration	0x0150
0x03		Sync/Latch [1:0] Configuration	0x0151
0x05 - 0x04	0x02	Pulse Length of SyncSignals	0x0983 - 0x0982
0x07 - 0x06	0x03	Extended PDI Configuration	0x0153 - 0x0152
0x09 - 0x08	0x04	Configured Station Alias	0x0013 - 0x0012
0x0A	0x05	Host Interface Extend Setting and Drive Strength	
0x0B		Reserved, shall be zero	
0x0C	0x06	Reserved, shall be zero	
0x0D		Multi-Function Select and Drive Strength	
0x0F - 0x0E	0x07	Checksum	
0x13 - 0x10	0x09 – 0x08	Vendor ID	
0x17 - 0x14	0x0B – 0x0A	Product Code	
0x1B - 0x18	0x0D – 0x0C	Revision Number	
0x1F - 0x1C	0x0F – 0x0E	Serial Number	
0x27 - 0x20	0x13 – 0x10	Reserved	
Bootstrap Mailbox Config			
0x29 - 0x28	0x14	Bootstrap Receive Mailbox Offset	
0x2B - 0x2A	0x15	Bootstrap Receive Mailbox Size	
0x2D - 0x2C	0x16	Bootstrap Send Mailbox Offset	
0x2F - 0x2E	0x17	Bootstrap Send Mailbox Size	
Mailbox Sync Man Config			
0x31 - 0x30	0x18	Standard Receive Mailbox Offset	
0x33 - 0x32	0x19	Standard Receive Mailbox Size	
0x35 - 0x34	0x1A	Standard Send Mailbox Offset	
0x37 - 0x36	0x1B	Standard Send Mailbox Size	
0x39 - 0x38	0x1C	Mailbox Protocol	
0x3F - 0x3A	0x1F – 0x1D	Reserved	
0x7B - 0x40	0x3D – 0x20	Reserved	
0x7D - 0x7C	0x3E	Size	
0x7F - 0x7E	0x3F	Version	
ESC Category 1 (for AX58100 Bridge Access Configuration if used) *Note1			
0x81 ~ 0x80	0x40	Category 1 Type (Default: **0x0001**)	
0x83 ~ 0x82	0x41	Category 1 Data Size (words) (Default: **0x0021**)	
0x84	0x42	MCTLR Access Control	0x0580

EEPROM Byte Offset	EEPROM Word Offset	Parameter	ESC Register Offset
0x85		PXCFGR Access Control	0x0581
0x86	0x43	PTAPPR Access Control	0x0582
0x87		PTBPPR Access Control	0x0583
0x88	0x44	PPCR Access Control	0x0584
0x89		PBBMR Access Control	0x0585
0x8A	0x45	P1CTRLR Access Control	0x0586
0x8B		P1SHR Access Control	0x0587
0x8C	0x46	P1HPWR Access Control	0x0588
0x8D		P2CTRLR Access Control	0x0589
0x8E	0x47	P2SHR Access Control	0x058A
0x8F		P2HPWR Access Control	0x058B
0x90	0x48	P3CTRLR Access Control	0x058C
0x91		P3SHR Access Control	0x058D
0x92	0x49	P3HPWR Access Control	0x058E
0x93		SGTR Access Control	0x058F
0x94	0x4A	SHPWR Access Control	0x0590
0x95		TDLYR Access Control	0x0591
0x96	0x4B	STNR Access Control	0x0592
0x97		SCFGR Access Control	0x0593
0x98	0x4C	SCTRLR Access Control	0x0594
0x99		SCNTR Access Control	0x0595
0x9A	0x4D	ECNTVR Access Control	0x0596
0x9B		ECNSTR Access Control	0x0597
0x9C	0x4E	ELATR Access Control	0x0598
0x9D		EMODR Access Control	0x0599
0x9E	0x4F	ECLRR Access Control	0x059A
0x9F		HALSTR Access Control	0x059B
0xA0	0x50	WTR Access Control	0x059C
0xA1		WCFGR Access Control	0x059D
0xA2	0x51	WTPVCR Access Control	0x059E
0xA3		WMSPR Access Control	0x059F
0xA4	0x52	WMMR Access Control	0x05A0
0xA5		WOMR Access Control	0x05A1
0xA6	0x53	WOER Access Control	0x05A2
0xA7		WOPR Access Control	0x05A3
0xA8	0x54	WTPVR Access Control	0x05A4
0xA9		SPICFGR Access Control	0x05A5
0xAA	0x55	SPIBRR Access Control	0x05A6
0xAB		SPIDBSR Access Control	0x05A7
0xAC	0x56	SPIDTR Access Control	0x05A8
0xAD		SPIRPTR Access Control	0x05A9
0xAE	0x57	SPILTR Access Control	0x05AA
0xAF		SPIPRLR Access Control	0x05AB
0xB0	0x58	SPI01BCR Access Control	0x05AC
0xB1		SPI23BCR Access Control	0x05AD
0xB2	0x59	SPI45BCR Access Control	0x05AE
0xB3		SPI67BCR Access Control	0x05AF
0xB4	0x5A	SPI03SSR Access Control	0x05B0

EEPROM Byte Offset	EEPROM Word Offset	Parameter	ESC Register Offset
0xB5		SPI47SSR Access Control	0x05B1
0xB6	0x5B	SPIINTSR Access Control	0x05B2
0xB7		SPITSR Access Control	0x05B3
0xB8	0x5C	SPIPOSR Access Control	0x05B4
0xB9		SPI Data Status (SPIDSR and SPIDSMR) Access Control	0x05B5
0xBA	0x5D	SPIC0DR Access Control	0x05B6
0xBB		SPIC1DR Access Control	0x05B7
0xBC	0x5E	SPIC2DR Access Control	0x05B8
0xBD		SPIC3DR Access Control	0x05B9
0xBE	0x5F	SPIC4DR Access Control	0x05BA
0xBF		SPIC5DR Access Control	0x05BB
0xC0	0x60	SPIC6DR Access Control	0x05BC
0xC1		SPIC7DR Access Control	0x05BD
0xC2	0x61	SPIMCR Access Control	0x05BE
0xC3		INTCR Access Control	0x05BF
0xC4	0x62	INTSR Access Control	0x05C0
0xC5		Function Mirror Enable	0x05C1
Other ESC Categories Information (Subdivided in Categories)			
		…	
		Category Strings	
		Category Generals	
		Category FMMU	
		Category SyncManager	
		Category Tx - / RxPDO for each PDO	

Figure 3-1: AX58100 I²C EEPROM Layout

Note 1: Reserved words or reserved bits of the ESC Configuration Area should be filled with 0.
Note 2: When (re-) configuring the EEPROM from an EtherCAT master system special care must be taken. Not every master allows writing a category 1 entry to the EEPROM. There are different ways to write this into the EEPROM for automatically loading access control configuration when AX58100 booting.
1. Use preprogrammed I²C EEPROM.
2. Use a different category, e.g., 2049, first. Then overwrite the upper byte with 0 with a single EEPROM byte writes.

The AX58100 HWCFGEE contents from offset 0x00 to 0x7F are mandatory, as well as the general category (at least the minimum I2C EEPROM size is 2Kbit, and for the complex devices with many categories should be equipped with 32 Kbit EEPROMs or larger one). The ESC Configuration Area is used for AX58100 hardware configuration. All other areas are used by the EtherCAT master or the local application.

The ESC Configuration Area (EEPROM offset 0x00 to 0x0F) is automatically read by AX58100 after power-on or reset. It contains the PDI configuration, Distributed Clocks settings, and Configured Station Alias. The consistency of the ESC Configuration Area data is secured with a checksum.

The EtherCAT Master can invoke reloading the EEPROM contents. In this case, the Configured Station Alias register 0x0012:0x0013 and ESC Configuration register bits 0x0141 [1,4,5,6,7] (enhanced link detection) are not transferred into the registers. They are only transferred at the initial EEPROM loading after power-on or reset.

To use AX58100 bridge functionalities, users should define the Bridger Access Configuration parameters in the first category located at EEPROM offset 0x80. The Category Type must be 0x0001and the Category Data Size

must be 0x0021 so the AX58100 will automatically load the EEPROM Bridger Access Configuration parameters into the Bridge Access Configuration registers memory area starting at 0x0580 after power-on or reset.

3.2.1 EEPROM Contents Detailed Descriptions

PDI Control (0x00)

Bit	Description
7:0	PDI Control [7:0] 0x00: Interface deactivated (no PDI) 0x04: Digital I/O 0x05: SPI Slave 0x08: 16-bit Asynchronous Local Bus 0x09: 8-bit Asynchronous Local Bus Others: reserved

ESC Configuration (0x01)

Bit	Description
0	Device emulation enables (control of AL status)
1	Enhanced Link detection all ports
3:2	Reserved
4	Enhanced Link port 0
5	Enhanced Link port 1
6	Enhanced Link port 2
7	Reserved

PDI Configuration (0x02)

Digital I/O

Bit	Description
0	OUTVALID polarity
1	OUTVALID mode
2	Unidirectional/Bidirectional mode
3	Watchdog behavior
5:4	Input DATA is sampled
7:6	Output DATA is updated

SPI Slave

Bit	Description
1:0	SPI mode
3:2	SPI_IRQ output driver/polarity
4	SPI_SEL polarity
5	Data Out sample mode
7:6	Reserved

Asynchronous Local Bus

Bit	Description
1:0	BUSY/RDY driver/polarity
3:2	IRQ driver/polarity
4	BHE/Byte Enable polarity
7:5	Reserved

Sync/Latch[1:0] Configuration (0x03)

Bit	Description
1:0	SYNC0 output driver/polarity
2	SYNC0/LATCH0 configuration
3	SYNC0 mapped to AL Event Request
5:4	SYNC1 output driver/polarity
6	SYNC1/LATCH1 configuration
7	SYNC1 mapped to AL Event Request

Pulse Length SyncSignals (0x05 - 0x04)

Bit	Description
15:0	Pulse length of SyncSignal

Extended PDI Configuration (0x07 - 0x06)

Digital I/O / SPI Slave (for GPIO)

Bit	Description
0	Digital I/O or GPIO Digital I/O or GPIO are configured in pairs (1:0) as inputs or outputs: 0: Input 1: Output
1	3:2 pair (0: Input, 1: Output)
2	5:4 pair (0: Input, 1: Output)
3	7:6 pair (0: Input, 1: Output)
4	9:8 pair (0: Input, 1: Output)
5	11:10 pair (0: Input, 1: Output)
6	13:12 pair (0: Input, 1: Output)
7	15:14 pair (0: Input, 1: Output)
8	17:16 pair (0: Input, 1: Output)
9	19:18 pair (0: Input, 1: Output)
10	21:20 pair (0: Input, 1: Output)
11	23:22 pair (0: Input, 1: Output)
12	25:24 pair (0: Input, 1: Output)
13	27:26 pair (0: Input, 1: Output)
14	29:28 pair (0: Input, 1: Output)
15	31:30 pair (0: Input, 1: Output)

Asynchronous Local Bus

Bit	Description
0	Read BUSY delay
1	Perform internal write
10:2	Reserved
11	23:22 pair (data bus 8-bit width only) (0: Input, 1: Output)
12	25:24 pair (data bus 8-bit width only) (0: Input, 1: Output)
13	27:26 pair (data bus 8-bit width only) (0: Input, 1: Output)
14	29:28 pair (data bus 8-bit width only) (0: Input, 1: Output)
15	31:30 pair (data bus 8-bit width only) (0: Input, 1: Output)

Configured Station Alias (0x09 - 0x08)

Bit	Description
15:0	Alias Address used for node addressing

Host Interface Extend Setting and Drive Strength (0x0A)

Digital I/O

Bit	Description
4:0	Reserved
5	Control Driving Select: 0: 4mA 1: 8mA
6	IO [9:0] Driving Select: 0: 4mA 1: 8mA
7	IO [15:10] Driving Select: 0: 4mA 1: 8mA

SPI Slave / Asynchronous Local Bus

Bit	Description
3:0	Interrupt Edge Pulse Length (INTP_LEN) Interrupt Edge Pulse = (INTP_LEN+1) * 100ns
4	The trigger type of interrupt signal, SINT / LINT 0: Level trigger. 1: Edge trigger.
5	Control Driving Select: 0: 4mA 1: 8mA
6	IO [9:0] Driving Select: 0: 4mA 1: 8mA
7	IO [15:10] Driving Select: 0: 4mA 1: 8mA

Multi-Function Select and Drive Strength (0x0D)

Bit	Description
0	IO [9:0] select: 0: IO [9:0] 1: MTRG, MDRLD, MSS [3:0], MINT, MMISO, MMOSI, MSCLK, Note: in Local Bus mode this bit no function
1	IO [15:10] (SPI slave separates) select: 0: IO [15:10] 1: IO [15:14], FMOSI, FSCLK, FMISO, SFINT Note: in Local Bus mode this bit no function
2	IO [21:16] select: 0: IO [21:16] 1: PULA, PULB, PULZ, PULZ, PULAB, IO [16] Note: in Local Bus mode this bit no function
3	IO [25:22] select: 0: IO [25:22] 1: PWM2L, PWM2H, PWM3L, PWM3H Note: in Local Bus 16 bits mode this bit no function
4	IO [28:26] select: 0: IO [28:26] 1: EM, PWM1L, PWM1H Note: in Local Bus 16 bits mode this bit no function
5	IO [31:29] select: 0: IO [31:29] 1: ENCZ, ENCB, ENCA Note: in Local Bus 16 bits mode this bit no function

6	IO [21:16] Driving Select: 0: 4mA 1: 8mA
7	IO [31:22] Driving Select: 0: 4mA 1: 8mA

Note: When MII port 2 enable, the IO [31:16] pins are forced to MII port 2

Checksum (0x0F - 0x0E)

Bit	Description
15:0	Checksum Low byte contains remainder of division of EEPROM offset 0x00 to 0x0D as unsigned number divided by the polynomial X^8+X^2+X+1 (initial value 0xFF) For debugging purposes, it is possible to disable the checksum validation with a checksum value of 0x88A4. **Note that NEVER use this for production!**

Category 1 Type (0x81 - 0x80)

Bit	Description
15:0	Category 1 Type MUST be 0x0001

Category 1 Data Size (0x83 - 0x82)

Bit	Description
15:0	Category 1 Data Size (words) MUST be 0x0021

MCTLR Access Control (0x84)

Bit	Description
3:0	Sync. Source Select 0x0: Always triggered 0x1: Start Of Frame (SOF) 0x2: End Of Frame (EOF) 0x3: SYNC0 signal 0x4: LATCH0 signal 0x5: SYNC1 signal 0x6: LATCH1 signal 0x7: After write access 0x8: Trigger when data value changes 0x9: PDI Chip Select Assert 0xA: PDI Chip Select De-assert 0xB: FUNC Chip Select Assert 0xC: FUNC Chip Select De-assert 0xD: Trigger at start of MFC PWM cycle Others: Always triggered
4	ESC Access Enable 0: Writeable with Function Host Interface 1: Writeable with ESC
7:5	Reserved

The Bit Definitions of the other parameters from EEPROM offset 0x85 to 0xC4 are the same as the Bit Definitions of EEPROM offset 0x84.

Function mirror enable (0xC5)

Bit	Description
0	PWM function register mirror: 0: Disable PWM function register mirror 1: Enable PWM function register mirror
1	ENC function register mirror: 0: Disable ENC function register mirror 1: Enable ENC function register mirror
2	SPI Master function register mirror: 0: Disable SPI Master function register mirror 1: Enable SPI Master function register mirror
3	IO Watchdog function register mirror: 0: Disable IO Watchdog function register mirror 1: Enable IO Watchdog function register mirror
7:4	Reserved

3.3 Memory Map

This section introduces the memory mapping in AX58100. AX58100 provides SPI and Local Bus slave interfaces for both ESC PDI and Function to access the internal registers. Section 3.3.1 introduces the ESC memory map which can be accessed by PDI SPI or Local bus interface ,and section 3.3.2 introduces the Function register map which can be accessed by Function SPI or Local Bus interface. Due to the Function registers can be accessed by PDI interface and EtherCAT Master directly. So, section 3.3.3 introduces the relationship between Function and ESC PDI through the Bridge function.

3.3.1 ESC Memory Map

ESC Address	Length (Bytes)	Description
ESC Information		
0x0000	1	Type
0x0001	1	Revision
0x0002	2	Build
0x0004	1	FMMUs supported
0x0005	1	SyncManagers supported
0x0006	1	RAM Size
0x0007	1	Port Descriptor
0x0008	2	ESC Features supported
Station Address		
0x0010	2	Configured Station Address
0x0012	2	Configured Station Alias
Write Protection		
0x0020	1	Write Register Enable
0x0021	1	Write Register Protection
0x0030	1	ESC Write Enable
0x0031	1	ESC Write Protection
Data Link Layer		
0x0040	1	ESC Reset ECAT
0x0041	1	ESC Reset PDI
0x0100	4	ESC DL Control
0x0108	2	Physical Read/Write Offset
0x0110	2	ESC DL Status
Application Layer		
0x0120	2	AL Control
0x0130	2	AL Status
0x0134	2	AL Status Code
0x0138	1	RUN LED Override
0x0139	1	ERR LED Override
PDI		
0x0140	1	PDI Control
0x0141	1	ESC Configuration
0x0150	1	PDI Configuration
0x0151	1	Sync/Latch PDI Configuration
0x0152	2	Extended PDI Configuration
Interrupts		
0x0200	2	ECAT Event Mask
0x0204	4	AL Event Mask
0x0210	2	ECAT Event Request

0x0220	4	AL Event Request
Error Counters		
0x0300	4x2	RX Error Counter [3:0]
0x0308	4x1	Forwarded RX Error counter [3:0]
0x030C	1	ECAT Processing Unit Error Counter
0x030D	1	PDI Error Counter
0x030E	1	PDI Error Code
0x0310	4x1	Lost Link Counter [3:0]
Watchdogs		
0x0400	2	Watchdog Divider
0x0410	2	Watchdog Time PDI
0x0420	2	Watchdog Time Process Data
0x0440	2	Watchdog Status Process Data
0x0442	1	Watchdog Counter Process Data
0x0443	1	Watchdog Counter PDI
I^2C EEPROM Interface		
0x0500	1	EEPROM Configuration
0x0501	1	EEPROM PDI Access State
0x0502	2	EEPROM Control/Status
0x0504	4	EEPROM Address
0x0508	4	EEPROM Data
MII Management Interface		
0x0510	2	MII Management Control/Status
0x0512	1	PHY Address
0x0513	1	PHY Register Address
0x0514	2	PHY Data
0x0516	1	MII Management ECAT Access State
0x0517	1	MII Management PDI Access State
Bridge Access Configuration (Refer to Section 9.3 of AX58100 Full datasheet)		
0x0580	1	MCTLR Access Control Register
0x0581	1	PXCFGR Access Control Register
0x0582	1	PTAPPR Access Control Register
0x0583	1	PTBPPR Access Control Register
0x0584	1	PPCR Access Control Register
0x0585	1	PBBMR Access Control Register
0x0586	1	P1CTRLR Access Control Register
0x0587	1	P1SHR Access Control Register
0x0588	1	P1HPWR Access Control Register
0x0589	1	P2CTRLR Access Control Register
0x058A	1	P2SHR Access Control Register
0x058B	1	P2HPWR Access Control Register
0x058C	1	P3CTRLR Access Control Register
0x058D	1	P3SHR Access Control Register
0x058E	1	P3HPWR Access Control Register
0x058F	1	Step Gap Time Access Control Register
0x0590	1	SHPWR Access Control Register
0x0591	1	TDLYR Access Control Register
0x0592	1	Step Target Number Access Control Register
0x0593	1	SCFGR Access Control Register
0x0594	1	SCTRLR Access Control Register
0x0595	1	Step Counter Content Access Control Register
0x0596	1	Encoder Counter Value Access Control Register
0x0597	1	Encoder Constant Access Control Register

0x0598	1	Encoder Latched Access Control Register
0x0599	1	EMODR Access Control Register
0x059A	1	ECLRR Access Control Register
0x059B	1	HALSTR Access Control Register
0x059C	1	Watchdog Timer Access Control Register
0x059D	1	WCFGR Access Control Register
0x059E	1	WTPVCR Access Control Register
0x059F	1	Watchdog monitored Polarity Access Control Register
0x05A0	1	Watchdog monitored Mask Access Control Register
0x05A1	1	Watchdog Output Mask Access Control Register
0x05A2	1	Watchdog Output Enable Access Control Register
0x05A3	1	Watchdog Output Polarity Access Control Register
0x05A4	1	Watchdog Timer Peak value Access Control Register
0x05A5	1	SPICFGR Access Control Register
0x05A6	1	SPIBRR Access Control Register
0x05A7	1	SPIDBSR Access Control Register
0x05A8	1	SPIDTR Access Control Register
0x05A9	1	SPIRPTR Access Control Register
0x05AA	1	SPILTR Access Control Register
0x05AB	1	SPIPRLR Access Control Register
0x05AC	1	SPI01BCR Access Control Register
0x05AD	1	SPI23BCR Access Control Register
0x05AE	1	SPI45BCR Access Control Register
0x05AF	1	SPI67BCR Access Control Register
0x05B0	1	SPI03SSR Access Control Register
0x05B1	1	SPI47SSR Access Control Register
0x05B2	1	SPINTSR Access Control Register
0x05B3	1	SPITSR Access Control Register
0x05B4	1	SPIPOSR Access Control Register
0x05B5	1	SPI Data Status (SPIDSR and SPIDSMR) Access Control Register
0x05B6	1	SPIC0DR Access Control Register
0x05B7	1	SPIC1DR Access Control Register
0x05B8	1	SPIC2DR Access Control Register
0x05B9	1	SPIC3DR Access Control Register
0x05BA	1	SPIC4DR Access Control Register
0x05BB	1	SPIC5DR Access Control Register
0x05BC	1	SPIC6DR Access Control Register
0x05BD	1	SPIC7DR Access Control Register
0x05BE	1	SPIMCR Access Control Register
0x05BF	1	INTCR Access Control Register
0x05C0	1	INTSR Access Control Register
0x05C1	1	Function Mirror Enable Register
0x0600:0x067F	**FMMU[7:0]**	
+0x0	4	Logical Start Address
+0x4	2	Length
+0x6	1	Logical Start bit
+0x7	1	Logical Stop bit
+0x8	2	Physical Start Address
+0xA	1	Physical Start bit
+0xB	1	Type
+0xC	1	Activate
+0xD	3	Reserved
0x0800:0x083F	**SyncManager[7:0]**	

+0x0	2	Physical Start Address
+0x2	2	Length
+0x4	1	Control Register
+0x5	1	Status Register
+0x6	1	Activate
+0x7	1	PDI Control
0x0900:0x09FF	**Distributed Clocks (DC)**	
DC – Receive Times		
0x0900	4	Receive Time Port 0
0x0904	4	Receive Time Port 1
0x0908	4	Receive Time Port 2
0x090C	4	Receive Time Port 3
DC – Time Loop Control Unit		
0x0910	4(W)/8(R)	System Time
0x0918	8	Receive Time ECAT Processing Unit
0x0920	8	System Time Offset
0x0928	4	System Time Delay
0x092C	4	System Time Difference
0x0930	2	Speed Counter Start
0x0932	2	Speed Counter Diff
0x0934	1	System Time Difference Filter Depth
0x0935	1	Speed Counter Filter Depth
DC – Cyclic Unit Control		
0x0980	1	Cyclic Unit Control
DC – SYNC Out Unit		
0x0981	1	Activation
0x0982	2	Pulse Length of SyncSignals
0x0984	1	Activation Status
0x098E	1	SYNC0 Status
0x098F	1	SYNC1 Status
0x0990	8	Start Time Cyclic Operation/Next SYNC0 Pulse
0x0998	8	Next SYNC1 Pulse
0x09A0	4	SYNC0 Cycle Time
0x09A4	4	SYNC1 Cycle Time
DC – Latch In Unit		
0x09A8	1	Latch0 Control
0x09A9	1	Latch1 Control
0x09AE	1	Latch0 Status
0x09AF	1	Latch1 Status
0x09B0	8	Latch0 Time Positive Edge
0x09B8	8	Latch0 Time Negative Edge
0x09C0	8	Latch1 Time Positive Edge
0x09C8	8	Latch1 Time Negative Edge
DC – SyncManager Event Times		
0x09F0	4	EtherCAT Buffer Change Event Time
0x09F8	4	PDI Buffer Start Event Time
0x09FC	4	PDI Buffer Change Event Time
ESC specific		
0x0E00	8	Product ID
0x0E08	8	Vendor ID
Digital Input/Output		
0x0F00	4	Digital I/O Output Data

0x0F10	4	General Purpose Outputs
0x0F18	4	General Purpose Inputs
User RAM/Extended ESC features		
0x0F80	128	User RAM/Extended ESC Features
Process Data RAM		
0x1000	4	Digital I/O Input Data
0x1000	8KB	Process Data RAM
Function Register Mirror (Refer to Section 3.3.2)		
Write / Read		
0x3000	2	Motor Control Register
0x3002	2	PWM Pulse X Configure Register
0x3004	2	PWM Trigger A Pulse Position Register
0x3006	2	PWM Trigger B Pulse Position Register
0x3008	2	PWM Period Cycle Register
0x300A	2	PWM Pulse Break Before Make Register
0x300C	2	PWM1Control Register
0x300E	2	PWM1 Counter Shift Register
0x3010	2	PWM1 High Pulse Width Register
0x3012	2	PWM2 Control Register
0x3014	2	PWM2 Shift Register
0x3016	2	PWM2 High Pulse Width Register
0x3018	2	PWM3 Control Register
0x301A	2	PWM3 Counter Shift Register
0x301C	2	PWM3 High Pulse Width Register
0x3020	4	Step Gap Time Register
0x3024	2	Step High Pulse Width Register
0x3026	2	Direction Transform Delay Step Register
0x3028	4	Step Target Number Register
0x302C	2	Step Configure Register
0x302E	2	Step Control Register
0x3040	4	Encoder Counter Value Register
0x3044	4	Encoder Constant Register
0x304C	2	Encoder Mode configuration Register
0x304E	2	Encoder Clear Register
0x3060	4	Watchdog Timer Register
0x3064	2	Watchdog Control Register
0x3066	2	Watchdog Timer Peak Value Clear Register
0x3068	4	Watchdog Monitored Signals Polarity Register
0x306C	4	Watchdog Monitored Signals Mask Register
0x3070	4	Watchdog Output Mask Register
0x3074	4	Watchdog Output Enable Register
0x3078	4	Watchdog Output Polarity Register
0x3080	2	SPI Configure Register
0x3082	2	SPI Baud Rate Register
0x3084	2	SPI Delay Byte and SS Register
0x3086	2	SPI Delay Transfer Register
0x3088	2	SPI RDY / Pulse Time Register
0x308A	2	SPI LDAC Time Register
0x308C	2	SPI Pulse/ RDY/ LDAC Register
0x3090	2	SPI 0/1 Byte Count Register
0x3092	2	SPI 2/3 Byte Count Register
0x3094	2	SPI 4/5 Byte Count Register
0x3096	2	SPI 6/7 Byte Count Register
0x3098	2	SPI 0/1/2/3 slave Select Register

0x309A	2	SPI 4/5/6/7 slave Select Register
0x30B0	8	SPI Channel 0 Data Register
0x30B8	8	SPI Channel 1 Data Register
0x30C0	8	SPI Channel 2 Data Register
0x30C8	8	SPI Channel 3 Data Register
0x30D0	8	SPI Channel 4 Data Register
0x30D8	8	SPI Channel 5 Data Register
0x30E0	8	SPI Channel 6 Data Register
0x30E8	8	SPI Channel 7 Data Register
0x30F2	2	SPI Master Control Register
0x3100	2	Interrupt Configure Register
0x3102	2	Interrupt Status Register
Read Only		
0x3230	4	Step Counter Content Register
0x3248	4	Encoder Latched Register
0x3250	2	Hall State Register
0x327C	4	Watchdog Timer Peak Value Register
0x32A8	2	SPI Interrupt Status Register
0x32AA	2	SPI Timeout Status Register
0x32AC	2	SPI Pulse Overrun Status Register
0x32AE	2	SPI Data Status Register
0x32B0	8	SPI Channel 0 Data Register
0x32B8	8	SPI Channel 1 Data Register
0x32C0	8	SPI Channel 2 Data Register
0x32C8	8	SPI Channel 3 Data Register
0x32D0	8	SPI Channel 4 Data Register
0x32D8	8	SPI Channel 5 Data Register
0x32E0	8	SPI Channel 6 Data Register
0x32E8	8	SPI Channel 7 Data Register
0x32F0	2	SPI Data Status Mirror Register

Table 3-2: ESC Memory Map

3.3.2 Function Register Map

Address Offset	Name	Description
0x000	MCTLR	Motor Control Register
0x002	PXCFGR	PWM Pulse X Configure Register
0x004	PTAPPR	PWM Trigger A Pulse Position Register
0x006	PTBPPR	PWM Trigger B Pulse Position Register
0x008	PPCR	PWM Period Cycle Register
0x00A	PBBMR	PWM Pulse Break Before Make Register
0x00C	P1CTRLR	PWM1Control Register
0x00E	P1SHR	PWM1 Counter Shift Register
0x010	P1HPWR	PWM1 High Pulse Width Register
0x012	P2CTRLR	PWM2 Control Register
0x014	P2SHR	PWM2 Shift Register
0x016	P2HPWR	PWM2 High Pulse Width Register
0x018	P3CTRLR	PWM3 Control Register
0x01A	P3SHR	PWM3 Counter Shift Register
0x01C	P3HPWR	PWM3 High Pulse Width Register
0x020	SGTLR	Step Gap Time Low Register
0x022	SGTHR	Step Gap Time High Register
0x024	SHPWR	Step High Pulse Width Register
0x026	TDLYR	direction Transform Delay step Register
0x028	STNLR	Step Target Number Low Word Register
0x02A	STNHR	Step Target Number High Word Register
0x02C	SCFGR	Step Configure Register
0x02E	SCTRLR	Step Control Register
0x030	SCNTLR	Step Counter Content Low Register
0x032	SCNTHR	Step Counter Content High Register
0x040	ECNTVLR	Encoder Counter value Low Register
0x042	ECNTVHR	Encoder Counter value High Register
0x044	ECNSTLR	Encoder Constant Low Register
0x046	ECNSTHR	Encoder Constant High Register
0x048	ELATLR	Encoder Latched Low Register
0x04A	ELATHR	Encoder Latched High Register
0x04C	EMODR	Encoder Mode Configuration Register
0x04E	ECLRR	Encoder Clear Register
0x050	HALSTR	Hall State Register
0x060	WTLR	Watchdog Timer Low Register
0x062	WTHR	Watchdog Timer High Register
0x064	WCFGR	Watchdog Configure Register
0x066	WTPVCR	Watchdog Timer Peak Value Clear Register
0x068	WMPLR	Watchdog Monitored Polarity Low Register
0x06A	WMPHR	Watchdog Monitored Polarity High Register
0x06C	WMMLR	Watchdog Monitored Mask Low Register
0x06E	WMMHR	Watchdog Monitored Mask High Register
0x070	WOMLR	Watchdog Output Mask Low Register
0x072	WOMHR	Watchdog Output Mask High Register
0x074	WOELR	Watchdog Output Enable Low Register
0x076	WOEHR	Watchdog Output Enable High Register
0x078	WOPLR	Watchdog Output Polarity Low Register
0x07A	WOPHR	Watchdog Output Polarity High Register
0x07C	WTPVLR	Watchdog Timer Peak Value Low Register
0x07E	WTPVHR	Watchdog Timer Peak Value High Register
0x080	SPICFGR	SPI Configure Register
0x082	SPIBRR	SPI Baud Rate Register

0x084	SPIDBSR	SPI Delay Byte and SS Register
0x086	SPIDTR	SPI Delay Transfer Register
0x088	SPIRPTR	SPI RDY / Pulse Time Register
0x08A	SPILTR	SPI LDAC Time Register
0x08C	SPIPRLR	SPI Pulse/ RDY/ LDAC Register
0x090	SPI01BCR	SPI 0/1 Byte Count Register
0x092	SPI23BCR	SPI 2/3 Byte Count Register
0x094	SPI45BCR	SPI 4/5 Byte Count Register
0x096	SPI67BCR	SPI 6/7 Byte Count Register
0x098	SPI03SSR	SPI 0/1/2/3 slave Select Register
0x09A	SPI47SSR	SPI 4/5/6/7 slave Select Register
0x0A8	SPINTSR	SPI Interrupt Status Register
0x0AA	SPITSR	SPI Timeout Status Register
0x0AC	SPIPOSR	SPI Pulse Overrun Status Register
0x0AE	SPIDSR	SPI Data Status Register
0x0B0	SPIC0DR	SPI Channel 0 Data Register
0x0B8	SPIC1DR	SPI Channel 1 Data Register
0x0C0	SPIC2DR	SPI Channel 2 Data Register
0x0C8	SPIC3DR	SPI Channel 3 Data Register
0x0D0	SPIC4DR	SPI Channel 4 Data Register
0x0D8	SPIC5DR	SPI Channel 5 Data Register
0x0E0	SPIC6DR	SPI Channel 6 Data Register
0x0E8	SPIC7DR	SPI Channel 7 Data Register
0x0F0	SPIDSMR	SPI Data Status Mirror Register
0x0F2	SPIMCR	SPI Master Control Register
0x100	INTCR	Interrupt Configure Register
0x102	INTSR	Interrupt Status Register
0x104	ESTOR	ESC State Override register
0x106	HSTSR	Host interface Status Register
Others	Reserved	Reserved

Table 3-3: Function Register Map

3.3.3 Memory Map between ESC Memory and Function Registers

Function Address	ESC Address		Name	Description
	R/W	RO		
0x000	0x3000	-	MCTLR	Motor Control Register
0x002	0x3002	-	PXCFGR	PWM Pulse X Configure Register
0x004	0x3004	-	PTAPPR	PWM Trigger A Pulse Position Register
0x006	0x3006	-	PTBPPR	PWM Trigger B Pulse Position Register
0x008	0x3008	-	PPCR	PWM Period Cycle Register
0x00A	0x300A	-	PBBMR	PWM Pulse Break Before Make Register
0x00C	0x300C	-	P1CTRLR	PWM1Control Register
0x00E	0x300E	-	P1SHR	PWM1 Counter Shift Register
0x010	0x3010	-	P1HPWR	PWM1 High Pulse Width Register
0x012	0x3012	-	P2CTRLR	PWM2 Control Register
0x014	0x3014	-	P2SHR	PWM2 Shift Register
0x016	0x3016	-	P2HPWR	PWM2 High Pulse Width Register
0x018	0x3018	-	P3CTRLR	PWM3 Control Register
0x01A	0x301A	-	P3SHR	PWM3 Counter Shift Register
0x01C	0x301C	-	P3HPWR	PWM3 High Pulse Width Register
0x020	0x3020	-	SGTLR	Step Gap Time Low Register
0x022			SGTHR	Step Gap Time High Register
0x024	0x3024	-	SHPWR	Step High Pulse Width Register
0x026	0x3026	-	TDLYR	direction Transform Delay step Register
0x028	0x3028	-	STNLR	Step Target Number Low Word Register
0x02A			STNHR	Step Target Number High Word Register
0x02C	0x302C	-	SCFGR	Step Configure Register
0x02E	0x302E	-	SCTRLR	Step Control Register
0x030	-	0x3230	SCNTLR	Step Counter Content Low Register
0x032			SCNTHR	Step Counter Content High Register
0x040	0x3040	-	ECNTVLR	Encoder Counter value Low Register
0x042			ECNTVHR	Encoder Counter value High Register
0x044	0x3044	-	ECNSTLR	Encoder Constant Low Register
0x046			ECNSTHR	Encoder Constant High Register
0x048	-	0x3248	ELATLR	Encoder Latched Low Register
0x04A			ELATHR	Encoder Latched High Register
0x04C	0x304C	-	EMODR	Encoder Mode Configuration Register
0x04E	0x304E	-	ECLRR	Encoder Clear Register
0x050	-	0x3250	HALSTR	Hall State Register
0x060	0x3060	-	WTLR	Watchdog Timer Low Register
0x062			WTHR	Watchdog Timer High Register
0x064	0x3064	-	WCFGR	Watchdog Configure Register
0x066	0x3066	-	WTPVCR	Watchdog Timer Peak Value Clear Register
0x068	0x3068	-	WMPLR	Watchdog Monitored Polarity Low Register
0x06A			WMPHR	Watchdog Monitored Polarity High Register
0x06C	0x306C	-	WMMLR	Watchdog Monitored Mask Low Register
0x06E			WMMHR	Watchdog Monitored Mask High Register
0x070	0x3070	-	WOMLR	Watchdog Output Mask Low Register
0x072			WOMHR	Watchdog Output Mask High Register
0x074	0x3074	-	WOELR	Watchdog Output Enable Low Register
0x076			WOEHR	Watchdog Output Enable High Register
0x078	0x3078	-	WOPLR	Watchdog Output Polarity Low Register
0x07A			WOPHR	Watchdog Output Polarity High Register
0x07C	-	0x327C	WTPVLR	Watchdog Timer Peak Value Low Register
0x07E			WTPVHR	Watchdog Timer Peak Value High Register
0x080	0x3080	-	SPICFGR	SPI Configure Register
0x082	0x3082	-	SPIBRR	SPI Baud Rate Register

0x084	0x3084	-	SPIDBSR	SPI Delay Byte and SS Register
0x086	0x3086	-	SPIDTR	SPI Delay Transfer Register
0x088	0x3088	-	SPIRPTR	SPI RDY / Pulse Time Register
0x08A	0x308A	-	SPILTR	SPI LDAC Time Register
0x08C	0x308C	-	SPIPRLR	SPI Pulse/ RDY/ LDAC Register
0x090	0x3090	-	SPI01BCR	SPI 0/1 Byte Count Register
0x092	0x3092	-	SPI23BCR	SPI 2/3 Byte Count Register
0x094	0x3094	-	SPI45BCR	SPI 4/5 Byte Count Register
0x096	0x3096	-	SPI67BCR	SPI 6/7 Byte Count Register
0x098	0x3098	-	SPI03SSR	SPI 0/1/2/3 slave Select Register
0x09A	0x309A	-	SPI47SSR	SPI 4/5/6/7 slave Select Register
0x0A8	-	0x32A8	SPINTSR	SPI Interrupt Status Register
0x0AA	-	0x32AA	SPITSR	SPI Timeout Status Register
0x0AC	-	0x32AC	SPIPOSR	SPI Pulse Overrun Status Register
0x0AE	-	0x32AE	SPIDSR	SPI Data Status Register
0x0B0	0x30B0	0x32B0	SPIC0DR	SPI Channel 0 Data Register
0x0B8	0x30B8	0x32B8	SPIC1DR	SPI Channel 1 Data Register
0x0C0	0x30C0	0x32C0	SPIC2DR	SPI Channel 2 Data Register
0x0C8	0x30C8	0x32C8	SPIC3DR	SPI Channel 3 Data Register
0x0D0	0x30D0	0x32D0	SPIC4DR	SPI Channel 4 Data Register
0x0D8	0x30D8	0x32D8	SPIC5DR	SPI Channel 5 Data Register
0x0E0	0x30E0	0x32E0	SPIC6DR	SPI Channel 6 Data Register
0x0E8	0x30E8	0x32E8	SPIC7DR	SPI Channel 7 Data Register
0x0F0	-	0x32F0	SPIDSMR	SPI Data Status Mirror Register
0x0F2	0x30F2	-	SPIMCR	SPI Master Control Register
0x100	0x3100	-	INTCR	Interrupt Configure Register
0x102	0x3102	-	INTSR	Interrupt Status Register

Table 3-4: ESC Memory and Function Registers Mirror Mapping Table

4 Electrical Specifications

4.1 DC Characteristics

4.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VCCK	Digital core power supply	- 0.5 to 1.6	V
VCC3IO, VCC33A	Power supply of 3.3V I/O and Ethernet PHY	- 0.5 to 4.6	V
VCC12A_PLL	Analog power supply for PLL	- 0.5 to 1.6	V
V_{IN}	Input voltage of 3.3V I/O with 5V tolerant.	- 0.5 to 5.8	V
T_{STG}	Storage temperature.	- 65 to 150	℃
I_{IN}	DC input current.	50	mA
I_{OUT}	Output short circuit current.	50	mA

Note:
Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted in the recommended operating condition section of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

4.1.2 Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Units
VCC3IO	Power supply of 3.3V I/O	2.97	3.3	3.63	V
VCC33A	Analog power supply for Ethernet PHY	2.97	3.3	3.63	V
VCCK	Digital core power supply	1.08	1.2	1.32	V
VCC12A_PLL	Analog power supply for PLL	1.08	1.2	1.32	V
Tj	operating junction temperature	-40	25	125	℃
Ta	operating ambient temperature	-40	-	105	℃

4.1.3 Leakage Current and Capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IN}	Input leakage current. No pull-up or pull-down.	3.3V with 5V tolerant I/O pins. Vin = 5 or 0V.	-	< ±1	-	μA
C_{IN}	Input capacitance.	3.3V with 5V tolerant I/O pins.	-	2.3	-	pF

4.1.4 DC Characteristics of 3.3V with 5V Tolerant I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCC3IO	Power supply of 3.3V I/O.	3.3V I/O	2.97	3.3	3.63	V
Vil	Input low voltage.	LVTTL	-	-	0.8	V
Vih	Input high voltage.		2.0	-	-	V
Vt-	Schmitt trigger negative going threshold voltage.	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage.	Iol = 4 ~ 8mA	-	-	0.4	V
Voh	Output high voltage.	Ioh = 4 ~ 8mA	2.4	-	-	V
Vopu (1)	Output pull-up voltage for 5V tolerant IO	With internal pull-up resistor	VCC3IO – 0.9	-	-	V
Rpu	Input pull-up resistance.		40	75	190	KΩ
Rpd	Input pull-down resistance.		40	75	190	KΩ
Iin	Input leakage current.	Vin = 5 or 0V	-	±1	-	μA
	Input leakage current with pull-up resistance.	Vin = 0 V	-	-45	-	μA
	Input leakage current with pull-down resistance.	Vin = VCC3IO	-	45	-	μA

Note: This parameter indicates that the pull-up resistor for the 5V tolerant I/O pins cannot reach VCC3IO DC level even without DC loading current.

4.2 Power Consumption

Item	Conditions	VCCIO + VCC33A	VCCK + VCC12A_PLL	Units
Digital IO (32 I/O Output)	Power on, Unlinked (Typ.)	120	33	mA
	INIT state, Linked (Typ.)	135	48	mA
	OP state, Linked (Typ.)	160	50	mA

Note: Above current value are typical values measured on AX58100 Test board.

Table 4-1: AX58100 Power Consumption

Symbol	Description	Condition	Min	Typ	Max	Unit
Θ_{JC}	Thermal resistance of junction to case		-	16	-	°C/W
Θ_{JA}	Thermal resistance of junction to ambient	Still air	-	28.3	-	°C/W
Ψ_{JT}	Junction to Top of the Package Characterization Parameter		-	1.49	-	°C/W

Table 4-2: Thermal Characteristics

4.3 Power-On-Reset (POR) Specification

Below figures and table show the two POR circuit spec during power ramp-up/down.

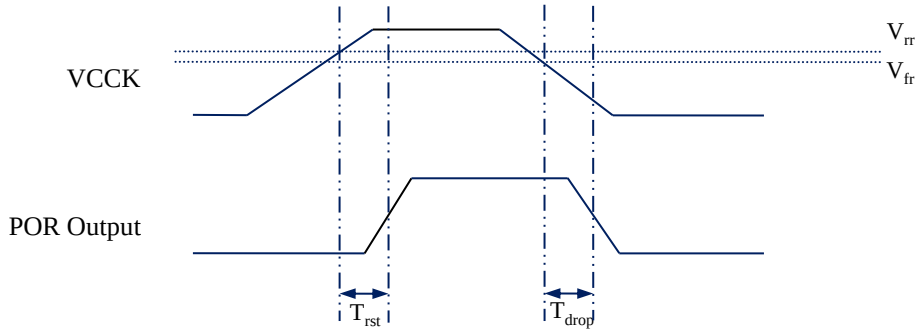


Figure 4-1: Power On Reset (POR) Timing Diagram

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
VCCK	Power supply voltage to be detected	-	1.0	1.2	1.32	V
V_{rr}	VCCK rise relax voltage	-	-	0.72	0.9	V
V_{fr}	VCCK fall release voltage	-	-	0.63	0.85	V
T_{rst}	Reset time after POR trigger up	VCCK slew rate = 1.0V / 1µs	1.8	2.5	4.8	µs
T_{drop}	Drop time of VCCK to reset	VCCK slew rate = 2.5V / 1µs	0.2	0.4	0.9	µs

Table 4-3: Power On Reset (POR) Timing Table

4.4 Power–up Sequence

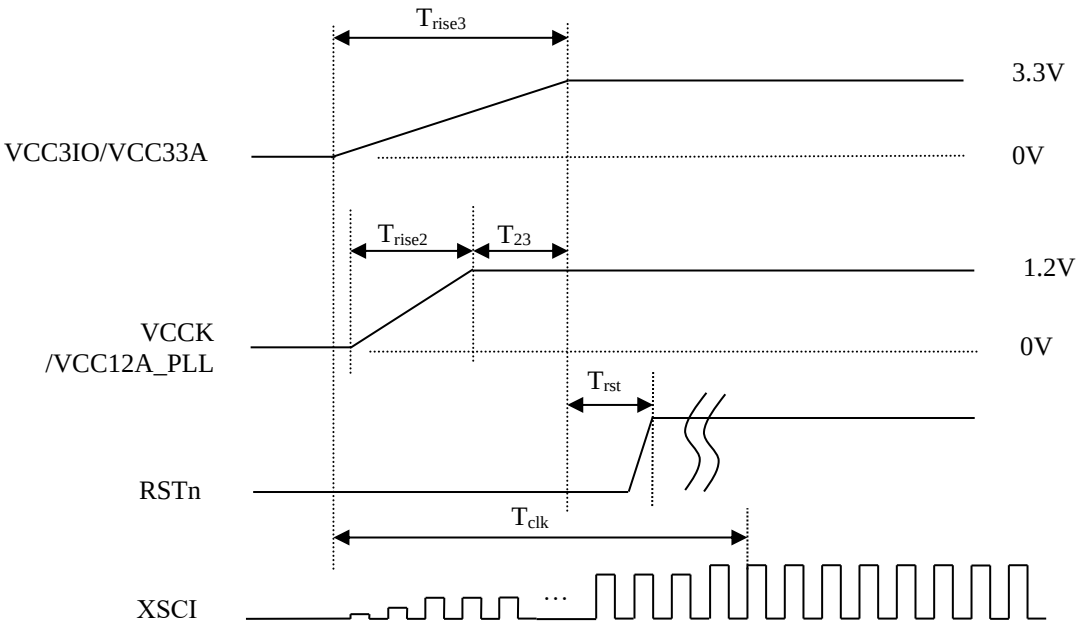


Figure 4-2: Power-up Sequence Timing Diagram

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{rise3}	3.3V power supply rise time.	From 0V to 3.3V.	-	400	-	us
T_{rise2}	1.2V power supply rise time.	From 0V to 1.2V.	-	200	-	us
T_{23}	VCCK rising to 1.2V to VCC3IO rising to 3.3V interval.		-	200	-	us
T_{rst}	RSTn asserted low level interval.	From VCC3IO rising to 3.3V to RSTn going high.	-	40	-	us
T_{clk}	25MHz crystal oscillator start-up time.	From VCC3IO rising to 3.3V to clock stable of 25MHz crystal oscillator.	-	-	60	ms
$T_{Startup}$	Startup time	PDI operational after power good, without I2C EEPROM loading error	-	-	70	ms

Note: The above typical timing data is measured from AX58100 test board.

Table 4-4: Power-up Sequence Timing Table

4.5 AC Timing Characteristics

4.5.1 I²C Timing

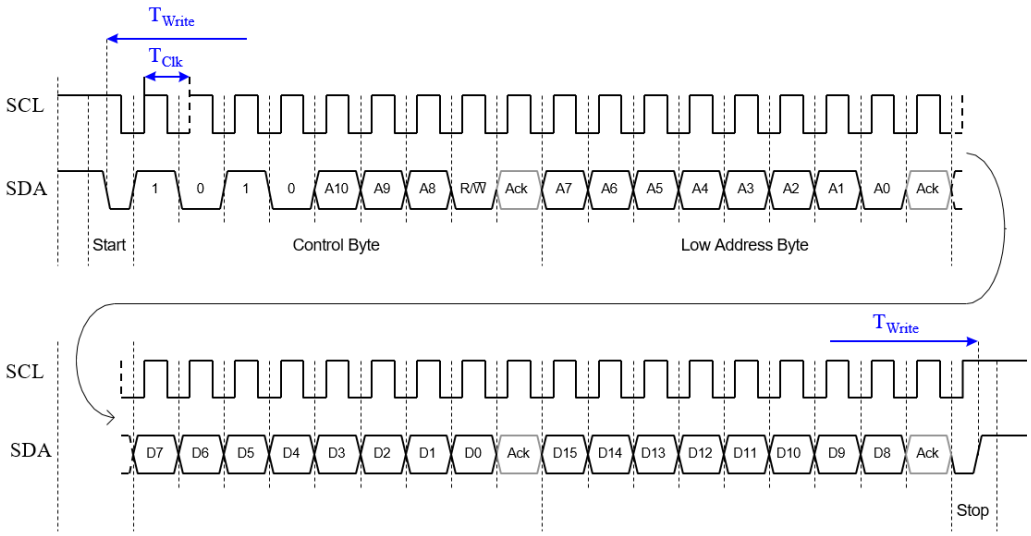


Figure 4-3: Write access (1 address byte, up to 16 Kbit EEPROMs)

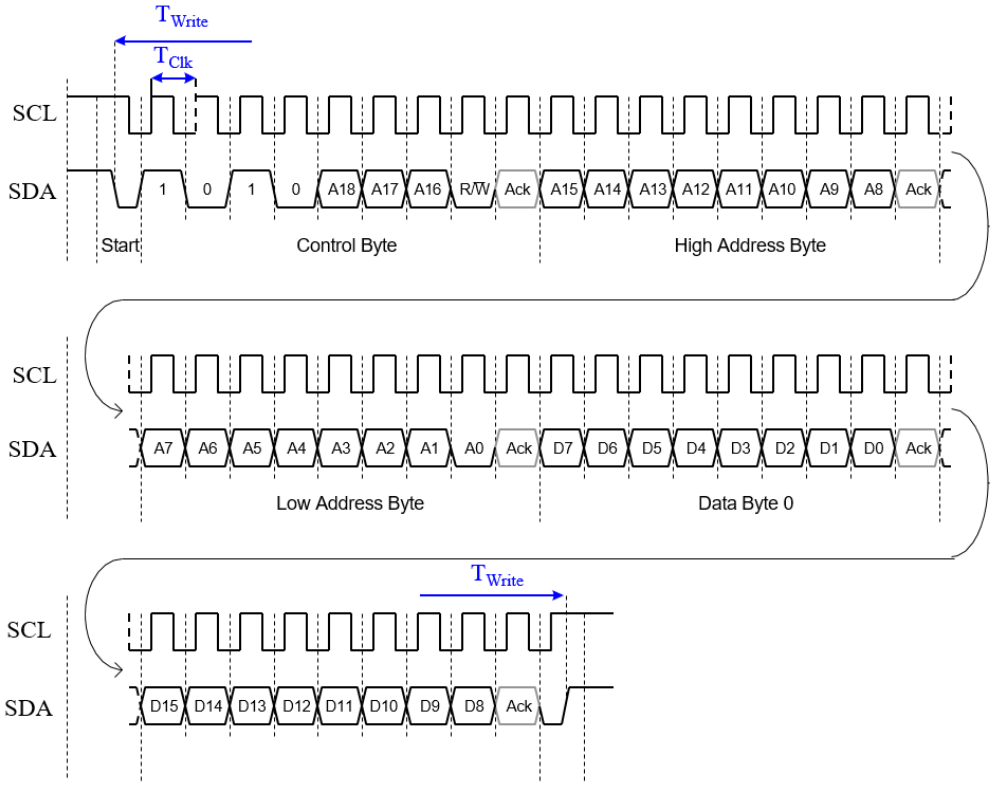


Figure 4-4: Write access (2 address bytes, 32 Kbit - 4 Mbit EEPROMs)

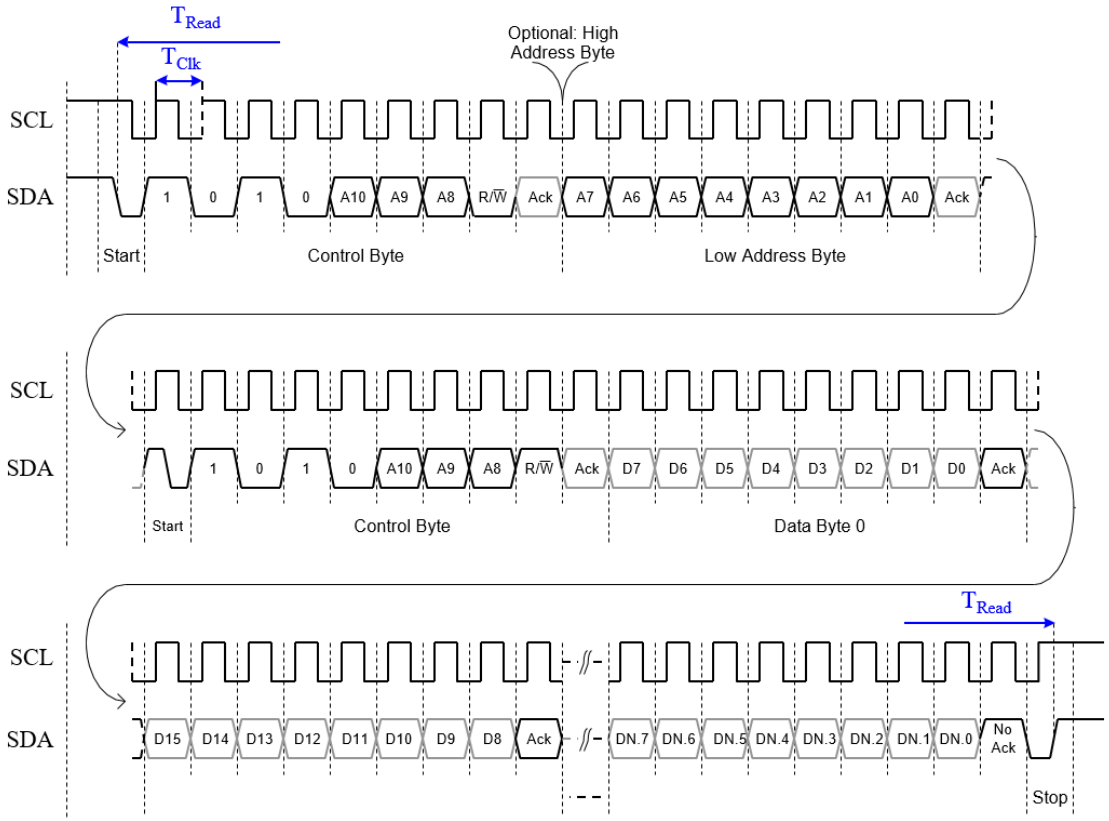


Figure 4-5: Read access (1 address byte, up to 16 Kbit EEPROMs)

Symbol	Parameter		Typical		Units
			Up to 16 Kbit	32 Kbit-4 Mbit	
T_{Clk}	EEPROM clock period		6.72 (≈ 150 KHz)		us
T_{Write}	Write access time (without errors)		250	310	us
T_{Read}	Read access time (without errors):	2 words	440	500	us
		configuration (8 Words)	1.16	1.22	ms
T_{Delay}	Time until configuration loading begins after Reset is gone		65.5		us

Table 4-5: I²C EEPROM Timing Table

4.5.2 Port 2 MII Timing

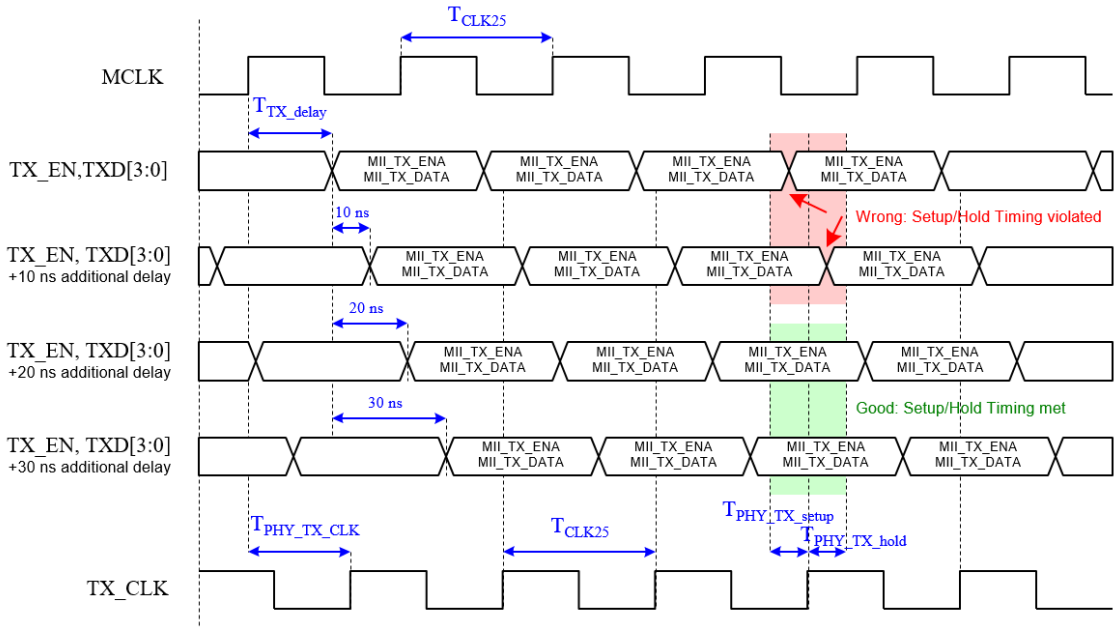


Figure 4-6: Port 2 MII TX Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{CLK25}	MCLK output	-	40	-	ns
T_{TX_delay}	TX_EN/TXD[3:0] delay after rising edge of MCLK	-	-	2	ns
$T_{PHY\_TX\_CLK}$	Delay between MCLK and TX_CLK output of the PHY	-	PHY dependent	-	ns
$T_{PHY\_TX\_setup}$	PHY setup time	PHY dependent	-	-	ns
$T_{PHY\_TX\_hold}$	PHY hold time	PHY dependent	-	-	ns

Table 4-6: Port 2 MII TX Timing Table

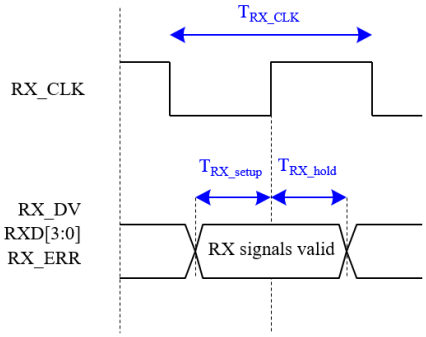


Figure 4-7: Port 2 MII RX Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{RX_CLK}	RX_CLK period (100 PPM with maximum FIFO Size only)	-	40	-	ns
T_{RX_setup}	RX_DV/RX_ER/RXD[3:0] valid before rising edge of RX_CLK	2.1	-	-	ns
T_{RX_hold}	RX_DV/RX_ER/RXD[3:0] valid after rising edge of RX_CLK	0.5	-	-	ns

Table 4-7: Port 2 MII RX Timing Table

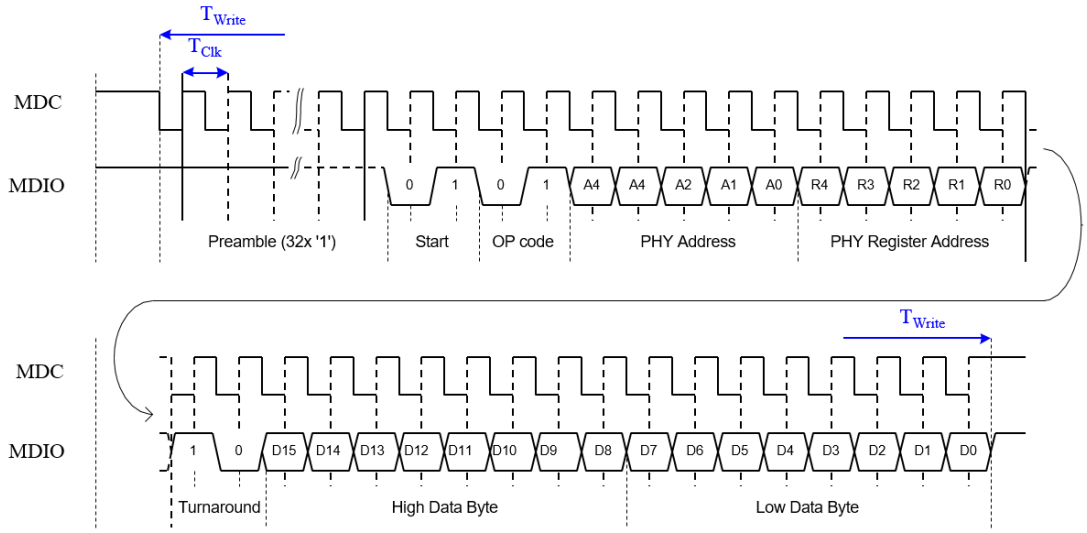


Figure 4-8: MDC/MDIO Write access

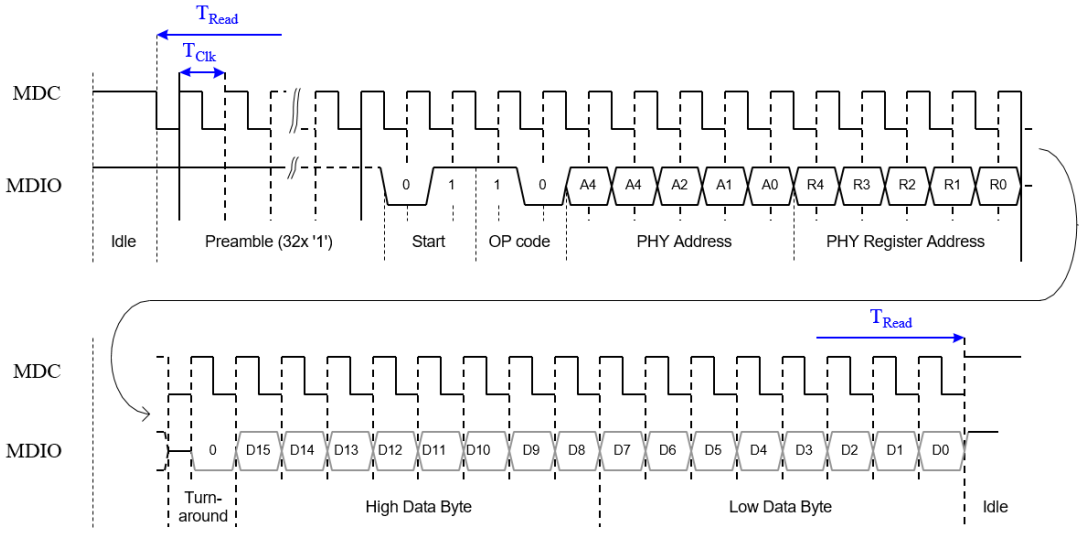


Figure 4-9: MDC/MDIO Read access

Symbol	Description	Min	Typ	Max	Units
T_{MDC}	MDC period		400 (≈ 2.5 MHz)		ns
T_{Write}	MI Write access time		25.6		us
T_{Read}	MI Read access time		25.4		us
$T_{MI\_startup}$	Time between reset end and the first access of MI Link detection and configuration		1.34		ms

Table 4-8: MDC/MDIO Timing Table

4.5.3 Distributed Clocks SYNC/LATCH

Symbol	Description	Min	Typ	Max	Units
T_{DC_LATCH}	Time between LATCH 0/1 events	12			ns
$T_{DC\_SYNC\_Jitter}$	SYNC 0/1 output jitter			12	ns

Table 4-9: DC SYNC/LATCH timing characteristics

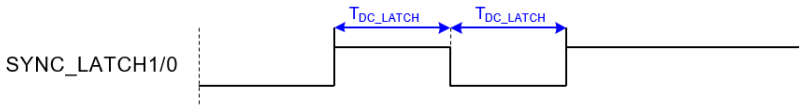


Figure 4-10: LATCH timing

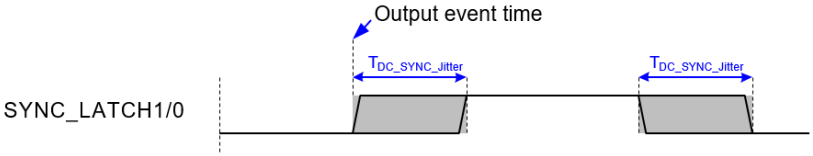


Figure 4-11: SYNC timing

4.5.4 Digital I/O Timing

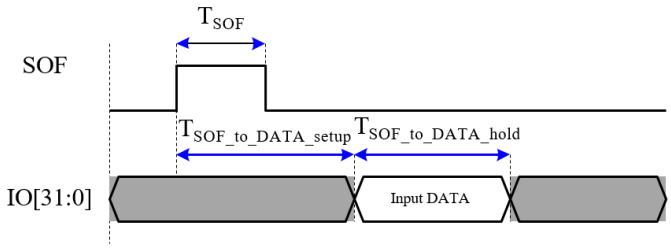


Figure 4-12: Digital Input: Input data sampled at SOF, IO can be read in the same frame

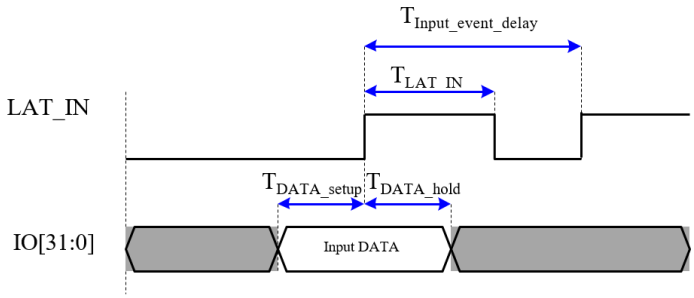


Figure 4-13: Digital Input: Input data sampled with LATCH_IN

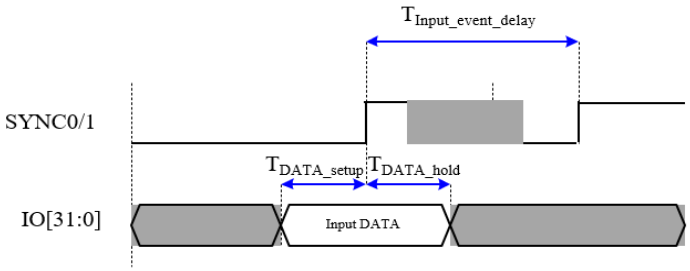


Figure 4-14: Digital Input: Input data sampled with SYNC0/1

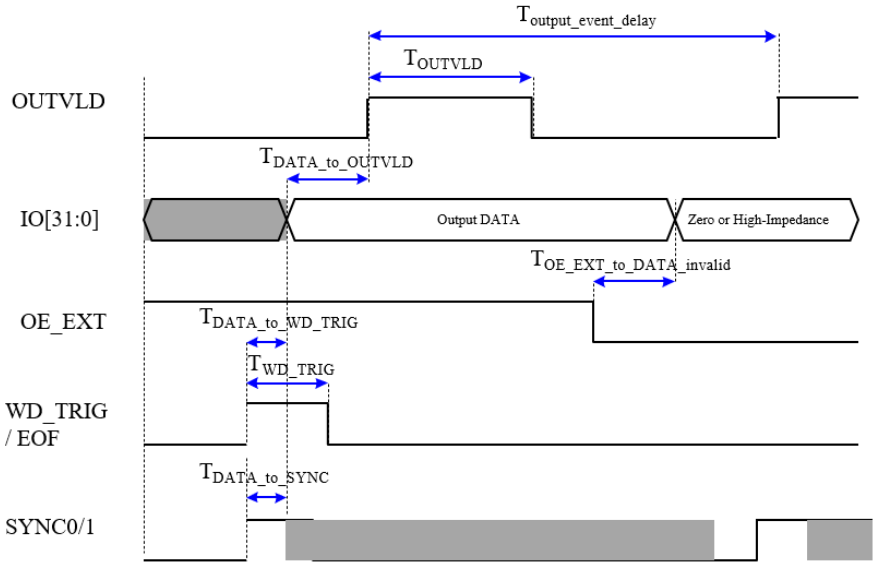


Figure 4-15: Digital Output timing

Symbol	Description	Min	Typ	Max	Units
T_{DATA_setup}	Input data valid before LAT_IN	5	-	-	ns
T_{DATA_hold}	Input data valid after LAT_IN	2	-	-	ns
T_{LAT_IN}	LAT_IN high time	4	-	-	ns
T_{SOF}	SOF high time	-	40	-	ns
$T_{SOF\_to\_DATA\_setup}$	Input data valid after SOF, so that Inputs can be read in the same frame	0	-	1.2	us
$T_{SOF\_to\_DATA\_hold}$	Input data invalid after SOF	1.6	-	-	us
$T_{input\_event\_delay}$	Time between consecutive input events	440	-	-	ns
T_{OUTVLD}	OUTVLD high time	-	80	-	ns
$T_{DATA\_to\_OUTVLD}$	Output data valid before OUTVLD	79	-	-	ns
T_{WD_TRIG}	WD_TRIG high time	-	40	-	ns
$T_{DATA\_to\_WD\_TRIG}$	Output data valid after WD_TRIG	-	-	20	ns
$T_{DATA\_to\_EOF}$	Output data valid after EOF	-	-	20	ns
$T_{DATA\_to\_SYNC}$	Output data valid after SYNC0/1	-	-	20	ns
$T_{OE\_EXT\_to\_DATA\_invalid}$	Outputs zero or Outputs hi-Z after OE_EXT set to low	0	-	9.5	ns
$T_{output\_event\_delay}$	Time between consecutive output events	320	-	-	ns
$T_{OUT\_EXT\_valid}$	OUT_EXT valid before OUTVLD	-	80	-	ns
$T_{OUT\_EXT\_invalid}$	OUT_EXT invalid after OUTVLD	-	80	-	ns

Table 4-10: Digital I/O timing Table

4.5.5 ESC PDI SPI Slave Timing

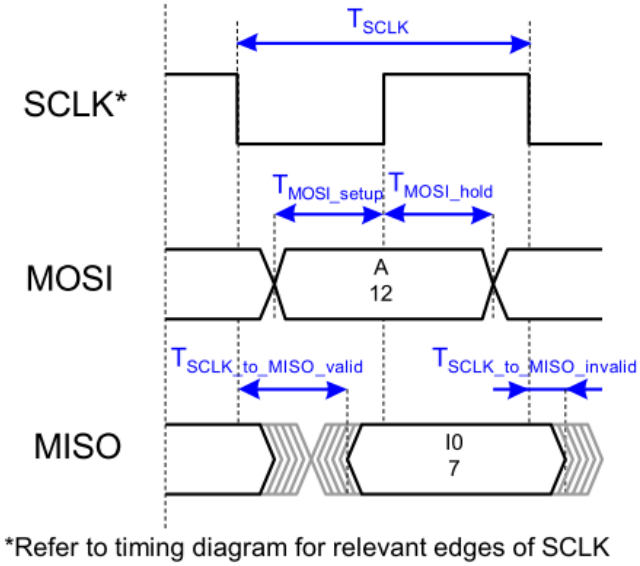


Figure 4-16: Basic MOSI/MISO timing

Symbol	Description		Min	Typ	Max	Units
T_{SCLK}	SCLK Period		33 (≤30MHz)	-	-	ns
$T_{SEL\_to\_CLK}$	First SCLK cycle after SCS_ESC asserted		5	-	-	ns
$T_{CLK\_to\_SEL}$	Deassertion of SCS_ESC after last SCLK cycle	SPI mode 0/2, SPI mode 1/3 with normal data out sample	5	-	-	ns
		SPI mode 1/3 with late data out sample	T_{CLK}/2+ 5			
T_{read}	Only for read access between address/command and first data byte. Can be ignored if BUSY or Wait State Bytes are used.		240	-	-	ns
T_{access_delay}	Delay between SPI accesses		40	-	-	ns
T_{MOSI_setup}	MOSI valid before SCLK edge		3	-	-	ns
T_{MOSI_hold}	MOSI valid after SCLK edge		0	-	-	ns
$T_{SCLK\_to\_MISO\_valid}$	MISO valid after SCLK edge		-	-	10.5	ns
$T_{SCLK\_to\_MISO\_invalid}$	MISO invalid after SCLK edge		0	-	-	ns
T_{IRQ_delay}	Internal delay between AL event and SINT output to enable correct reading of the interrupt registers.		-	180	-	ns

Table 4-11: PDI SPI Slave Timing Table

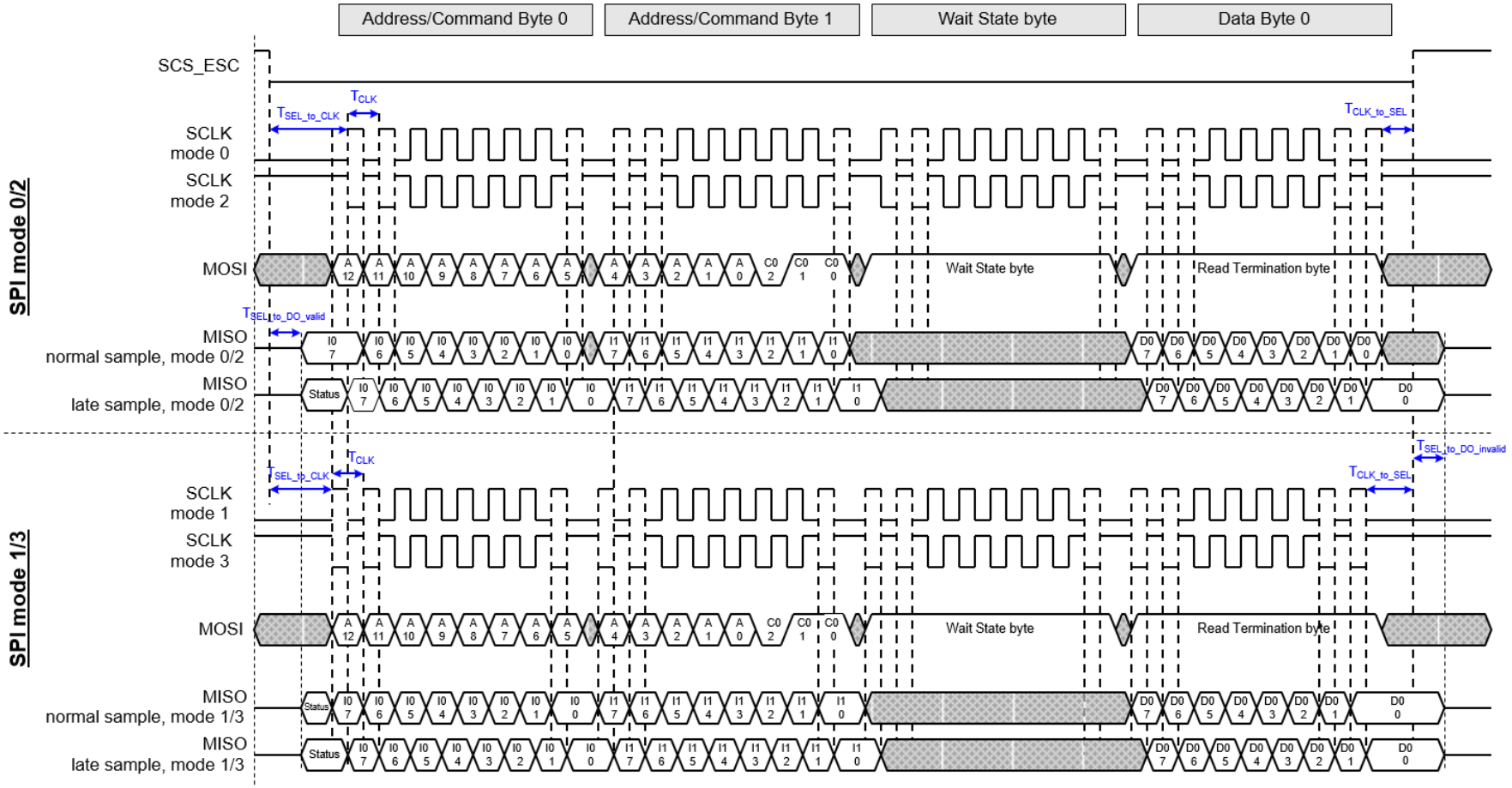


Figure 4-17: PDI SPI Slave read access (2 byte addressing, 1 byte read data) with Wait State byte

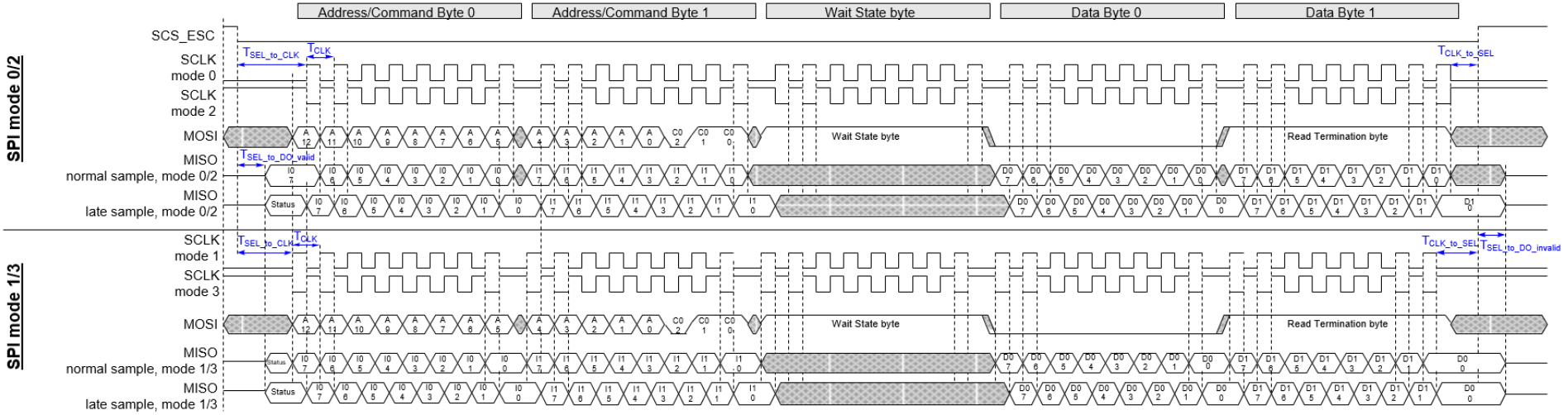


Figure 4-18: PDI SPI Slave read access (2 byte addressing, 2 byte read data) with Wait State byte

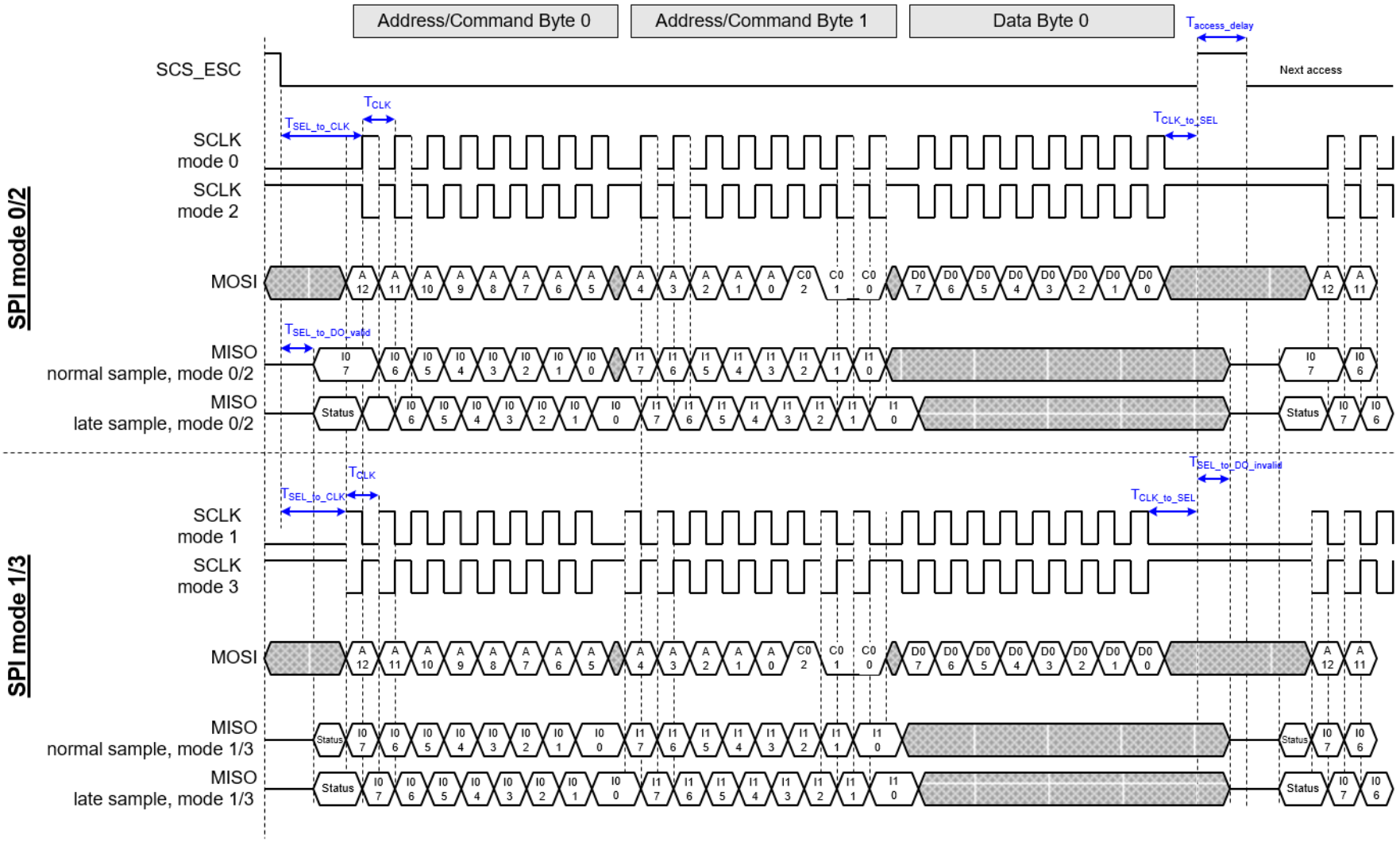


Figure 4-19: PDI SPI Slave write access (2 byte addressing, 1 byte write data)

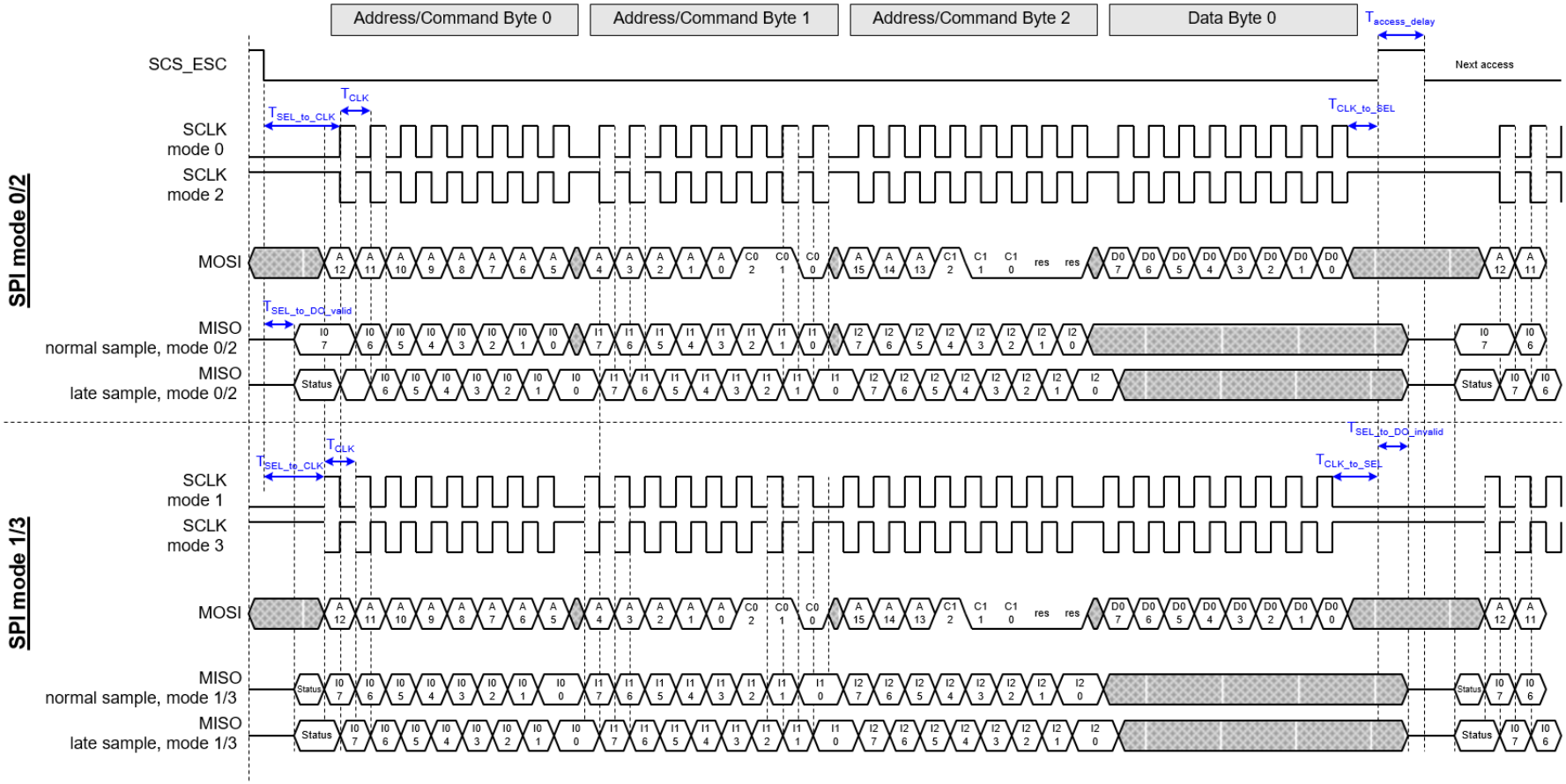


Figure 4-20: PDI SPI Slave write access (3 byte addressing, 1 byte write data)

4.5.6 Function SPI Slave Timing

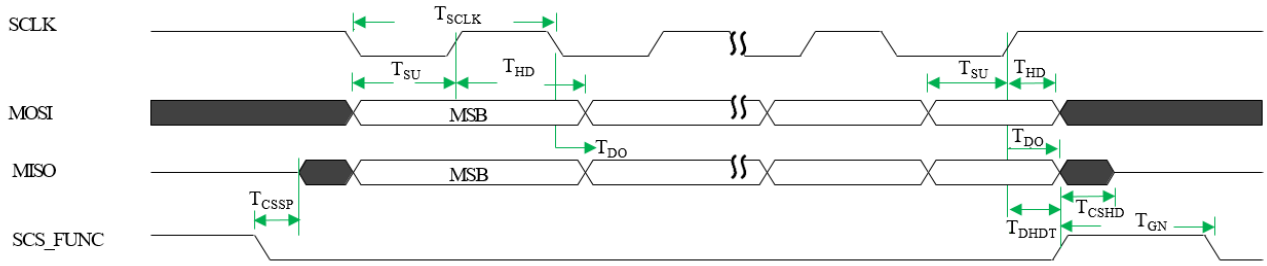


Figure 4-21: Function SPI Slave with share pin Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{SCLK}	SCLK clock frequency	-	-	50	MHz
T_{DO}	MISO data valid time after SCLK edge	9.2	-	-	ns
T_{SU}	MOSI data setup time before SCLK edge	2	-	-	ns
T_{HD}	MOSI data hold time after SCLK edge	2	-	-	ns
T_{CSSP}	SCS setup time before MISO active	7.6	-	-	ns
T_{DHD}	SCS hold time after SCLK edge	21	-	-	ns
T_{CSHD}	MISO data hold time after SCS de-assert	2.6	-	-	ns
T_{GN}	SCS negation to next SCS assertion time	40	-	-	ns

Table 4-12: Function SPI with share pin Timing Table

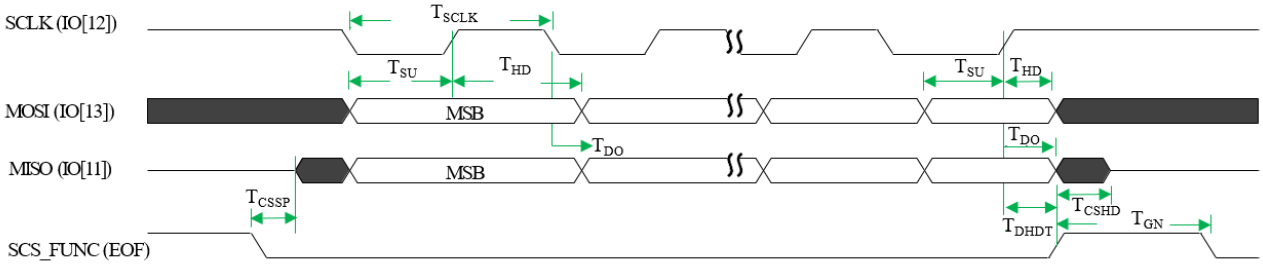


Figure 4-22: Function SPI Slave with individual pin Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{SCLK}	SCLK clock frequency	-	-	47	MHz
T_{DO}	MISO data valid time after SCLK edge	10.5	-	-	ns
T_{SU}	MOSI data setup time before SCLK edge	2	-	-	ns
T_{HD}	MOSI data hold time after SCLK edge	2	-	-	ns
T_{CSSP}	SCS setup time before MISO active	7.7	-	-	ns
T_{DHD}	SCS hold time after SCLK edge	21	-	-	ns
T_{CSHD}	MISO data hold time after SCS de-assert	2.5	-	-	ns
T_{GN}	SCS negation to next SCS assertion time	40	-	-	ns

Table 4-13: Function SPI with individual pin Timing Table

4.5.7 ESC PDI Local Bus Timing

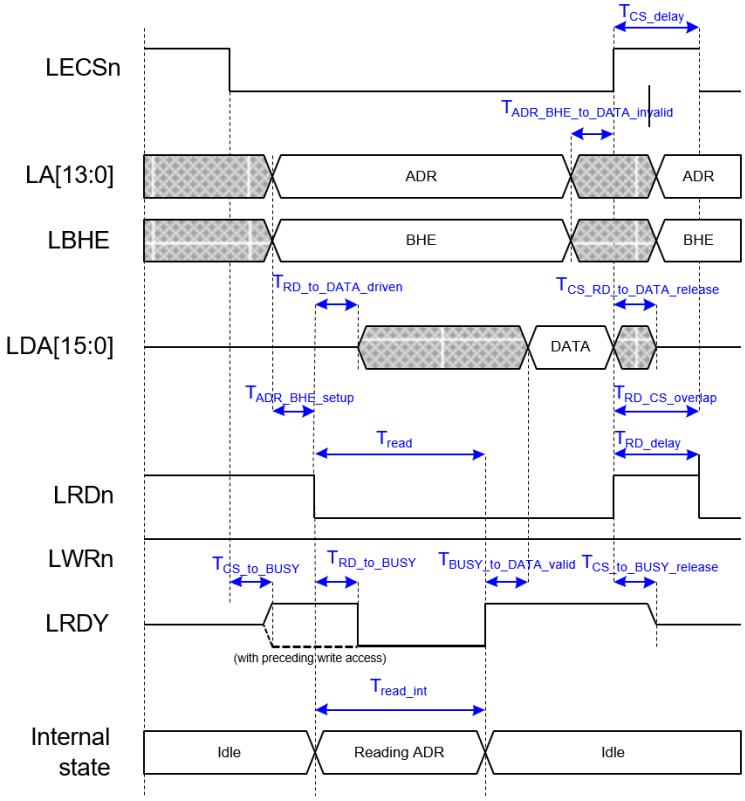


Figure 4-23: PDI Local Bus Read access (without preceding write access)

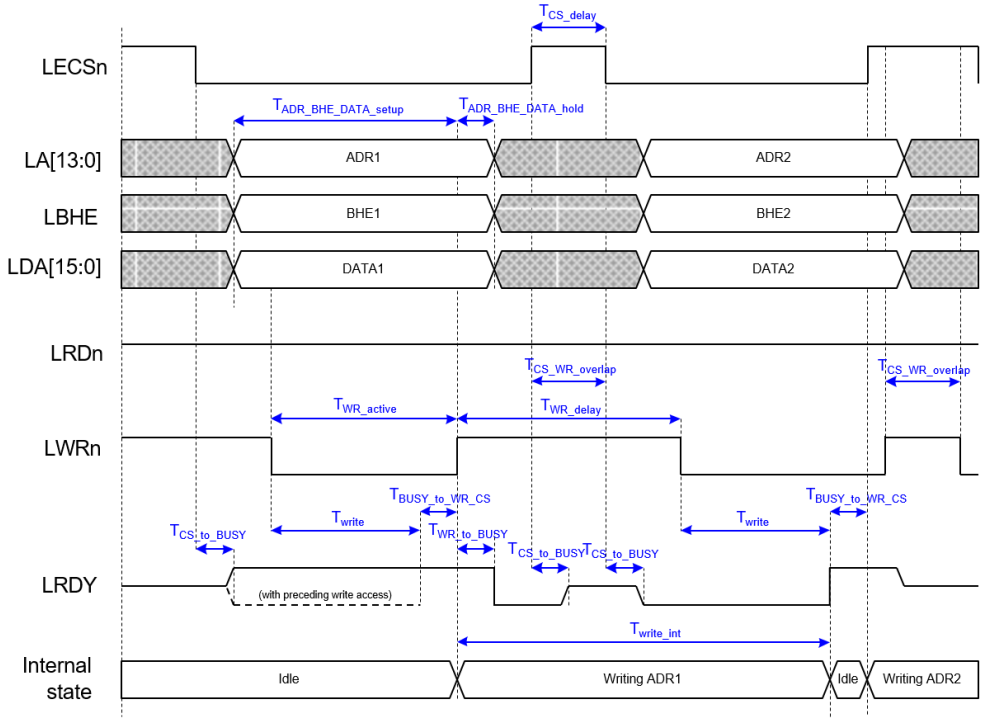


Figure 4-24: PDI Local Bus Write access (write after rising edge LWRn, without preceding write access)

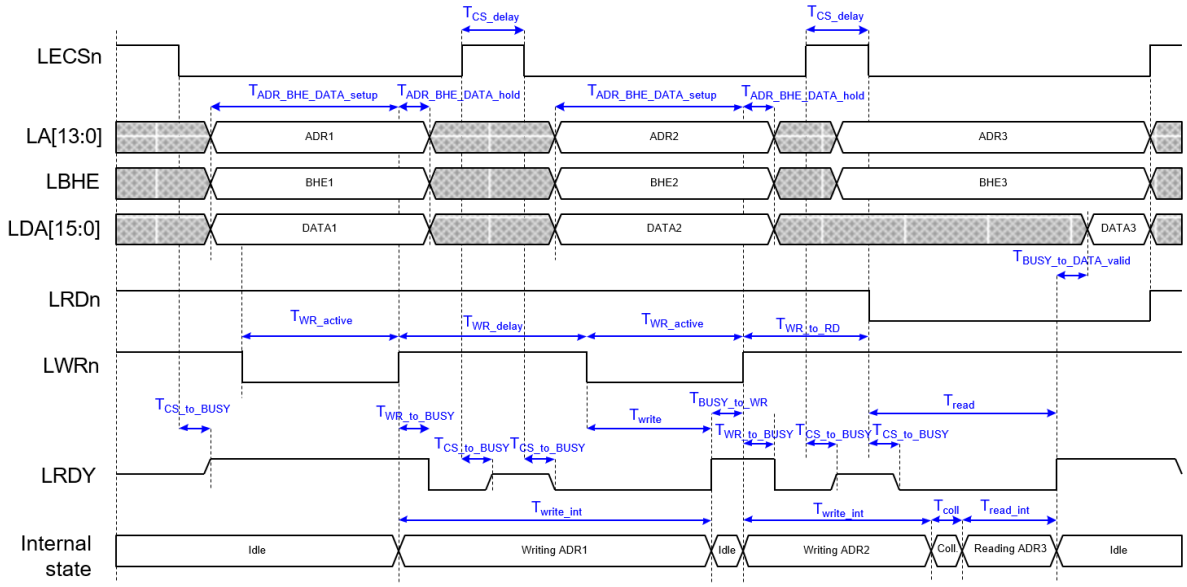


Figure 4-25: PDI Local Bus Sequence of two write accesses and a read access

Note: The first write access to ADR1 is performed after the first rising edge of WR. After that, the ESC is internally busy writing to ADR1. After CS is deasserted, BUSY is not driven any more, nevertheless, the ESC is still writing to ADR1.

Hence, the second write access to ADR2 is delayed because the write access to ADR1 has to be completed first. So, the second rising edge of WR must not occur before BUSY is gone. After the second rising edge of WR, the ESC is busy writing to ADR2. This is reflected with the BUSY signal as long as CS is asserted.

The third access in this example is a read access. The ESC is still busy writing to ADR2 while the falling edge of RD occurs. In this case, the write access to ADR2 is finished first, and afterwards, the read access to ADR3 is performed. The ESC signals BUSY during both write and read access

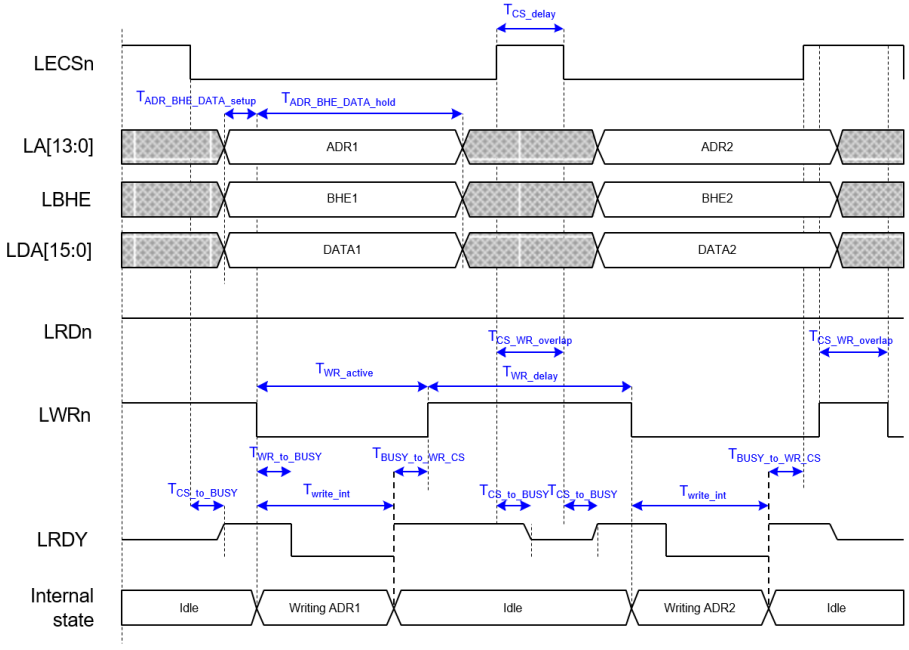


Figure 4-26: PDI Local Bus Write access (write after falling edge LWRn

Symbol	Description		Min	Typ	Max	Units
$T_{CS\_to\_BUSY}$	BUSY driven and valid after CS assertion		-	-	45	ns
$T_{ADR\_BHE\_setup}$	ADR and BHE valid before RD assertion		0	-	-	ns
$T_{RD\_to\_DATA\_driven}$	DATA bus driven after RD assertion		0	-	-	ns
$T_{RD\_to\_BUSY}$	BUSY asserted after RD assertion		0	-	10	ns
T_{read}	External read time (RD assertion to BUSY deassertion) with normal read busy output (0x0152[0]). Additional 20 ns if delayed read busy output is configured.					ns
	without preceding write access or $T_{WR\_to\_RD} \geq T_{prec\_write} + T_{Coll}$ or configuration: write after falling edge of WR		-	-	T_{read_int}	
	with preceding write access and $T_{WR\_to\_RD} < T_{prec\_write} + T_{Coll}$		-	-	$T_{read\_int} + T_{prec\_write} + T_{Coll} - T_{WR\_to\_RD}$	
	8-bit access, absolute worst case with preceding write access ($T_{WR\_to\_RD}$=min, T_{prec_write} =max, T_{Coll}=max)		-	-	420	
	16-bit access, absolute worst case with preceding write access ($T_{WR\_to\_RD}$=min, T_{prec_write} =max, T_{Coll}=max)		-	-	560	
T_{read_int}	Internal read time	8-bit access	-	-	220	ns
		16-bit access			300	
T_{prec_write}	Time for preceding write access	8-bit access	-	-	180	ns
		16-bit access			260	
$T_{BUSY\_to\_DATA\_valid}$	DATA bus valid after device BUSY is deasserted	normal read busy output	-	-	5	ns
		delayed read busy output			-15	
$T_{ADR\_BHE\_to\_DATA\_invalid}$	DATA invalid after ADR or BHE change		0	-	-	ns
$T_{CS\_RD\_to\_DATA\_release}$	DATA bus released after CS deassertion or RD deassertion		2.5	-	7.5	ns
$T_{CS\_to\_BUSY\_release}$	BUSY released after CS deassertion		2.5	-	8.5	ns
T_{CS_delay}	Delay between CS deassertion an assertion		5	-	-	ns
T_{RD_delay}	Delay between RD deassertion and assertion		5	-	-	ns
$T_{ADR\_BHE\_DATA\_setup}$	ADR, BHE and Write DATA valid before WR deassertion		6.5	-	-	ns
$T_{ADR\_BHE\_DATA\_hold}$	ADR, BHE and Write DATA valid after WR deassertion		2	-	-	ns
T_{WR_active}	WR assertion time		8.5	-	-	ns
$T_{BUSY\_to\_WR\_CS}$	WR or CS deassertion after BUSY deassertion		0	-	-	ns
$T_{WR\_to\_BUSY}$	BUSY assertion after WR deassertion		-	-	12	ns
T_{write}	External write time (WR assertion to BUSY deassertion)					ns
	Configuration: write after falling edge of WR (act. low)		0	-	T_{write_int}	

	with preceding write access and $T_{WR\_delay} < T_{write\_int}$ (Write after rising edge -of WR)			-	T_{write_int} - T_{WR_delay}	ns
	without preceding write access or $T_{WR\_delay} \geq T_{write\_int}$ (Write after rising edge of WR)			-	0	
	8-bit access, absolute worst case with preceding write access (T_{WR_delay}= min, T_{WR_int}=max, Write after rising edge of WR)			-	180	
	16-bit access, absolute worst case with preceding write access (T_{WR_delay}=min, T_{WR_int}=max, Write after rising edge of WR)			-	260	
T_{write_int}	Internal write time	8-bit access	-	-	180	ns
		16-bit access			260	
T_{WR_delay}	Delay between WR deassertion and assertion		5	-	-	ns
T_{Coll}	Extra read delay	RD access directly follows WR access with the same address (8-bit accesses or 8-bit WR and 16-bit RD)	-	-	20	ns
		different addresses or 16-bit accesses			0	
$T_{WR\_to\_RD}$	Delay between WR deassertion and RD assertion		0	-	-	ns
$T_{CS\_WR\_overlap}$	Time both CS and WR have to be deasserted simultaneously (only if CS is deasserted at all)		5	-	-	ns
$T_{CS\_RD\_overlap}$	Time both CS and RD have to be deasserted simultaneously (only if CS is deasserted at all)		5	-	-	ns
T_{IRQ_delay}	Internal delay between AL event and LINT output to enable correct reading of the interrupt registers.		-	180	-	ns

Table 4-14: PDI Local Bus Timing Table

4.5.8 Function Local Bus Timing

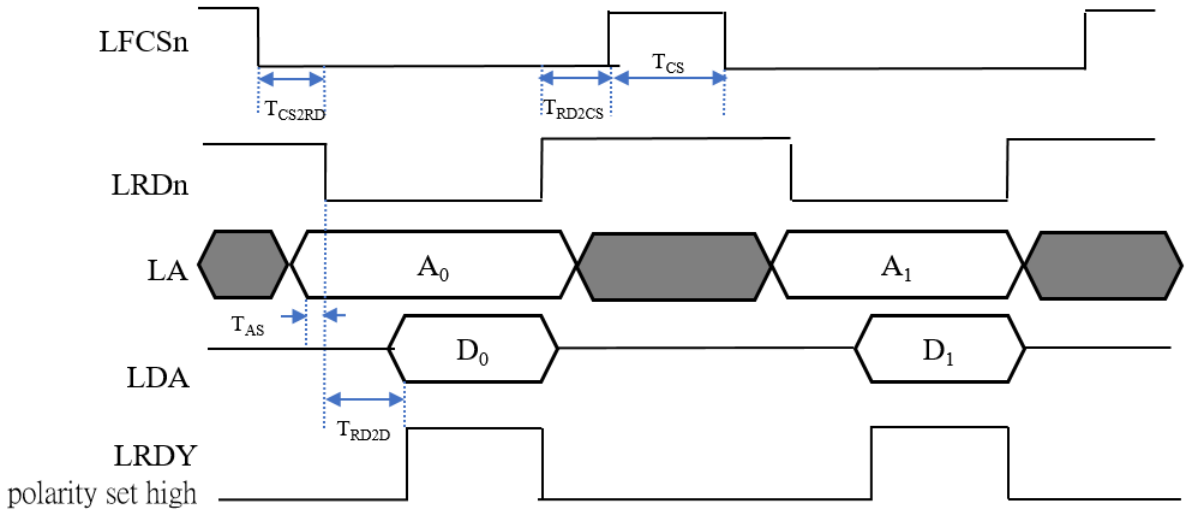


Figure 4-27: Function Local Bus Signal Read Access

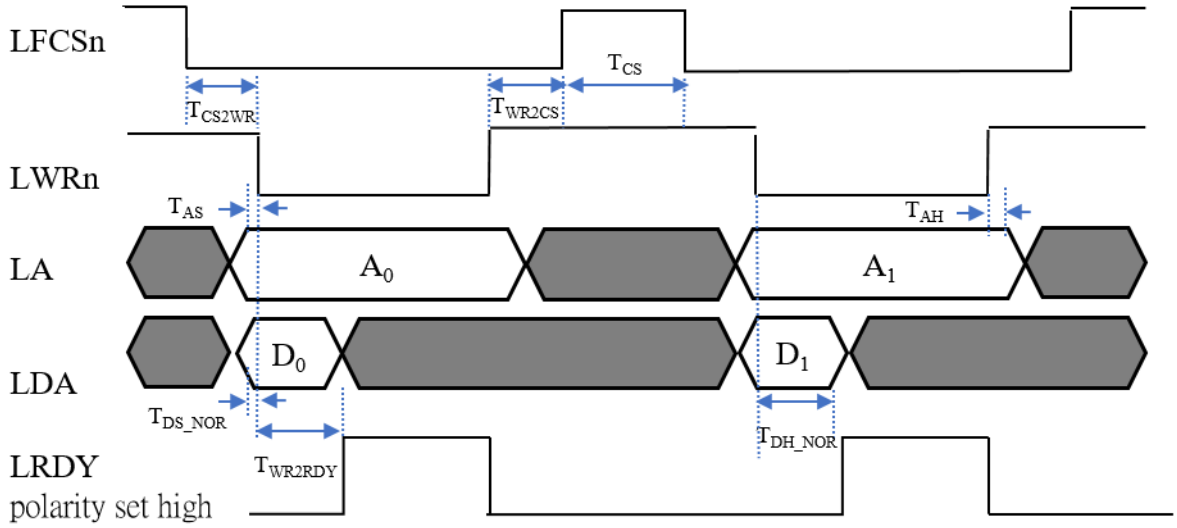


Figure 4-28: Function Local Bus Write Access (Late Sample = 0)

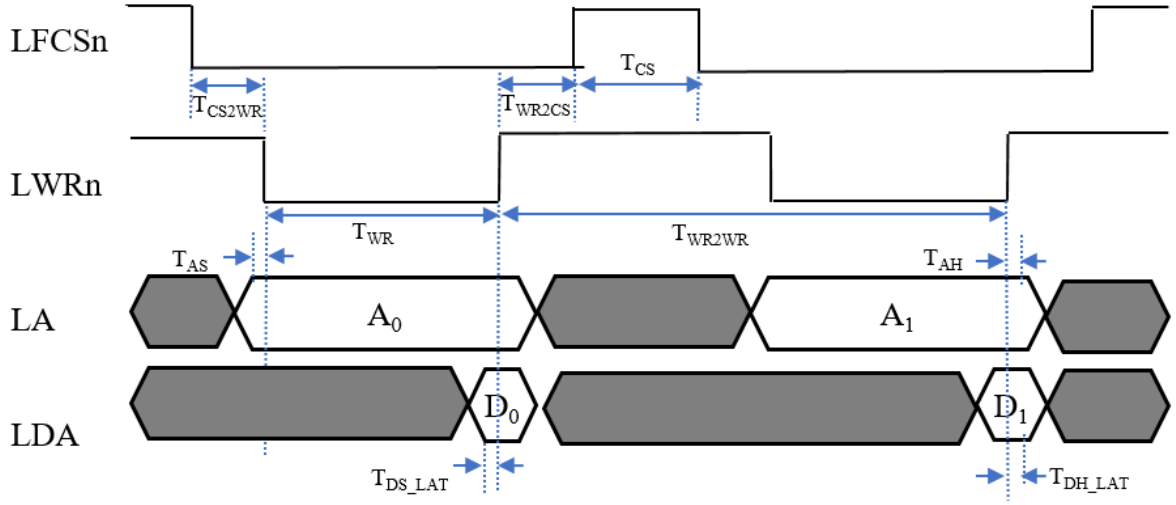
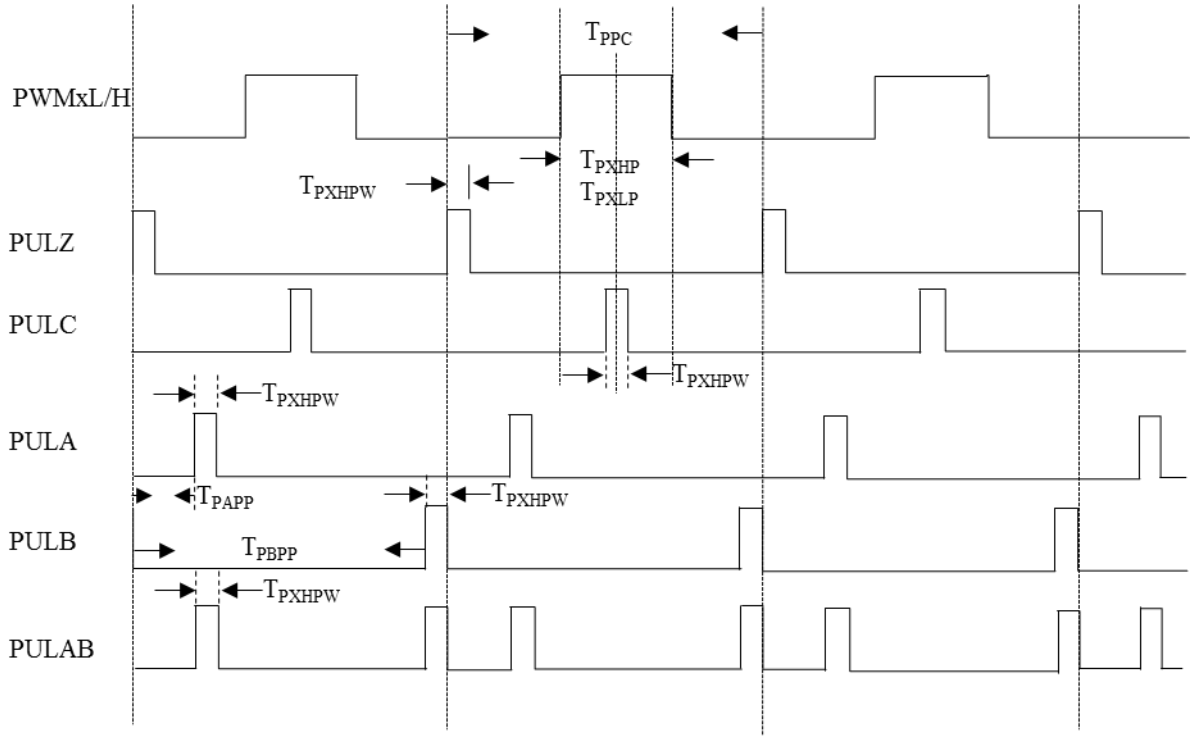


Figure 4-29: Function Local Bus Write Access (Late Sample = 1)

Symbol	Description	Min	Typ	Max	Units
T_{CS}	LFCSn back to back	30	-	-	ns
T_{CS2RD}	LFCSn to LRDn	0	-	-	ns
T_{CS2WR}	LFCSn to LWR,	0	-	-	ns
T_{RD2CS}	LRDn to LFCSn	0	-	-	ns
T_{WR2CS}	LWRn to LFCSn	0	-	-	ns
T_{AS}	LA setup time	0	-	-	ns
T_{AH}	LA hold time	0	-	-	ns
T_{A2D}	LA change to LDA valid	-	-	40	ns
T_{RD}	LRDn pulse	T_{RD2D}	-	-	ns
T_{RD2D}	LRDn to LRDY	-	-	80	ns
T_{WR}	LWRn pulse	30	-	-	ns
T_{WR2RDY}	LWRn assert to LRDY assert	-	-	60	ns
T_{WR2WR}	LWRn back to back (late sample)	100	-	-	ns
T_{DS_NOR}	LDA setup time	0	-	-	ns
T_{DH_NOR}	LDA hold time	40	-	-	ns
T_{DS_LAT}	LDA setup time with Late Sample	10	-	-	ns
T_{DH_LAT}	LDA hold time with Late Sample	10	-	-	ns

Table 4-15: Function Local Bus Access Timing

4.5.9 PWM Motor Controller Timing



Note: PWMx mean PWM 1 to PWM 3

Figure 4-30: PWMx Timing

Symbol	Description	EN8X	Min	Typ	Max	Units
T_{PPC}	PWM Period Cycle	x1	-	PPC * 10	-	ns
		x8	-	PPC * 80	-	ns
T_{PxHP}	PWM x High pulse Width set by PxHPWR	x1	-	PxHPV * 10*1	-	ns
		x8	-	PxHPV * 80*1	-	ns
T_{PxLP}	PWM x Low pulse Width set by PxHPWR	x1	-	PxHPV * 10*1	-	ns
		x8	-	PxHPV * 80*1	-	ns
T_{PXHPW}	Pulse width for PULZ, PULC, PULA, PULB, and PULAB	x1	-	PXHPW * 10	-	ns
		x8	-	PXHPW * 80	-	ns
T_{PAPP}	PWM Trigger Pulse A Position in PWM Period Cycle	x1	-	PTAPP * 10	-	ns
		x8	-	PTAPP * 80	-	ns
T_{PBPP}	PWM Trigger Pulse B Position in PWM Period Cycle	x1	-	PTBPP * 10	-	ns
		x8	-	PTBPP * 80	-	ns

Note *1: “x” = 1 ~ 3

Table 4-16: PWMx Timing Table

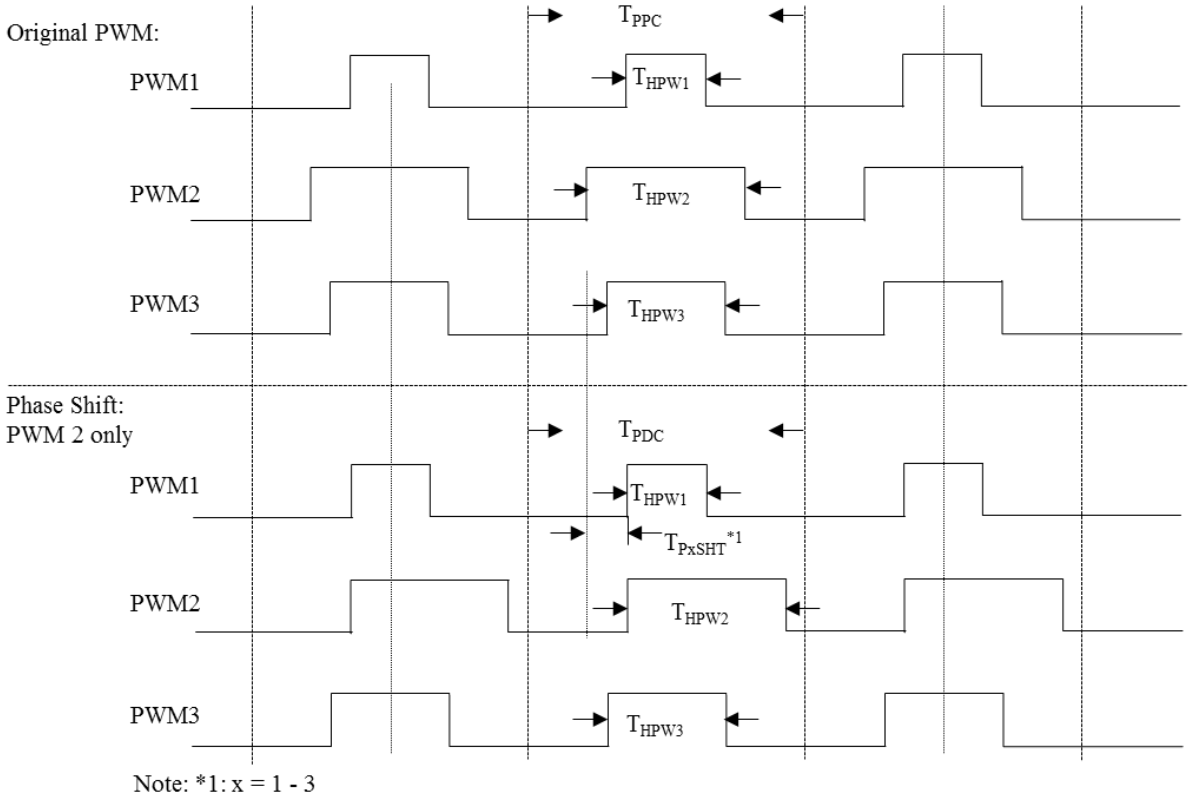


Figure 4-31: Only PWM Channel 2 Shift Diagram

Symbol	Description	EN8X	Min	Typ	Max	Units
T_{P1SHT}	PWM pulse was postponed raising time (addition with P1SHR) and the pulse width stays the same	x1	-	P1SHIFT * 10	-	ns
		x8	-	P1SHIFT * 80	-	ns
T_{P2SHT}	Please reference T_{P1SHT} content	x1	-	P2SHIFT * 10	-	ns
		x8	-	P2SHIFT * 80	-	ns
T_{P3SHT}	Please reference T_{P1SHT} content	x1	-	P3SHIFT * 10	-	ns
		x8	-	P3SHIFT * 80	-	ns

Table 4-17: PWMx Shift Timing Table

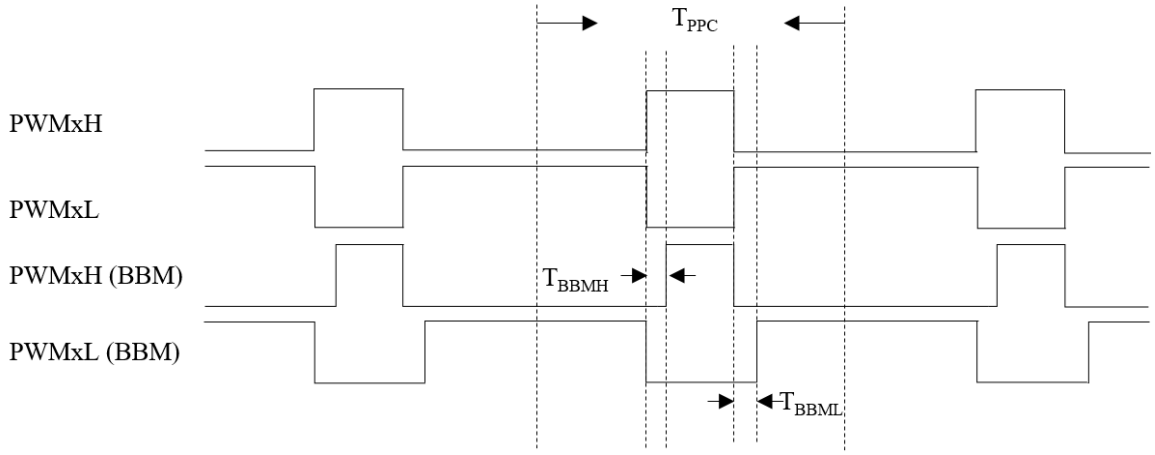


Figure 4-32: BBM (Break Before Make) Timing Diagram

Symbol	Description	EN8X	Min	Typ	Max	Units
T_{BBMH}	High pulse was postponed raising and reduce pulse width	x1	-	PBBMH * 10	-	ns
		x8	-	PBBMH * 80	-	ns
T_{BBML}	Low pulse was postponed falling and addition pulse width	x1	-	PBBML * 10	-	ns
		x8	-	PBBML * 80	-	ns

Table 4-18: PWMx BBM Timing Table

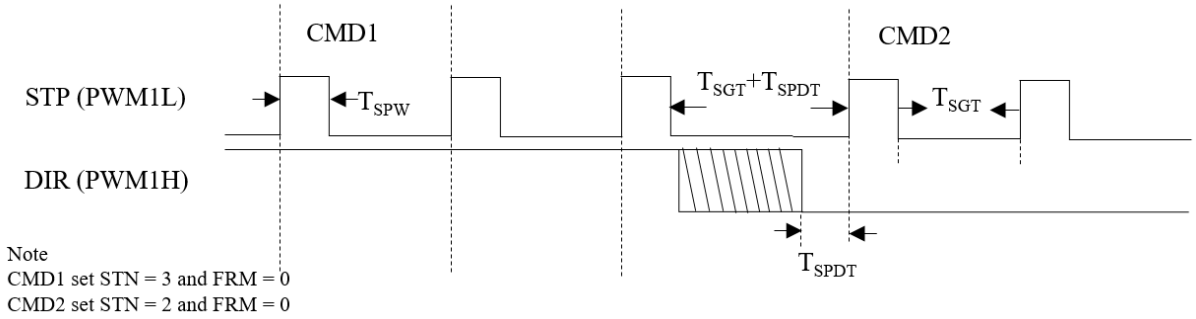


Figure 4-33: One Shot with multi Step Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{SGT}	Step Pulse to Pulse Gap time set by SGTLR and SGTHR	-	SGT * 10	-	ns
T_{SPW}	Step Pulse Width set by SHPWR Note: Step frequency = 1/ (T_{SPW} +T_{SGT})	-	SPW * 10	-	ns
T_{SPDY}	Direction Transform Delay Time set by TDLYR	-	SPDT * 10	-	ns

Table 4-19: Step function timing table

4.5.10 Incremental and Hall Encoder Interface Timing

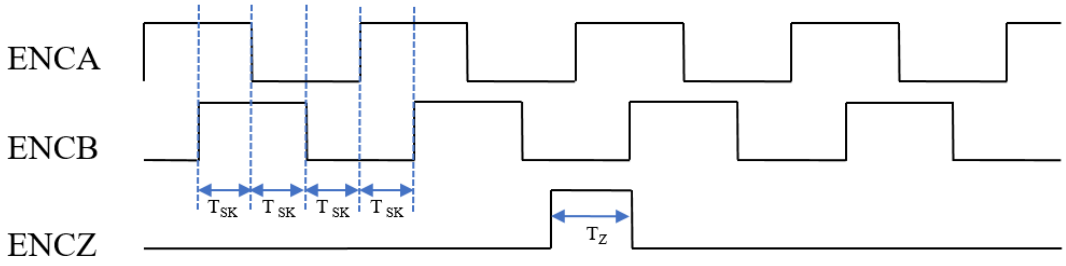


Figure 4-34: ABZ Timing Diagram

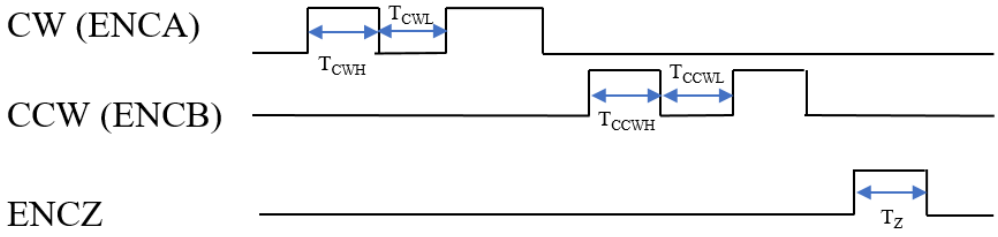


Figure 4-35: CW/CCW Timing Diagram

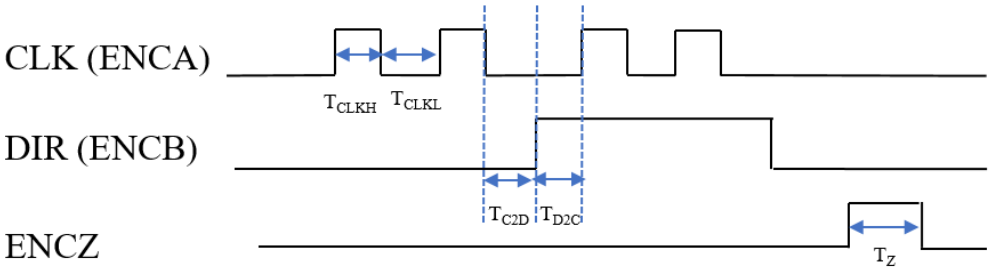


Figure 4-36: CLK/DIR Timing Diagram

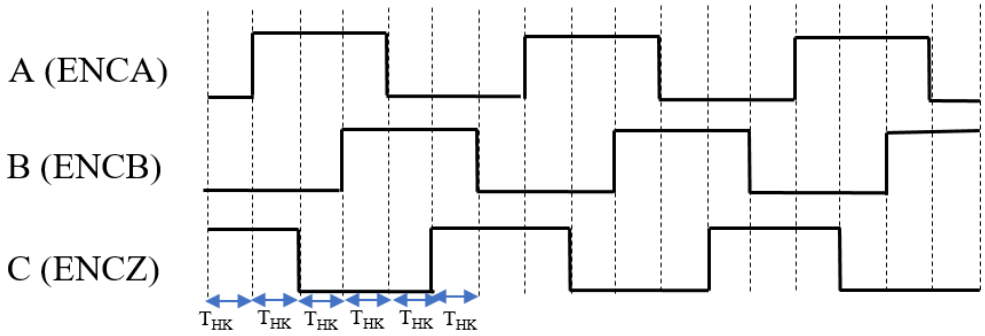


Figure 4-37: Hall Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{SK}	AB state keep time	30	-	-	ns
T_{Z}	Z Pulse Width	30	-	-	ns
T_{CWH}	CW high time	30	-	-	ns
T_{CWL}	CW low time	30	-	-	ns
T_{CCWH}	CCW high time	30	-	-	ns
T_{CCWL}	CCW low time	30	-	-	ns
T_{CLKH}	CLK high time	30	-	-	ns
T_{CLKL}	CLK low time	30	-	-	ns
T_{C2D}	CLK to DIR time	30	-	-	ns
T_{D2C}	DIR to CLK time	30	-	-	ns
T_{HK}	Hall state keeps time	60	-	-	ns

Table 4-20: Incremental and Hall Encoder Timing Table

4.5.11 SPI Master Timing

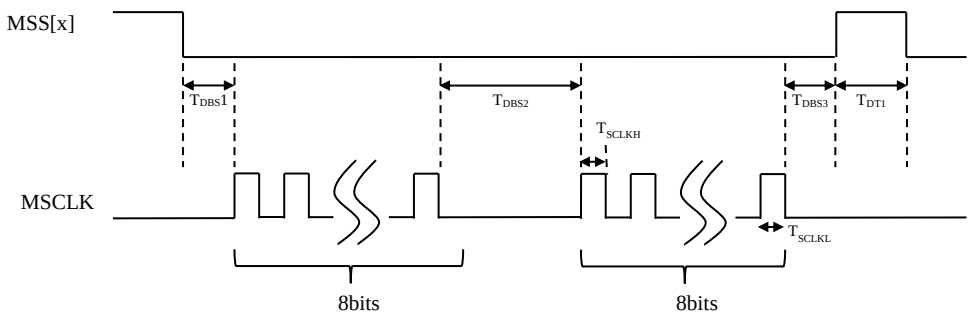


Figure 4-38: SPI Master Timing

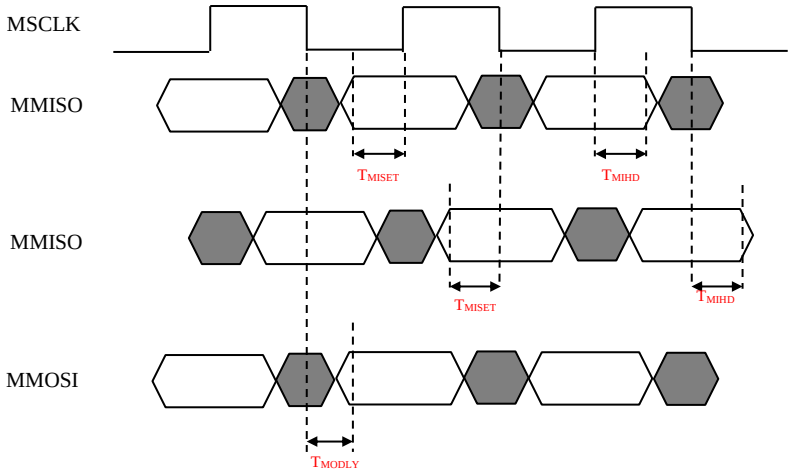


Figure 4-39: MMISO /MMOSIO Timing

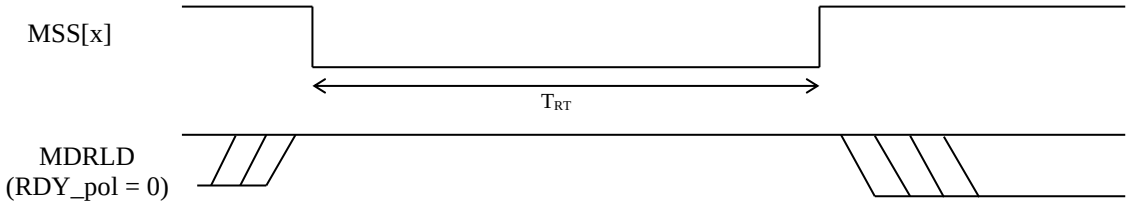


Figure 4-40: SPI MDRLD Ready Timeout Timing

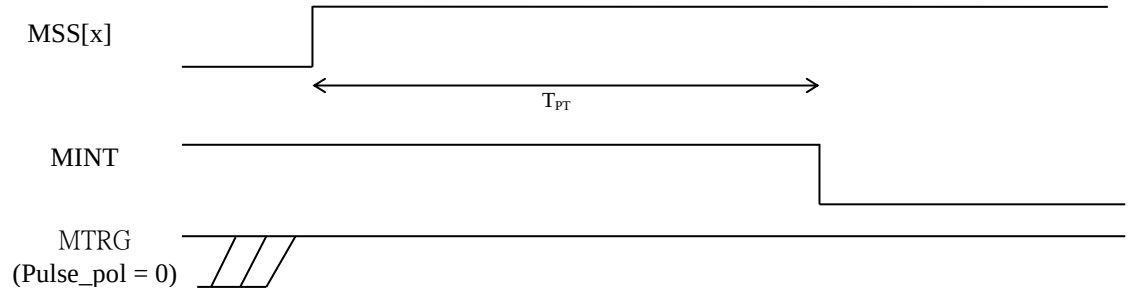


Figure 4-41: SPI MTRG Trigger Pulse Timeout

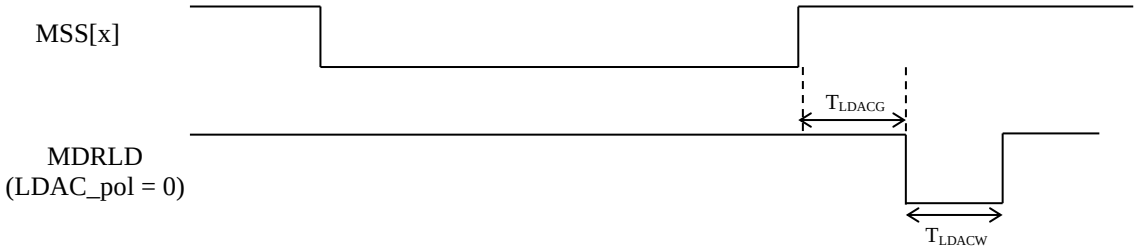


Figure 4-42: SPI MDRLD Trigger LDAC Gap and Width Timing

Symbol	Description	Min	Typ	Max	Units
Clock					
T_{SCLK}	MSCLK Period	-	T_{SCLKH} + T_{SCLKL}	-	ns
T_{SCLKH}	MSCLK high	-	5 * Divide	-	ns
T_{SCLKL}	MSCLK low	-	5 * Divide	-	ns
Bus Timing					
T_{DBS1}	MSS[x] to MSCLK (Mode0/1 without DBS1K)	-	(DBS + 1) * Tsclk	-	ns
	MSS[x] to MSCLK (Mode2/3 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	MSS[x] to MSCLK (Mode0/1 with DBS1K)	-	((1024 * (DBS + 1)) + 1) * Tsclk	-	ns
	MSS[x] to MSCLK (Mode2/3 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
T_{DBS2}	Byte to byte (Mode0/1 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	Byte to byte (Mode2/3 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	Byte to byte (Mode0/1 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
	Byte to byte (Mode2/3 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
T_{DBS3}	MSCLK to MSS[x] (Mode0/1 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	MSCLK to MSS[x] (Mode2/3 without DBS1K)	-	(DBS + 1.0) * Tsclk	-	ns
	MSCLK to MSS[x] (Mode0/1 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
	MSCLK to MSS[x] (Mode2/3 with DBS1K)	-	((1024 * (DBS + 1)) + 1.0) * Tsclk	-	ns
T_{DT1}	MSS[x] gap (without DT1K)	-	(DT + 2) * Tsclk	-	ns
	MSS[x] gap (with DT1K)	-	(1024 * (DT + 1) + 2) * Tsclk	-	ns
T_{MISET}	MMISO setup time	10.5	-	-	ns
T_{MIHD}	MMISO hold time	0	-	-	ns
T_{MODLY}	MMOSI output delay	-	-	0.5	ns
T_{RT}	MDRLD ready timeout (RDY mode)	-	(1 + SPIRPT) * 1024 * Tsclk	-	ns
T_{PT}	MTRG timeout	-	(1 + SPIRPT) * 1024 * Tsclk	-	ns
T_{LDACG}	MDRLD Gap (LDAC mode)	-	((LDACG1K * 1023) + 1) * (LDGAP + 1) * Tsclk	-	ns
T_{LDACW}	MDRLD Width (LDAC mode)	-	(LDACG1K * 1023 + 1) * (LDWID + 1) * Tsclk	-	ns

Table 4-21: SPI Master Timing Table

4.5.12 RSTO, EEPROM and EEP_DONE Timing

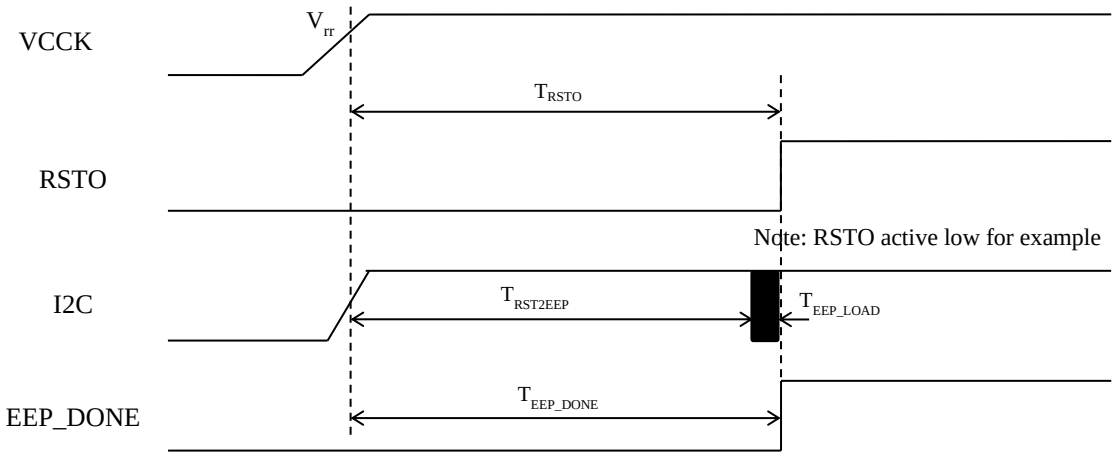


Figure 4-43: Power up to RSTO, EEPROM and EEP_DONE Timing

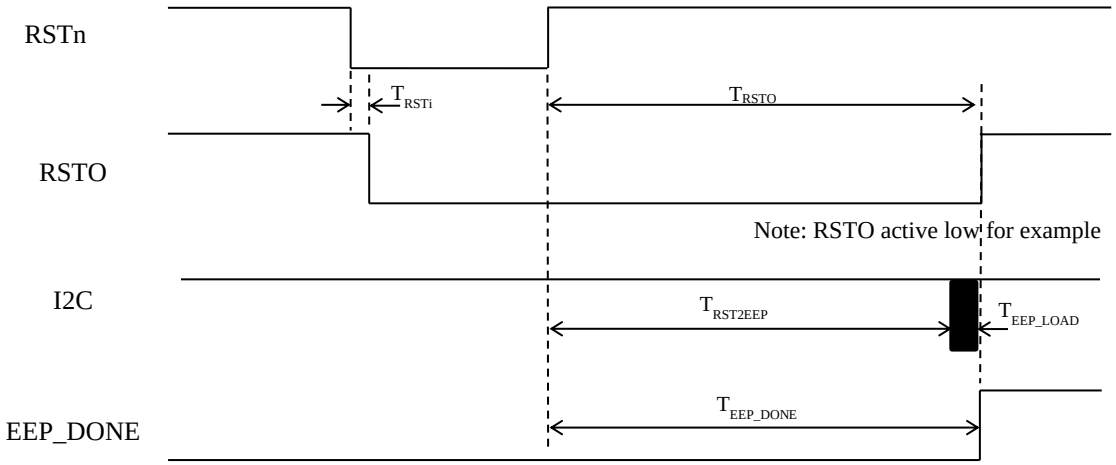


Figure 4-44: RSTn to RSTO, EEPROM and EEP_DONE Timing

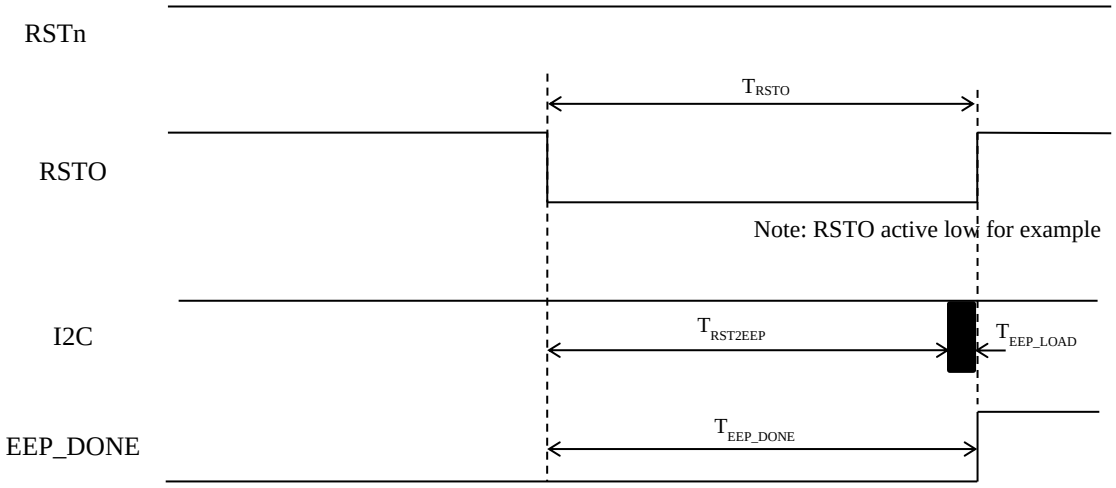
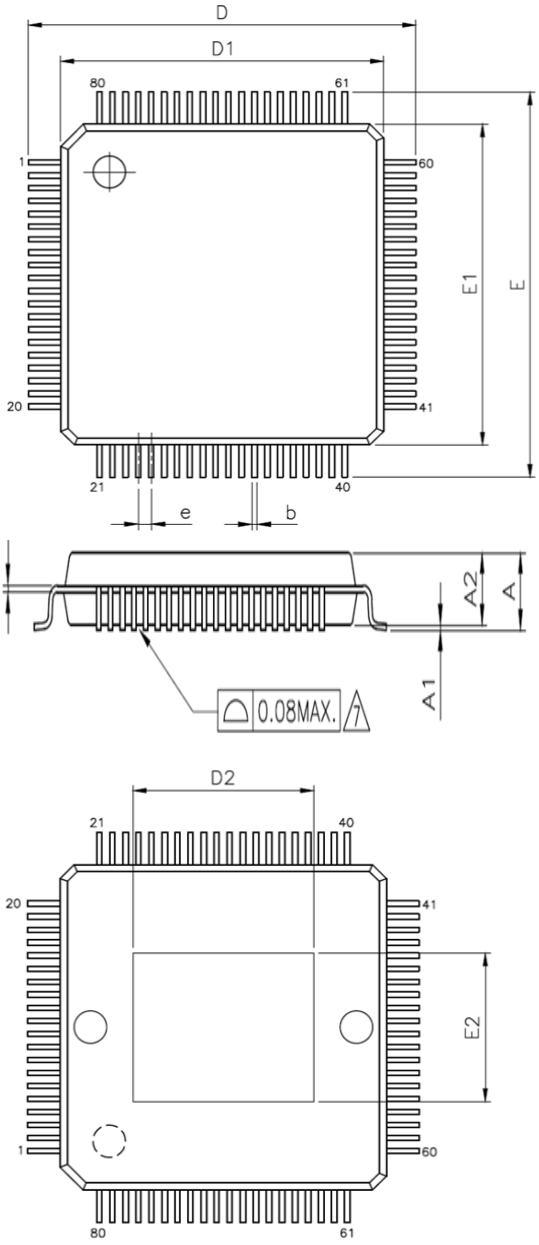


Figure 4-45: Register Reset to RSTO, EEPROM and EEP_DONE Timing

Symbol	Description	Min	Typ	Max	Units
T_{RSTO}	The period of chip internal reset counter	-	63	-	ms
T_{RSTi}	RSTn asserted to RSTO active	-	0	-	ns
$T_{RST2EEP}$	RSTn de-asserted to start EEPROM Loading	-	61.5	-	ms
T_{EEP_LOAD}	EEPROM loading period (Checksum Matched)	-	1.5	-	ms
T_{EEP_DONE}	RSTn de-asserted to EEP_DONE active	-	63	-	ms

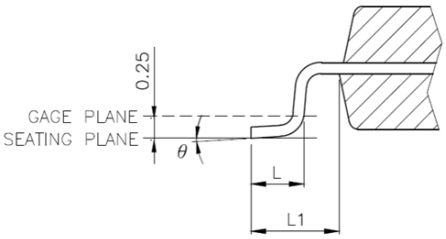
Table 4-22: RSTO, EEPROM and EEP_DONE timing table

5 Package Information



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

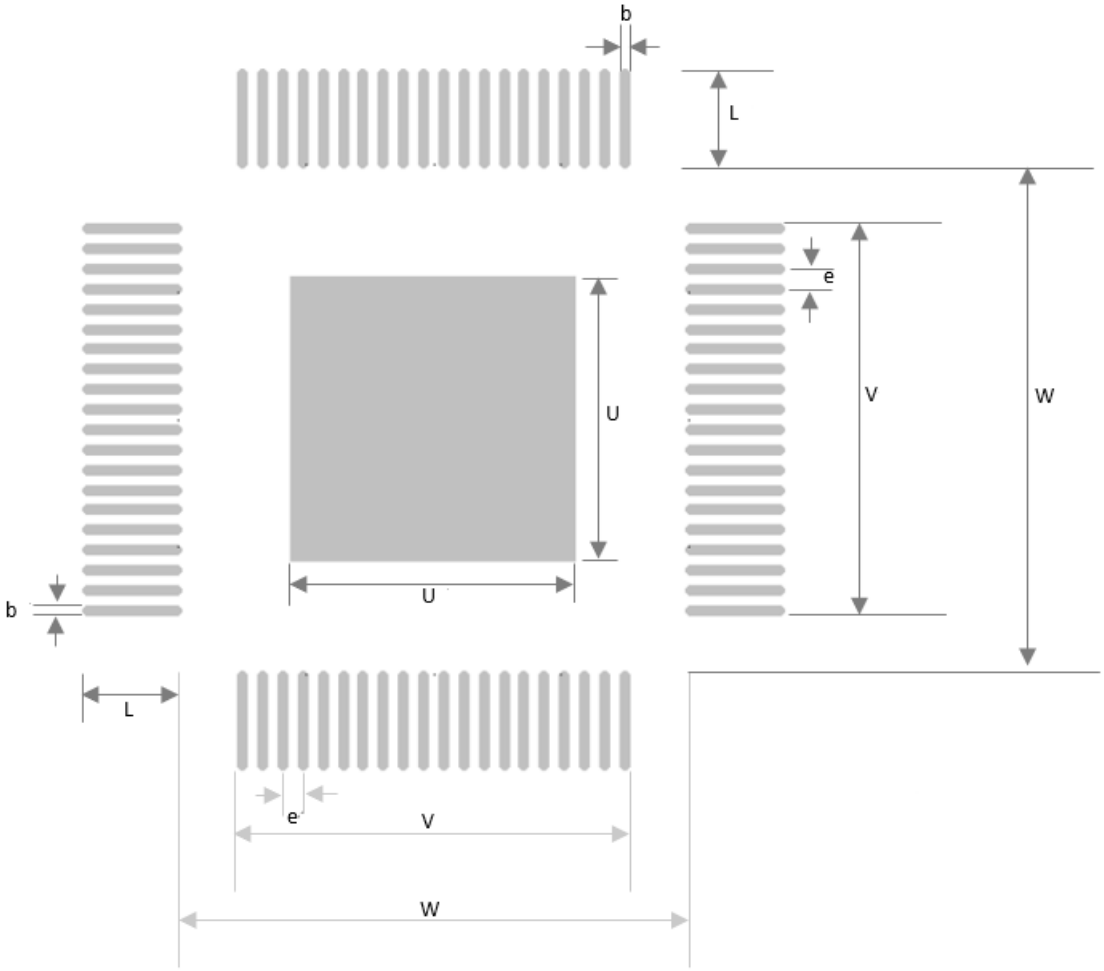
SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	--	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°



THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	D2		E2	
	MIN.	MAX.	MIN.	MAX.
21*X18*	4.71	5.69	3.88	4.72

Recommended PCB Footprint for 80-pin LQFP lead Free package



Symbol	Description	Typical Dimension
e	Lead pitch	0.40 mm
b	Pad width	0.20 mm
L	Pad length	2.00 mm
U	-	5.70 mm
V	-	7.80 mm
W	-	10.00 mm

6 Ordering Information

Part Number	Description
AX58100 LT	80-pin LQFP lead Free package, Industrial temperature range: -40 to 105°C.

7 Revision History

Revision	Date	Comments
V0.20	2018/06/11	Preliminary release.
V0.30	2018/07/27	1. Changed the pin name, type and descriptions of pin #56 in Section 1.3, 1.4. 2. Removed the "VCC33D" descriptions in Section 14. 3. Modified some descriptions in Section 2.1, 3.2.1, 9.2, 9.4.1. 4. Updated Figure 0-1.
V1.00	2018/09/26	1. Changed some pin definitions in Section 1.4. 2. Added a new bootstrap pin definition in Section 3.1. 3. Modified some EEPROM layout and bit definitions in Section 3.2. 4. Changed the default value of EEPROM word offset 0x41 to 0x0021. 5. Modified some ESC Memory Map and Function Registers Map definitions in Section 3.3. 6. Updated some timing spec. and waveforms in Section 4. 7. Modified some descriptions in Features and Section 1.1, 2. 8. Updated Figure 1-1, 1-2.
V1.01	2018/10/05	1. Modified some descriptions in Section 1.1, 2.4, 3, 5. 2. Corrected a typo in Figure 1-2.
V1.02	2018/11/07	1. Modified a typo in Section 6.
V1.03	2019/02/20	1. Modified some information in Section 4.2. 2. Updated some description in Section 5.
V1.04	2019/09/11	Corrected some typos and modified some descriptions
V1.05	2020/05/19	1. Updated power consumption value in section 4.2 2. Added section 4.5.12 for RSTO, EEPROM and EEP_DONE timing 3. Added some description for EEP_DONE in section 1.4.1 4. Updated Digital IO Timing in section 4.5.4
V1.06	2021/06/30	Corrected some description in Section 3.2
V1.07	2021/08/17	Modified some descriptions in Section 4.5.4
V1.08	2024/11/26	Removed ESC's register 0x518 description in Section 3.3.1
V1.09	2024/12/12	1. Modified T_{SCLK} information in Table 4-11 and 4-13 2. Added Recommended PCB Footprint in Section 5

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