Features

Document No: AX58400/V1.04/12/03/24

- **A System-in-Package (SiP) product based on STSTM32H755 microcontroller and ASIX EtherCAT slave controller**
  - **STM32H755 Dual-Core ARM® Cortex®-M7 & Cortex®-M4 microcontroller**
    - 32-bit Arm® Cortex®-M7 core with double-precision FPU and L1 cache: 16 Kbytes of data and 16 Kbytes of instruction cache; frequency up to 480 MHz, MPU, 1027 DMIPS/ 2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
    - 32-bit Arm® 32-bit Cortex®-M4 core with FPU, Adaptive real-time accelerator (ST ART Accelerator™) for internal Flash memory and external memories, frequency up to 240 MHz, MPU, 300 DMIPS/1.25 DMIPS /MHz (Dhrystone 2.1), and DSP instructions
  - **Memories**
    - 2 Mbytes of dual bank Flash memory with read-while-write support
    - 1 Mbyte of RAM: 192 Kbytes of TCM RAM (inc. 64 Kbytes of ITCM RAM + 128 Kbytes of DTCM RAM for time critical routines), 864 Kbytes of user SRAM, and 4 Kbytes of SRAM in Backup domain
    - Dual mode Quad-SPI memory interface running up to 133 MHz
    - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND Flash memory clocked up to 125 MHz in Synchronous mode
    - CRC calculation unit
  - **Security**
    - ROP, PC-ROP, active tamper, secure firmware upgrade support, Secure access mode
  - **General-purpose input/outputs (GPIO)**
    - Up to 97 I/O ports with interrupt capability
  - **Reset and power management**
    - 3 separate power domains which can be independently clock-gated or switched off:
    - D1: high-performance capabilities
    - D2: communication peripherals and timers
    - D3: reset/clock control/power management
    - 1.62 to 3.6 V application supply and I/Os
    - POR, PDR, PVD and BOR
    - Dedicated USB power embedding a 3.3 V internal regulator to supply the internal PHYs
    - Embedded regulator (LDO) to supply the digital circuitry
    - High power-efficiency SMPS step-down converter regulator to directly supply VCORE and/or external circuitry
    - Voltage scaling in Run and Stop mode (6 configurable ranges)
    - Backup regulator (~0.9 V)
    - Voltage reference for analog peripheral/VREF+
    - 1.2 to 3.6 V VBAT supply
    - Low-power modes: Sleep, Stop, Standby and VBAT supporting battery charging
  - **Low-power consumption**
    - VBAT battery operating mode with charging capability
    - CPU and domain power state monitoring pins
    - 2.95 µA in Standby mode (Backup SRAM OFF, RTC/LSE ON)
  - **Clock management**
    - Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 KHz LSI
    - External oscillators: 4-48 MHz HSE, 32.768 KHz LSE
    - 3× PLLs (1 for the system clock, 2 for kernel clocks) with Fractional mode
  - **Interconnect matrix**
    - 3 bus matrices (1 AXI and 2 AHB)
    - Bridges (5× AHB2-APB, 2× AXI2-AHB)
  - **4 DMA controllers to unload the CPU**
    - 1× high-speed master direct memory access controller (MDMA) with linked list support
    - 2× dual-port DMAs with FIFO
    - 1× basic DMA with request router capabilities
  - **Up to 35 communication peripherals**
    - 4× I2Cs FM+ interfaces (SMBus/PMBus)
    - 4× USARTs/4x UARTs (ISO7816 interface, LIN, IrDA, up to 12.5 Mbit/s) and 1x LPUART
    - 6× SPIs, 3 with muxed duplex I2S audio class accuracy via internal audio PLL or external clock, 1x I2S in LP domain (up to 150 MHz)
    - 4x SAIs (serial audio interface)
    - SPDIFRX interface
    - SWPMI single-wire protocol master I/F
    - MDIO Slave interface
    - 2× SD/SDIO/MMC interfaces (up to 125 MHz)
    - 2× CAN controllers: 2 with CAN FD, 1 with time-triggered CAN (TT-CAN)
    - 2× USB OTG interfaces (1FS, 1HS/FS) crystal-less solution with LPM and BCD
    - Ethernet MAC interface with DMA controller
    - HDMI-CEC
    - 8- to 14-bit camera interface (up to 80 MHz)
  - **11 analog peripherals**
    - 3× ADCs with 16-bit max. resolution (up to 36 channels, up to 3.6 MSPS)
    - 1× temperature sensor

ASIX Electronics Corporation
4F, No.8, Hsin Ann Rd.,
Hsinchu Science Park,
Hsinchu, Taiwan 30078

Released Date: 12/03/2024
TEL: +886-3-579-9500
FAX: +886-3-579-9558
https://www.asix.com.tw/

- 2× 12-bit D/A converters (1 MHz)
- 2× ultra-low-power comparators
- 2× operational amplifiers (7.3 MHz bandwidth)
- 1× digital filters for sigma delta modulator (DFSDM) with 8 channels/4 filters

Graphics

- LCD-TFT controller up to XGA resolution
- ST Chrom-ART graphical hardware Accelerator™ (DMA2D) to reduce CPU load
- Hardware JPEG Codec

Up to 22 timers and watchdogs

- 1× high-resolution timer (2.1 ns max resolution)
- 2× 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input (up to 240 MHz)
- 2× 16-bit advanced motor control timers (up to 240 MHz)
- 10× 16-bit general-purpose timers (up to 240 MHz)
- 5× 16-bit low-power timers (up to 240 MHz)
- 4× watchdogs (independent and window)
- 2× SysTick timers
- RTC with sub-second accuracy and hardware calendar

Cryptographic acceleration

- AES 128, 192, 256, TDES,
- HASH (MD5, SHA-1, SHA-2), HMAC
- True random number generators

Debug mode

- SWD & JTAG interfaces
- 4 Kbytes Embedded Trace Buffer

96-bit Unique Identifier (UID)

EtherCAT Slave Controller (ESC) Sub-system

- 2 Integrated Fast Ethernet PHYs
- 3rd Ethernet MII Port for flexible EtherCAT network configuration
- 8 Fieldbus Memory Management Units (FMMUs)
- 8 Sync Managers
- 64-bit distributed clock support allows synchronization with other EtherCAT devices
- 9K bytes RAM
- Step & Direction Controller
- Incremental and Hall Encoder Interface
- SPI Master Controller
- Emergency Stop Input
- Configurable Watchdog for Outputs and Inputs Monitoring
- 20 GPIOs controled by EtherCAT direclty

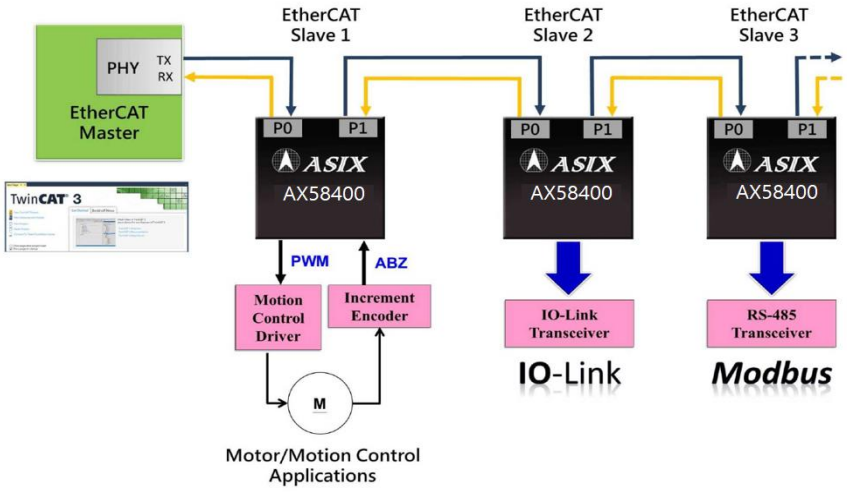
225LD EHS-TFBGA 13x13 mm, 0.8-mm pitch, RoHS Compliant Package

Operating Temperature Range: -40 to +85°C

Target Applications

- Motion/Motor Control
- Digital I/O Control
- Robotics
- Sensors Data Acquisition
- EtherCAT IO-Link Master
- EtherCAT Junction Slave Module
- Communication Module
- Operator HMI Interfaces

Typical Applications Diagram



Functional Block Diagram

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1 Introduction

1.1 General Description

The AX58400 EtherCAT Slave Controller with Dual-Core MCU is a System-in-Package (SiP) product based on the STM32H755 microcontroller from STMicroelectronics. AX58400 is equipped with STM32 Dual-core Arm® Cortex®-M7 and Cortex®- M4 32-bit RISC cores. The Cortex®-M7 core operates at up to 480 MHz and the Cortex®- M4 core at up to 240 MHz. Both cores feature a floating point unit (FPU) which supports Arm® single- and double-precision (Cortex®-M7 core) operations and conversions (IEEE 754 compliant), including a full set of DSP instructions and a memory protection unit (MPU) to enhance application security. The EtherCAT Slave Controller (ESC) with two integrated Fast Ethernet PHYs which support 100Mbps full-duplex operation and HP Auto-MDIX. The AX58400 supports the CANopen (CoE), TFTP (FoE), Vender specific application (VoE), etc. standard EtherCAT protocols and provides a cost-effective solution for industrial automation, motion/motor control, robotics, digital I/O control, sensors data acquisition, etc. industrial fieldbus applications.

AX58400 incorporates high-speed embedded memories with a dual-bank Flash memory of 2 Mbytes, up to 1 Mbyte of RAM (including 192 Kbytes of TCM RAM, up to 864 Kbytes of user SRAM and 4 Kbytes of backup SRAM), as well as an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, 2x32-bit multi-AHB bus matrix and a multi-layer AXI interconnect supporting internal and external memory access.

AX58400 offers three ADCs, two DACs, two ultra-low power comparators, a low-power RTC, a high-resolution timer, 12 general-purpose 16-bit timers, two PWM timers for motor control, five low-power timers, a true random number generator (RNG), and a cryptographic acceleration cell. The devices support four digital filters for external sigma-delta modulators (DFSDM). They also feature standard and advanced communication interfaces.

- Standard peripherals
  - Four I^2Cs
  - Four USARTs, four UARTs and one LPUART
  - Six SPIs, three I^2Ss in Half-duplex mode. To achieve audio class accuracy, the I^2S peripherals can be clocked by a dedicated internal audio PLL or by an external clock to allow synchronization.
  - Four SAI serial audio interfaces
  - One SPDIFRX interface
  - One SWPMI (Single Wire Protocol Master Interface)
  - Management Data Input/Output (MDIO) slaves
  - Two SDMMC interfaces
  - A USB OTG full-speed and a USB OTG high-speed interface with full-speed capability (with the ULPI)
  - One FDCAN plus one TT-FDCAN interface
  - An Ethernet interface
  - ST Chrom-ART Accelerator™
  - HDMI-CEC
- Advanced peripherals including
  - A flexible memory control (FMC) interface
  - A Quad-SPI Flash memory interface
  - A camera interface for CMOS sensors
  - An LCD-TFT display controller
  - A JPEG hardware compressor/decompressor

Refer to Table 1.1-1: AX58400 Features and Peripheral Counts for the list of peripherals available in detail.

The AX58400's ESC circuit also provides a three-channel PWM controller or a one-channel Step/Direction controller, and an increment/hall encode interface for closed-loop motor control, a SPI master controller for data acquisition and output, and an I/O watchdog for functional safety.

The AX58400, in 225LD EHS-TFBGA 13x13 mm, 0.8-mm pitch, supports the RoHS compliant package and industrial grade operating temperature range from -40 to 85°C. For VDD power domain, supply voltage can drop down to 1.62 V by using an external power supervisor (see Section 2.5.2: Power supply supervisor) and connecting the PDR_ON pin to VSS. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.

Dedicated supply inputs for USB (OTG_FS and OTG_HS) are available on AX58400 to allow a greater power supply choice. A comprehensive set of power-saving modes allows the design of low-power applications.

These features make AX58400 microcontrollers suitable for a wide range of the EtherCAT applications:

- Motor drive and application control
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Field-Bus to EtherCAT converter

Table 1.1-1: AX58400 Features and Peripheral Counts

Peripherals		AX58400
Flash memory		2 Mbytes
SRAM in Kbytes	SRAM mapped onto AXI bus	512
	SRAM1 (D2 domain)	128
	SRAM2 (D2 domain)	128
	SRAM3 (D2 domain)	32
	SRAM4 (D3 domain)	64
TCM RAM in Kbytes	ITCM RAM (instruction)	64
	DTCM RAM (data)	128
Backup SRAM (Kbytes)		4
FMC		Yes
General-purpose input/outputs		97
Quad-SPI		Yes
Ethernet		Yes
Timers	High-resolution	1
	General-purpose	10
	Advanced-control (PWM)	2
	Basic	2
	Low-power	5
Wakeup pins Tamper pins		4 2
Random number generator		Yes
Cryptographic accelerator		Yes
Communication interfaces	SPI / I^2S	6/3(1)
	I^2C	4
	USART/ UART/ LPUART	4/4/ 1
	SAI	4
	SPDIFRX	4 inputs
	SWPMI	Yes
	MDIO	Yes
	SDMMC	2
	FDCAN/TT-FDCAN	1/1
	USB OTG_FS	Yes
	USB OTG_HS	Yes
Camera interface		Yes
LCD-TFT		Yes
JPEG Codec		Yes
Chrom-ART Accelerator™ (DMA2D)		Yes

Peripherals		AX58400
16-bit ADCs		3
Number of Direct channels		2
Number of Fast channels		6
Number of Slow channels		15
12-bit DAC		Yes
Number of channels		2
Comparators		2
Operational amplifiers		2
Digital filters for sigma delta modulator (DFSDM)		1
Maximum CPU frequency		480 MHz(2)
		400 MHz(3)
		300 MHz(4)
Operating voltage (VDD)		1.62 to 3.6 V(5)
Operating temperatures	Ambient temperature	–40 up to +85 °C(6)
	Junction temperature	–40 to + 125 °C
Package		225LD EHS-TFBGA

1. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
2. The product junction temperature must be kept within the –40 to +105 °C range.
3. The product junction temperature must be kept within the –40 to +125 °C range.
4. Up to 300 MHz for STM32H755xxx3 sales types (extended industrial temperature range).
5. V_{DD}/V_{DDA} can drop down to 1.62 V by using an external power supervisor (see Section 2.5.2: Power supply supervisor) and connecting PDR_ON pin to V_{SS}. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.
6. Using appropriate cooling methods to guarantee that the maximum junction temperature (125 °C) is not exceeded, the maximum ambient temperature (85°C) can be exceeded.

1.2 Block Diagram

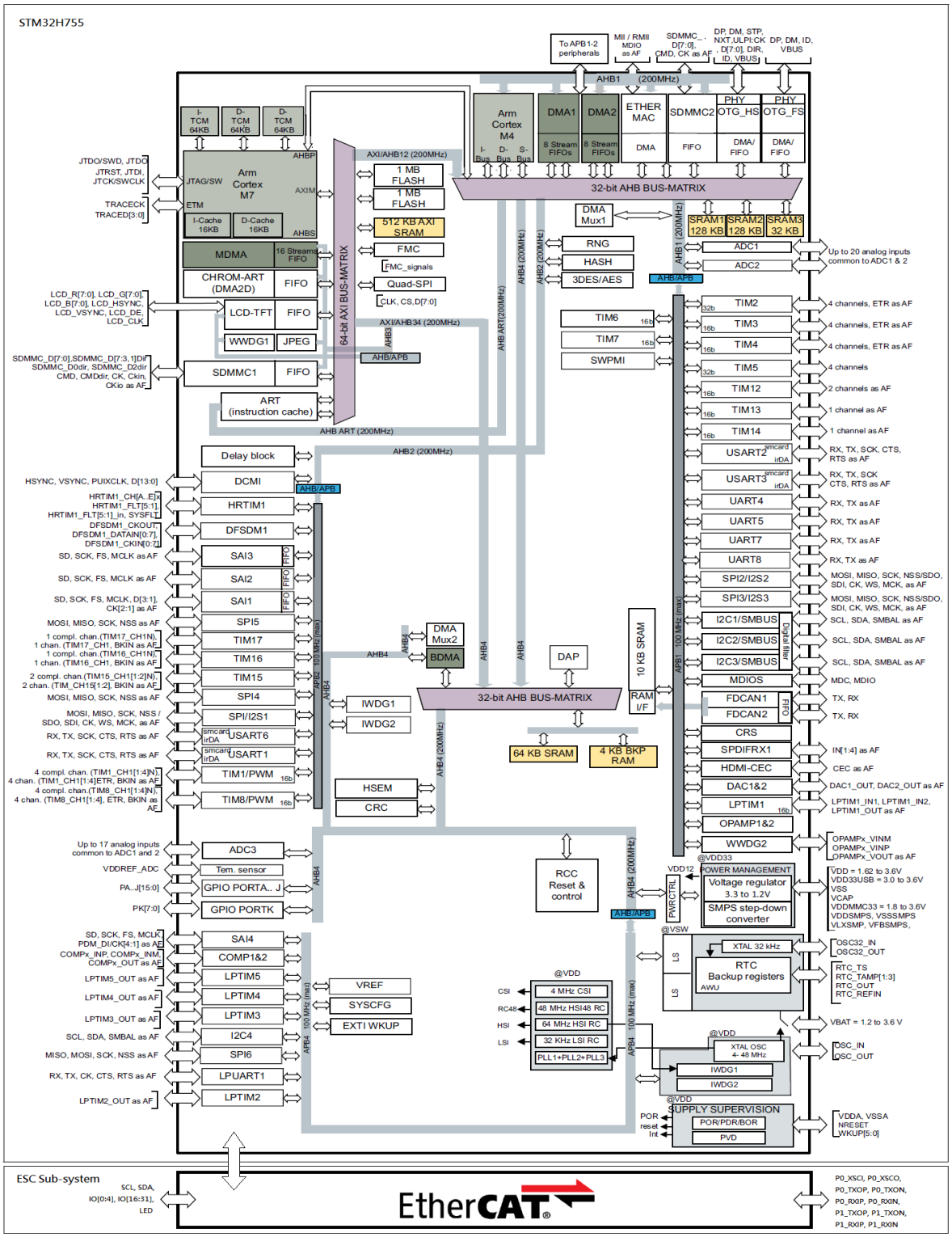


Figure 1.2-1: AX58400 Block Diagram

1.3 Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	VDDLDO	PE13	PE11	PE10	PE8	PF15	PF11	SCLK	PB1	SDA	PA7	PA4	PA3	VREF+	VSSA	A
B	GND	PB10	PE15	PE14	PE12	PE9	PE7	PF14	PB2	PB0	PC4	PA5	RSTO	VREF-	VDDA	B
C	VCAP	SCS_ESC	PB11	IO[24]	MOSI	VDD	VCC3IO	IO[23]	GND	VCCK	PDI_EMU	PA6	RSTn	PA2	GND_PLL	C
D	PB12	PB13	PB14	SCS_FUNC	SINT	VDD	VCC3IO	IO[22]	GND	VCCK	SCL	PC5	PA1	PA0	VCC12A_PLL	D
E	PB15	PD8	PD9	PD10	IO[26]	VDD	VCC3IO	IO[21]	GND	VCCK	IO[4]	TEST	PC1	PC3_C	PC2_C	E
F	PD11	PD12	PD13	SYNC_LATCH[0]	IO[25]	VDD	VCC3IO	GND	GND	VCCK	GND	NC	PC0	PF10	PH1-OSC_OUT	F
G	PD14	PD15	PG6	SYNC_LATCH[1]	IO[2]	VDD	GND	GND	GND	GND	NRST	IO[19]	PF7	PF8	PH0-OSC_IN	G
H	VDD33USB	PG8	PG7	MISO	IO[27]	VDD	GND	GND	GND	GND	IO[17]	IO[18]	PF9	VFBSMPS	VDDSMPS	H
J	VDD50USB	PC8	PC6	PC7	IO[28]	VDD	GND	GND	GND	VDD	IO[0]	IO[1]	PF6	GND	VLXSMPS	J
K	PA10	PA8	PA9	PC9	IO[29]	VDD	VDD	GND	GND	VDD	IO[16]	PE5	PC13	VBAT	VSSSMPS	K
L	PA12	PA11	PA13	IO[31]	IO[30]	PD6	PG11	PG12	P0_RSET_BG	PB4	IO[20]	PE1	PE6	P0_ACT	PC15-OSC32_OUT	L
M	LED_RUN	LED_ERR	EEP_DONE	PA14	PA15	PG9	PG10	PG13	PG14	PB3	PB6	PE4	P1_ACT	PDR_ON	PC14-OSC32_IN	M
N	VCAP	PC10	PC11	PD0	PD7	GND	GND	GND	GND	GND	PB5	PB9	PE0	PE2	PE3	N
P	GND	PC12	PD1	PD3	GND	P1_TXON	P1_RXIN	P1_SD	P0_TXON	P0_RXIN	P0_SD	P0_XSCI	BOOT0	PB8	GND	P
R	VDDLDO	PD2	PD4	PD5	VCC33A	P1_TXOP	P1_RXIP	VCC33A	P0_TXOP	P0_RXIP	VCC33A	P0_XSCO	PB7	VCAP	VDDLDO	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 1.3-1: AX58400 Pinout Diagram

1.4 Signal Description

1.4.1 Main System Pin Description

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
		ANA	Analog-only Input
I/O structure		FT	5 V tolerant I/O
		TT	3.3 V tolerant I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT and FT I/Os	
		_f	I2C FM+ option
		_a	analog option (supplied by V_{DDA})
		_u	USB option (supplied by $V_{DD33USB}$)
		_h	High-speed low-voltage I/O
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 1.4-1: Legend/abbreviations used in the pinout table

By ball definitions

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
N14	PE2	I/O	FT_h	-	TRACECLK, SAI1_CK1, SPI4_SCK, SAI1_MCLK_A, SAI4_MCLK_A, QUADSPI_BK1_IO2, SAI4_CK1, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
N15	PE3	I/O	FT_h	-	TRACED0, TIM15_BKIN, SAI1_SD_B, SAI4_SD_B, FMC_A19, EVENTOUT	-
M12	PE4	I/O	FT_h	-	TRACED1, SAI1_D2, DFSDM1_DATIN3, TIM15_CH1N, SPI4_NSS, SAI1_FS_A, SAI4_FS_A, SAI4_D2, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-
K12	PE5	I/O	FT_h	-	TRACED2, SAI1_CK2, DFSDM1_CKIN3, TIM15_CH1, SPI4_MISO, SAI1_SCK_A, SAI4_SCK_A, SAI4_CK2, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
L13	PE6	I/O	FT_h	-	TRACED3, TIM1_BKIN2, SAI1_D1, TIM15_CH2, SPI4_MOSI, SAI1_SD_A, SAI4_SD_A, SAI4_D1, SAI2_MCLK_B, TIM1_BKIN2_COMP12, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
K13	PC13	I/O	FT	-	EVENTOUT	RTC_TAMP1/RTC_TS/WKUP2
M15	PC14-OSC32_IN (OSC32_IN)(1)	I/O	FT	-	EVENTOUT	OSC32_IN
L15	PC15-OSC32_OUT (OSC32_OUT) (1)	I/O	FT	-	EVENTOUT	OSC32_OUT
J13	PF6	I/O	FT_ha	-	TIM16_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, SAI4_SD_B,	ADC3_INN4, ADC3_INP8

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					QUADSPI_BK1_IO3, EVENTOUT	
G13	PF7	I/O	FT_ha	-	TIM17_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, SAI4_MCLK_B, QUADSPI_BK1_IO2, EVENTOUT	ADC3_INP3
G14	PF8	I/O	FT_ha	-	TIM16_CH1N, SPI5_MISO, SAI1_SCK_B, UART7_RTS/UART7_DE, SAI4_SCK_B, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_INN3, ADC3_INP7
H13	PF9	I/O	FT_ha	-	TIM17_CH1N, SPI5_MOSI, SAI1_FS_B, UART7_CTS, SAI4_FS_B, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_INP2
F14	PF10	I/O	FT_ha	-	TIM16_BKIN, SAI1_D3, QUADSPI_CLK, SAI4_D3, DCMI_D11, LCD_DE, EVENTOUT	ADC3_INN2, ADC3_INP6
G15	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
F15	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
G11	NRST	I/O	RST	-	-	-
F13	PC0	I/O	FT_a	-	DFSDM1_CKIN0, DFSDM1_DATIN4, SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT	ADC123_INP10
E13	PC1	I/O	FT_ha	-	TRACED0, SAI1_D1, DFSDM1_DATIN0, DFSDM1_CKIN4, SPI2_MOSI/I2S2_SDO, SAI1_SD_A, SAI4_SD_A, SDMMC2_CK, SAI4_D1, ETH_MDC,	ADC123_INN10, ADC123_INP11, RTC_TAMP3/WKUP5

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					MDIOS_MDC, EVENTOUT	
E15	PC2_C	ANA	TT_a	-	C1DSLEEP, DFSDM1_CKIN1, SPI2_MISO/I2S2_SDI, DFSDM1_CKOUT, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC3_INN1, ADC3_INP0
E14	PC3_C	ANA	TT_a	-	C1SLEEP, DFSDM1_DATIN1, SPI2_MOSI/I2S2_SDO, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC3_INP1
D14	PA0	I/O	FT_a	-	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, TIM15_BKIN, USART2_CTS/USART2_NSS, UART4_TX, SDMMC2_CMD, SAI2_SD_B, ETH_MII_CRS, EVENTOUT	ADC1_INP16, WKUP0
D13	PA1	I/O	FT_ha	-	TIM2_CH2, TIM5_CH2, LPTIM3_OUT, TIM15_CH1N, USART2_RTS/USART2_DE, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCLK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, LCD_R2, EVENTOUT	ADC1_INN16, ADC1_INP17
C14	PA2	I/O	FT_a	-	TIM2_CH3, TIM5_CH3, LPTIM4_OUT, TIM15_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC12_INP14, WKUP1
A13	PA3	I/O	FT_ ha	-	TIM2_CH4, TIM5_CH4, LPTIM5_OUT, TIM15_CH2,	ADC12_INP15

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	
A12	PA4	I/O	TT_a	-	D1PWREN, TIM5_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_INP18, DAC1_OUT1
B12	PA5	I/O	TT_ ha	-	D2PWREN, TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC12_INN18, ADC12_INP19, DAC1_OUT2
C12	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO/I2S1_SDI, SPI6_MISO,TIM13_CH1, TIM8_BKIN_COMP12, MDIOS_MDC, TIM1_BKIN_COMP12, DCMI_PIXCLK,LCD_G2, EVENTOUT	ADC12_INP3
A11	PA7	I/O	TT_a	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SDO, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC12_INN3, ADC12_INP7, OPAMP1_VINM
B11	PC4	I/O	TT_a	-	C2DSLEEP, DFSDM1_CKIN2, I2S1_MCK, SPDIFRX1_IN3, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC12_INP4, OPAMP1_VOUT, COMP1_INM
D12	PC5	I/O	TT_a	-	C2SLEEP, SAI1_D3, DFSDM1_DATIN2, SPDIFRX1_IN4,	ADC12_INN4, ADC12_INP8, OPAMP1_VINM

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					SAI4_D3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, COMP1_OUT, EVENTOUT	
B10	PB0	I/O	FT_a	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM1_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC12_INN5, ADC12_INP9, OPAMP1_VINP, COMP1_INP
A9	PB1	I/O	TT_u	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC12_INP5, COMP1_INM
B9	PB2	I/O	FT_ ha	-	RTC_OUT, SAI1_D1, DFSDM1_CKIN1, SAI1_SD_A, SPI3_MOSI/I2S3_SDO, SAI4_SD_A, QUADSPI_CLK, SAI4_D1, EVENTOUT	COMP1_INP
A7	PF11	I/O	FT_a	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT	ADC1_INP2
B8	PF14	I/O	FT_fha	-	DFSDM1_CKIN6, I2C4_SCL, FMC_A8, EVENTOUT	ADC2_INN2, ADC2_INP6
A6	PF15	I/O	FT_fh	-	I2C4_SDA, FMC_A9, EVENTOUT	-
B7	PE7	I/O	TT_ha	-	TIM1_ETR, DFSDM1_DATIN2, UART7_RX, QUADSPI_BK2_IO0, FMC_D4/FMC_DA4, EVENTOUT	OPAMP2_VOUT, COMP2_INM
A5	PE8	I/O	TT_ha	-	TIM1_CH1N, DFSDM1_CKIN2, UART7_TX, QUADSPI_BK2_IO1,	OPAMP2_VINM

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					FMC_D5/FMC_DA5, COMP2_OUT, EVENTOUT	
B6	PE9	I/O	TT_ha	-	TIM1_CH1, DFSDM1_CKOUT, UART7_RTS/UART7_DE, QUADSPI_BK2_IO2, FMC_D6/FMC_DA6, EVENTOUT	OPAMP2_VINP, COMP2_INP
A4	PE10	I/O	FT_ha	-	TIM1_CH2N, DFSDM1_DATIN4, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7/FMC_DA7, EVENTOUT	COMP2_INM
A3	PE11	I/O	FT_ha	-	TIM1_CH2, DFSDM1_CKIN4, SPI4_NSS, SAI2_SD_B, FMC_D8/FMC_DA8, LCD_G3, EVENTOUT	COMP2_INP
B5	PE12	I/O	FT_h	-	TIM1_CH3N, DFSDM1_DATIN5, SPI4_SCK, SAI2_SCK_B, FMC_D9/FMC_DA9, COMP1_OUT, LCD_B4, EVENTOUT	-
A2	PE13	I/O	FT_h	-	TIM1_CH3, DFSDM1_CKIN5, SPI4_MISO, SAI2_FS_B, FMC_D10/FMC_DA10, COMP2_OUT, LCD_DE, EVENTOUT	-
B4	PE14	I/O	FT_h	-	TIM1_CH4, SPI4_MOSI, SAI2_MCLK_B, FMC_D11/FMC_DA11, LCD_CLK, EVENTOUT	-
B3	PE15	I/O	FT_h	-	TIM1_BKIN, FMC_D12/FMC_DA12, TIM1_BKIN_COMP12/COMP_TIM1_BKIN, LCD_R7, EVENTOUT	-
B2	PB10	I/O	FT_f	-	TIM2_CH3, HRTIM_SCOUT, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK,	-

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					DFSDM1_DATIN7, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	
C3	PB11	I/O	FT_f	-	TIM2_CH4, HRTIM_SCIN, LPTIM2_ETR, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, LCD_G5, EVENTOUT	-
D1	PB12	I/O	FT_u	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN1, USART3_CK, FDCAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, TIM1_BKIN_COMP12, UART5_RX, EVENTOUT	-
D2	PB13	I/O	FT_u	-	TIM1_CH1N, LPTIM2_OUT, SPI2_SCK/I2S2_CK, DFSDM1_CKIN1, USART3_CTS/USART3_NSS, FDCAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, UART5_TX, EVENTOUT	OTG_HS_VBUS
D3	PB14	I/O	FT_u	-	TIM1_CH2N, TIM12_CH1, TIM8_CH2N, USART1_TX, SPI2_MISO/I2S2_SDI, DFSDM1_DATIN2, USART3_RTS/USART3_DE, UART4_RTS/UART4_DE, SDMMC2_D0, OTG_HS_DM, EVENTOUT	-

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
E1	PB15	I/O	FT_u	-	RTC_REFIN, TIM1_CH3N, TIM12_CH2, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SDO, DFSDM1_CKIN2, UART4_CTS, SDMMC2_D1, OTG_HS_DP, EVENTOUT	-
E2	PD8	I/O	FT_h	-	DFSDM1_CKIN3, SAI3_SCK_B, USART3_TX, SPDIFRX1_IN2, FMC_D13/FMC_DA13, EVENTOUT	-
E3	PD9	I/O	FT_h	-	DFSDM1_DATIN3, SAI3_SD_B, USART3_RX, FDCAN2_RXFD_MODE, FMC_D14/FMC_DA14, EVENTOUT	-
E4	PD10	I/O	FT_h	-	DFSDM1_CKOUT, SAI3_FS_B, USART3_CK, FDCAN2_TXFD_MODE, FMC_D15/FMC_DA15, LCD_B3, EVENTOUT	-
F1	PD11	I/O	FT_h	-	LPTIM2_IN2, I2C4_SMBA, USART3_CTS/USART3_NSS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16, EVENTOUT	-
F2	PD12	I/O	FT_fh	-	LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, I2C4_SCL, USART3_RTS/USART3_DE, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17, EVENTOUT	-
F3	PD13	I/O	FT_fh	-	LPTIM1_OUT, TIM4_CH2, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18,	-

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					EVENTOUT	
G1	PD14	I/O	FT_h	-	TIM4_CH3, SAI3_MCLK_B, UART8_CTS, FMC_D0/FMC_DA0, EVENTOUT	-
G2	PD15	I/O	FT_h	-	TIM4_CH4, SAI3_MCLK_A, UART8_RTS/UART8_DE, FMC_D1/FMC_DA1, EVENTOUT	-
G3	PG6	I/O	FT_h	-	TIM17_BKIN, HRTIM_CHE1, QUADSPI_BK1_NCS, FMC_NE3, DCMI_D12, LCD_R7, EVENTOUT	-
H3	PG7	I/O	FT_h	-	HRTIM_CHE2, SAI1_MCLK_A, USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT	-
H2	PG8	I/O	FT_h	-	TIM8_ETR, SPI6_NSS, USART6_RTS/USART6_DE, SPDIFRX1_IN3, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT	-
J3	PC6	I/O	FT_h	-	HRTIM_CHA1, TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, I2S2_MCK, USART6_TX, SDMMC1_D0DIR, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	SWPMI_IO
J4	PC7	I/O	FT_h	-	TRGIO, HRTIM_CHA2, TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, I2S3_MCK, USART6_RX, SDMMC1_D123DIR, FMC_NE1, SDMMC2_D7, SWPMI_TX,	-

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT	
J2	PC8	I/O	FT_h	-	TRACED1, HRTIM_CHB1, TIM3_CH3, TIM8_CH3, USART6_CK, UART5_RTS/UART5_DE, FMC_NE2/FMC_NCE, SWPMI_RX, SDMMC1_D0, DCMI_D2, EVENTOUT	-
K4	PC9	I/O	FT_fh	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, LCD_G3, SWPMI_SUSPEND, SDMMC1_D1, DCMI_D3, LCD_B2, EVENTOUT	-
K2	PA8	I/O	FT_fha	-	MCO1, TIM1_CH1, HRTIM_CHB2, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, UART7_RX, TIM8_BKIN2_COMP12, LCD_B3, LCD_R6, EVENTOUT	-
K3	PA9	I/O	FT_u	-	TIM1_CH2, HRTIM_CHC1, LPUART1_TX, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, FDCAN1_RXFD_MODE, DCMI_D0, LCD_R5, EVENTOUT	OTG_FS_VBUS
K1	PA10	I/O	FT_u	-	TIM1_CH3, HRTIM_CHC2, LPUART1_RX, USART1_RX, FDCAN1_TXFD_MODE, OTG_FS_ID, MDIOS_MDIO, LCD_B4, DCMI_D1, LCD_B1, EVENTOUT	-
L2	PA11	I/O	FT_u	-	TIM1_CH4,	-

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					HRTIM_CHD1, LPUART1_CTS, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS/USART1_NSS, FDCAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	
L1	PA12	I/O	FT_u	-	TIM1_ETR, HRTIM_CHD2, LPUART1_RTS/LPUART1_DE, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS/USART1_DE, SAI2_FS_B, FDCAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
L3	PA13(JTMS/SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
M4	PA14(JTCK/SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
M5	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, HRTIM_FLT1, CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS/UART4_DE, UART7_TX, EVENTOUT	-
N2	PC10	I/O	FT_ha	-	HRTIM_EEV1, DFSDM1_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT	-
N3	PC11	I/O	FT_h	-	HRTIM_FLT2, DFSDM1_DATIN5, SPI3_MISO/I2S3_SDI, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, DCMI_D4,	-

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					EVENTOUT	
P2	PC12	I/O	FT_h	-	TRACED3, HRTIM_EEV2, SPI3_MOSI/I2S3_SDO, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9, EVENTOUT	-
N4	PD0	I/O	FT_h	-	DFSDM1_CKIN6, SAI3_SCK_A, UART4_RX, FDCAN1_RX, FMC_D2/FMC_DA2, EVENTOUT	-
P3	PD1	I/O	FT_h	-	DFSDM1_DATIN6, SAI3_SD_A,UART4_TX, FDCAN1_TX, FMC_D3/FMC_DA3, EVENTOUT	-
R2	PD2	I/O	FT_h	-	TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, DCMI_D11, EVENTOUT	-
P4	PD3	I/O	FT_h	-	DFSDM1_CKOUT, SPI2_SCK/I2S2_CK, USART2_CTS/USART2_NSS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-
R3	PD4	I/O	FT_h	-	HRTIM_FLT3, SAI3_FS_A, USART2_RTS/USART2_DE, FDCAN1_RXFD_MODE, FMC_NOE, EVENTOUT	-
R4	PD5	I/O	FT_h	-	HRTIM_EEV3, USART2_TX, FDCAN1_TXFD_MODE, FMC_NWE, EVENTOUT	-
L6	PD6	I/O	FT_h	-	SAI1_D1, DFSDM1_CKIN4, DFSDM1_DATIN1, SPI3_MOSI/I2S3_SDO, SAI1_SD_A, USART2_RX,	-

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					SAI4_SD_A, FDCAN2_RXFD_MODE, SAI4_D1, SDMMC2_CK, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT	
N5	PD7	I/O	FT_h	-	DFSDM1_DATIN4, SPI1_MOSI/I2S1_SDO, DFSDM1_CKIN1, USART2_CK, SPDIFRX1_IN1, SDMMC2_CMD, FMC_NE1, EVENTOUT	-
M6	PG9	I/O	FT_h	-	SPI1_MISO/I2S1_SDI, USART6_RX, SPDIFRX1_IN4, QUADSPI_BK2_IO2, SAI2_FS_B, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT	-
M7	PG10	I/O	FT_h	-	HRTIM_FLT5, SPI1_NSS/I2S1_WS, LCD_G3, SAI2_SD_B, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT	-
L7	PG11	I/O	FT_h	-	LPTIM1_IN2, HRTIM_EEV4, SPI1_SCK/I2S1_CK, SPDIFRX1_IN1, SDMMC2_D2, ETH_MII_TX_EN/ETH_RMII_TX_EN, DCMI_D3, LCD_B3, EVENTOUT	-
L8	PG12	I/O	FT_h	-	LPTIM1_IN1, HRTIM_EEV5, SPI6_MISO, USART6_RTS/USART6_DE, SPDIFRX1_IN2, LCD_B4, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_NE4, LCD_B1, EVENTOUT	-
M8	PG13	I/O	FT_h	-	TRACED0,LPTIM1_OUT, HRTIM_EEV10, SPI6_SCK, USART6_CTS/USART6_	-

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					NSS, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24, LCD_R0, EVENTOUT	
M9	PG14	I/O	FT_h	-	TRACED1, LPTIM1_ETR, SPI6_MOSI, USART6_TX, QUADSPI_BK2_IO3, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_A25, LCD_B0, EVENTOUT	-
M10	PB3(JTDO/TRACESWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, HRTIM_FLT4, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK, SDMMC2_D2, CRS_SYNC, UART7_RX, EVENTOUT	-
L10	PB4(NJTRST)	I/O	FT	-	NJTRST, TIM16_BKIN, TIM3_CH1, HRTIM_EEV6, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_NSS/I2S2_WS, SPI6_MISO, SDMMC2_D3, UART7_TX, EVENTOUT	-
N11	PB5	I/O	FT	-	TIM17_BKIN, TIM3_CH2, HRTIM_EEV7, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, I2C4_SMBA, SPI3_MOSI/I2S3_SDO, SPI6_MOSI, FDCAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, UART5_RX, EVENTOUT	-
M11	PB6	I/O	FT_f	-	TIM16_CH1N, TIM4_CH1, HRTIM_EEV8, I2C1_SCL, CEC, I2C4_SCL, USART1_TX,	-

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					LPUART1_TX, FDCAN2_TX, QUADSPI_BK1_NCS, DFSDM1_DATIN5, FMC_SDNE1, DCMI_D5, UART5_TX, EVENTOUT	
R13	PB7	I/O	FT_fa	-	TIM17_CH1N, TIM4_CH2, HRTIM_EEV9, I2C1_SDA, I2C4_SDA, USART1_RX, LPUART1_RX, FDCAN2_TXFD_MODE, DFSDM1_CKIN5, FMC_NL, DCMI_VSYNC, EVENTOUT	PVD_IN
P13	BOOT0	I	B	-	-	VPP
P14	PB8	I/O	FT_fh	-	TIM16_CH1, TIM4_CH3, DFSDM1_CKIN7, I2C1_SCL, I2C4_SCL, SDMMC1_CKIN, UART4_RX, FDCAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT	-
N12	PB9	I/O	FT_fh	-	TIM17_CH1, TIM4_CH4, DFSDM1_DATIN7, I2C1_SDA, SPI2_NSS/I2S2_WS, I2C4_SDA, SDMMC1_CDIR, UART4_TX, FDCAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
N13	PE0	I/O	FT_h	-	LPTIM1_ETR, TIM4_ETR, HRTIM_SCIN, LPTIM2_ETR, UART8_RX, FDCAN1_RXFD_MODE, SAI2_MCLK_A, FMC_NBL0, DCMI_D2,	-

Pin No	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
					EVENTOUT	
L12	PE1	I/O	FT_h	-	LPTIM1_IN2, HRTIM_SCOUT, UART8_TX, FDCAN1_TXFD_MODE, FMC_NBL1, DCMI_D3, EVENTOUT	-
M14	PDR_ON	I	FT	-	-	-

1. When this ball was previously configured as an oscillator, the oscillator function is kept during and after a reset. This is valid for all resets except for power-on reset.
2. Pxy_C and Pxy balls are two separate pads (analog switch open). The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.
3. There is a direct path between Pxy_C and Pxy balls, through an analog switch. Pxy alternate functions are available on Pxy_C when the analog switch is closed. The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.

By port functions

Table 1.4-2: Port A alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/ SPDIFRX1	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX1	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD/CRS	I2C4/UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/ OTG1_FS/LCD	TIM1/ DCMI/LCD/ COMP	UART5/ LCD	SYS
Port A	PA0	-	TIM2_CH1/ TIM2_ETR	TIM5_CH1	TIM8_ETR	TIM15_BKIN	-	-	USART2_ CTS/ USART2_NSS	UART4_TX	SDMMC2_ CMD	SAI2_SD_B	ETH_MII_ CRS	-	-	-	EVENT OUT
	PA1	-	TIM2_CH2	TIM5_CH2	LPTIM3_ OUT	TIM15_ CH1N	-	-	USART2_ RTS/ USART2_DE	UART4_RX	QUADSPI_ BK1_IO3	SAI2_ MCLK_B	ETH_MII_RX _CLK/ETH_ RMII_REF_CLK	-	-	LCD_R2	EVENT OUT
	PA2	-	TIM2_CH3	TIM5_CH3	LPTIM4_ OUT	TIM15_CH1	-	-	USART2_ TX	SAI2_SCK _B	-	-	ETH_MDIO	MDIOS_ MDIO	-	LCD_R1	EVENT OUT
	PA3	-	TIM2_CH4	TIM5_CH4	LPTIM5_ OUT	TIM15_CH2	-	-	USART2_ RX	-	LCD_B2	OTG_HS_ ULPI_D0	ETH_MII_ COL	-	-	LCD_B5	EVENT OUT
	PA4	D1PWR EN	-	TIM5_ETR	-	-	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	USART2_ CK	SPI6_NSS	-	-	-	OTG_HS_ SOF	DCMI_ HSYNC	LCD_ VSYNC	EVENT OUT
	PA5	D2PWR EN	TIM2_CH1/ TIM2_ETR	-	TIM8_ CH1N	-	SPI1_SCK/ I2S1_CK	-	-	SPI6_SCK	-	OTG_HS_ ULPI_CK	-	-	-	LCD_R4	EVENT OUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_ MISO/I2S1 _SDI	-	-	SPI6_ MISO	TIM13_CH1	TIM8_BKIN _COMP12	MDIOS_ MDC	TIM1_BKIN _COMP12	DCMI_PIX CLK	LCD_G2	EVENT OUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_ CH1N	-	SPI1_ MOSI/I2S1 _SDO	-	-	SPI6_ MOSI	TIM14_CH1	-	ETH_MII_RX _DV/ETH_ RMII_CRS_DV	FMC_SDN WE	-	-	EVENT OUT
	PA8	MCO1	TIM1_CH1	HRTIM_ CHB2	TIM8_BKIN2	I2C3_SCL	-	-	USART1_ CK	-	-	OTG_FS_ SOF	UART7_RX	TIM8_BKIN 2_COMP12	LCD_B3	LCD_R6	EVENT OUT
	PA9	-	TIM1_CH2	HRTIM_ CHC1	LPUART1_TX	I2C3_SMBA	SPI2_SCK/ I2S2_CK	-	USART1_ TX	-	FDCAN1_ RXFD_ MODE	-	-	-	DCMI_D0	LCD_R5	EVENT OUT
	PA10	-	TIM1_CH3	HRTIM_ CHC2	LPUART1_ RX	-	-	-	USART1_ RX	-	FDCAN1_ TXFD_MODE	OTG_FS_ID	MDIOS_ MDIO	LCD_B4	DCMI_D1	LCD_B1	EVENT OUT
	PA11	-	TIM1_CH4	HRTIM_ CHD1	LPUART1_ CTS	-	SPI2_NSS/ I2S2_WS	UART4_RX	USART1_ CTS/ USART1_NSS	-	FDCAN1_ RX	OTG_FS_ DM	-	-	-	LCD_R4	EVENT OUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/ 4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4 /5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/ 5/6/CEC	SPI2/3/SAI1 /3/I2C4 / UART4/ DFSDM	SPI2/3/6/ USART1/2/ 3/6/UART7 /SDMMC1	SPI6/SAI2/ 4/UART4/5 /8/LPUART /SDMMC1/ SPDIFRX1	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX1	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD/CRS	I2C4/UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FM C/SDMMC1 /MDIOS/ OTG1_FS/LCD	TIM1/ DCMI/LCD/ COMP	UART5/ LCD	SYS
Port A	PA12	-	TIM1_ETR	HRTIM_ CHD2	LPUART1_ RTS/ LPUART1_DE	-	SPI2_SCK/ I2S2_CK	UART4_TX	USART1_ RTS/ USART1_DE	SAI2_FS_B	FDCAN1_ TX	OTG_FS_ DP	-	-	-	LCD_R5	EVENT OUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA15	JTDI	TIM2_CH1/ TIM2_ETR	HRTIM_ FLT1	-	CEC	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	SPI6_NSS	UART4_ RTS/UART 4_DE	-	-	UART7_TX	-	-	-	EVENT OUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD/CRS	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	DFSDM1_CKOUT	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	LCD_G1	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_DATIN1	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	LCD_G0	EVENTOUT
	PB2	RTC_OUT	-	SAI1_D1	-	DFSDM1_CKIN1	-	SAI1_SD_A	SPI3_MOSI/I2S3_SDO	SAI4_SD_A	QUADSPI_CLK	SAI4_D1	-	-	-	-	EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	HRTIM_FLT4	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	SPI6_SCK	SDMMC2_D2	CRS_SYNC	UART7_RX	-	-	-	EVENTOUT
	PB4	NJTRST	TIM16_BKIN	TIM3_CH1	HRTIM_EEV6	-	SPI1_MISO/I2S1_SDI	SPI3_MISO/I2S3_SDI	SPI2_NSS/I2S2_WS	SPI6_MISO	SDMMC2_D3	-	UART7_TX	-	-	-	EVENTOUT
	PB5	-	TIM17_BKIN	TIM3_CH2	HRTIM_EEV7	I2C1_SMBA	SPI1_MOSI/I2S1_SDO	I2C4_SMBA	SPI3_MOSI/I2S3_SDO	SPI6_MOSI	FDCAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SDCKE1	DCMI_D10	UART5_RX	EVENTOUT
	PB6	-	TIM16_CH1N	TIM4_CH1	HRTIM_EEV8	I2C1_SCL	CEC	I2C4_SCL	USART1_TX	LPUART1_TX	FDCAN2_TX	QUADSPI_BK1_NCS	DFSDM1_DATIN5	FMC_SDNE1	DCMI_D5	UART5_TX	EVENTOUT
	PB7	-	TIM17_CH1N	TIM4_CH2	HRTIM_EEV9	I2C1_SDA	-	I2C4_SDA	USART1_RX	LPUART1_RX	FDCAN2_TXFD_MODE	-	DFSDM1_CKIN5	FMC_NL	DCMI_VSYNC	-	EVENTOUT
	PB8	-	TIM16_CH1	TIM4_CH3	DFSDM1_CKIN7	I2C1_SCL	-	I2C4_SCL	SDMMC1_CKIN	UART4_RX	FDCAN1_RX	SDMMC2_D4	ETH_MII_TXD3	SDMMC1_D4	DCMI_D6	LCD_B6	EVENTOUT
	PB9	-	TIM17_CH1	TIM4_CH4	DFSDM1_DATIN7	I2C1_SDA	SPI2_NSS/I2S2_WS	I2C4_SDA	SDMMC1_CDIR	UART4_TX	FDCAN1_TX	SDMMC2_D5	I2C4_SMBA	SDMMC1_D5	DCMI_D7	LCD_B7	EVENTOUT
	PB10	-	TIM2_CH3	HRTIM_SCOUT	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/I2S2_CK	DFSDM1_DATIN7	USART3_TX	-	QUADSPI_BK1_NCS	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	LCD_G4	EVENTOUT
	PB11	-	TIM2_CH4	HRTIM_SCIN	LPTIM2_ETR	I2C2_SDA	-	DFSDM1_CKIN7	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	-	LCD_G5	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	DFSDM1_DATIN1	USART3_CK	-	FDCAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0/ETH_RMII_TXD0	OTG_HS_ID	TIM1_BKIN_COMP12	UART5_RX	EVENTOUT
	PB13	-	TIM1_CH1N	-	LPTIM2_OUT	-	SPI2_SCK/I2S2_CK	DFSDM1_CKIN1	USART3_CTS/USART3_NSS	-	FDCAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1/ETH_RMII_TXD1	-	-	UART5_TX	EVENTOUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/ 4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4 /5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/ 5/6/CEC	SPI2/3/SAI1 /3/I2C4 / UART4/ DFSDM	SPI2/3/6/ USART1/2/ 3/6/UART7 /SDMMC1	SPI6/SAI2/ 4/UART4/5 /8/LPUART /SDMMC1/ SPDIFRX1	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX1	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD/CRS	I2C4/UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FM C/SDMMC1 /MDIOS/ OTG1_FS/ LCD	TIM1/ DCMI/LCD/ COMP	UART5/ LCD	SYS
Port B	PB14	-	TIM1_CH2N	TIM12_CH1	TIM8_CH2N	USART1_TX	SPI2_ MISO/I2S2 _SDI	DFSDM1_ DATIN2	USART3_ RTS/USAR T3_DE	UART4_ RTS/UART 4_DE	SDMMC2_ D0	-	-	OTG_HS_ DM	-	-	EVENT OUT
	PB15	RTC_ REFIN	TIM1_CH3N	TIM12_CH2	TIM8_CH3N	USART1_RX	SPI2_ MOSI/I2S2 _SDO	DFSDM1_ CKIN2	-	UART4_ CTS	SDMMC2_D1	-	-	OTG_HS_ DP	-	-	EVENT OUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD/CRS	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port C	PC0	-	-	-	DFSDM1_CKIN0	-	-	DFSDM1_DATIN4	-	SAI2_FS_B	-	OTG_HS_ULPI_STP	-	FMC_SDNWE	-	LCD_R5	EVENTOUT
	PC1	TRACED0	-	SAI1_D1	DFSDM1_DATIN0	DFSDM1_CKIN4	SPI2_MOSI/I2S2_SDO	SAI1_SD_A	-	SAI4_SD_A	SDMMC2_CK	SAI4_D1	ETH_MDC	MDIOS_MDC	-	-	EVENTOUT
	PC2	C1DSLEEP	-	-	DFSDM1_CKIN1	-	SPI2_MISO/I2S2_SDI	DFSDM1_CKOUT	-	-	-	OTG_HS_ULPI_DIR	ETH_MII_TXD2	FMC_SDNE0	-	-	EVENTOUT
	PC3	C1SLEEP	-	-	DFSDM1_DATIN1	-	SPI2_MOSI/I2S2_SDO	-	-	-	-	OTG_HS_ULPI_NXT	ETH_MII_TX_CLK	FMC_SDCKE0	-	-	EVENTOUT
	PC4	C2DSLEEP	-	-	DFSDM1_CKIN2	-	I2S1_MCK	-	-	-	SPDIFRX1_IN3	-	ETH_MII_RXD0/ETH_RMII_RXD0	FMC_SDNE0	-	-	EVENTOUT
	PC5	C2SLEEP	-	SAI1_D3	DFSDM1_DATIN2	-	-	-	-	-	SPDIFRX1_IN4	SAI4_D3	ETH_MII_RXD1/ETH_RMII_RXD1	FMC_SDCKE0	COMP1_OUT	-	EVENTOUT
	PC6	-	HRTIM_CHA1	TIM3_CH1	TIM8_CH1	DFSDM1_CKIN3	I2S2_MCK	-	USART6_TX	SDMMC1_D0DIR	FMC_NWAIT	SDMMC2_D6	-	SDMMC1_D6	DCMI_D0	LCD_HSYNC	EVENTOUT
	PC7	TRGIO	HRTIM_CHA2	TIM3_CH2	TIM8_CH2	DFSDM1_DATIN3	-	I2S3_MCK	USART6_RX	SDMMC1_D123DIR	FMC_NE1	SDMMC2_D7	SWPMI_TX	SDMMC1_D7	DCMI_D1	LCD_G6	EVENTOUT
	PC8	TRACED1	HRTIM_CHB1	TIM3_CH3	TIM8_CH3	-	-	-	USART6_CK	UART5_RTS/UART5_DE	FMC_NE2/FMC_NCE	-	SWPMI_RX	SDMMC1_D0	DCMI_D2	-	EVENTOUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	-	UART5_CTS	QUADSPI_BK1_IO0	LCD_G3	SWPMI_SUSPEND	SDMMC1_D1	DCMI_D3	LCD_B2	EVENTOUT
	PC10	-	-	HRTIM_EEV1	DFSDM1_CKIN5	-	-	SPI3_SCK/I2S3_CK	USART3_TX	UART4_TX	QUADSPI_BK1_IO1	-	-	SDMMC1_D2	DCMI_D8	LCD_R2	EVENTOUT
	PC11	-	-	HRTIM_FLT2	DFSDM1_DATIN5	-	-	SPI3_MISO/I2S3_SDI	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	-	-	SDMMC1_D3	DCMI_D4	-	EVENTOUT
	PC12	TRACED3	-	HRTIM_EEV2	-	-	-	SPI3_MOSI/I2S3_SDO	USART3_CK	UART5_TX	-	-	-	SDMMC1_CK	DCMI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/ SPDIFRX1	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX1	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD/CRS	I2C4/UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/ OTG1_FS/ LCD	TIM1/ DCMI/LCD/ COMP	UART5/ LCD	SYS
Port C	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/ 4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4 /5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/ 5/6/CEC	SPI2/3/SAI1 /3/I2C4 / UART4/ DFSDM	SPI2/3/6/ USART1/2/3/ 6/UART7/SD MMC1	SPI6/SAI2/ 4/UART4/5 /8/LPUART /SDMMC1/ SPDIFRX1	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX1	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD/CRS	I2C4/UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FM C/SDMMC1 /MDIOS/ OTG1_FS/ LCD	TIM1/ DCMI/LCD/ COMP	UART5/ LCD	SYS
Port D	PD0	-	-	-	DFSDM1_ CKIN6	-	-	SAI3_SCK_A	-	UART4_RX	FDCAN1_ RX	-	-	FMC_D2/ FMC_DA2	-	-	EVENT OUT
	PD1	-	-	-	DFSDM1_ DATIN6	-	-	SAI3_SD_A	-	UART4_TX	FDCAN1_ TX	-	-	FMC_D3/ FMC_DA3	-	-	EVENT OUT
	PD2	TRACE D2	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDMMC1_ CMD	DCMI_D11	-	EVENT OUT
	PD3	-	-	-	DFSDM1_ CKOUT	-	SPI2_SCK/ I2S2_CK	-	USART2_CTS/ USART2_NSS	-	-	-	-	FMC_CLK	DCMI_D5	LCD_G7	EVENT OUT
	PD4	-	-	HRTIM_ FLT3	-	-	-	SAI3_FS_A	USART2_ RTS/USART2 _DE	-	FDCAN1_ RXFD_ MODE	-	-	FMC_NOE	-	-	EVENT OUT
	PD5	-	-	HRTIM_EE V3	-	-	-	-	USART2_ TX	-	FDCAN1_ TXFD_ MODE	-	-	FMC_NWE	-	-	EVENT OUT
	PD6	-	-	SAI1_D1	DFSDM1_ CKIN4	DFSDM1_ DATIN1	SPI3_ MOSI/I2S3 _SDO	SAI1_SD_A	USART2_ RX	SAI4_SD_A	FDCAN2_ RXFD_ MODE	SAI4_D1	SDMMC2_ CK	FMC_ NWAIT	DCMI_D10	LCD_B2	EVENT OUT
	PD7	-	-	-	DFSDM1_ DATIN4	-	SPI1_ MOSI/I2S1 _SDO	DFSDM1_ CKIN1	USART2_ CK	-	SPDIFRX1_ IN1	-	SDMMC2_ CMD	FMC_NE1	-	-	EVENT OUT
	PD8	-	-	-	DFSDM1_ CKIN3	-	-	SAI3_SCK_B	USART3_ TX	-	SPDIFRX1_ IN2	-	-	FMC_D13/ FMC_DA13	-	-	EVENT OUT
	PD9	-	-	-	DFSDM1_ DATIN3	-	-	SAI3_SD_B	USART3_ RX	-	FDCAN2_ RXFD_ MODE	-	-	FMC_D14/ FMC_DA14	-	-	EVENT OUT
	PD10	-	-	-	DFSDM1_ CKOUT	-	-	SAI3_FS_B	USART3_ CK	-	FDCAN2_ TXFD_ MODE	-	-	FMC_D15/ FMC_DA15	-	LCD_B3	EVENT OUT
	PD11	-	-	-	LPTIM2_ IN2	I2C4_SMBA	-	-	USART3_CTS/ USART3_NSS	-	QUADSPI_ BK1_IO0	SAI2_SD_A	-	FMC_A16	-	-	EVENT OUT
	PD12	-	LPTIM1_IN1	TIM4_CH1	LPTIM2_IN1	I2C4_SCL	-	-	USART3_ RTS/ USART3_ DE	-	QUADSPI_ BK1_IO1	SAI2_FS_A	-	FMC_A17	-	-	EVENT OUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/ SPDIFRX1	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX1	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD/CRS	I2C4/UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/ OTG1_FS/ LCD	TIM1/ DCMI/LCD/ COMP	UART5/ LCD	SYS
Prot D	PD13	-	LPTIM1_ OUT	TIM4_CH2	-	I2C4_SDA	-	-	-	-	QUADSPI_ BK1_IO3	SAI2_SCK_A	-	FMC_A18	-	-	EVENT OUT
	PD14	-	-	TIM4_CH3	-	-	-	SAI3_MCLK_B	-	UART8_ CTS	-	-	-	FMC_D0/ FMC_DA0	-	-	EVENT OUT
	PD15	-	-	TIM4_CH4	-	-	-	SAI3_MCLK_A	-	UART8_RTS/ UART8_DE	-	-	-	FMC_D1/ FMC_DA1	-	-	EVENT OUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/ SPDIFRX1	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX1	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD/CRS	I2C4/UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/ OTG1_FS/ LCD	TIM1/ DCMI/LCD/ COMP	UART5/ LCD	SYS
Port E	PE0	-	LPTIM1_ ETR	TIM4_ETR	HRTIM_ SCIN	LPTIM2_ ETR	-	-	-	UART8_RX	FDCAN1_ RXFD_ MODE	SAI2_ MCLK_A	-	FMC_NBL0	DCMI_D2	-	EVENT OUT
	PE1	-	LPTIM1_IN2	-	HRTIM_ SCOUT	-	-	-	-	UART8_TX	FDCAN1_ TXFD_ MODE	-	-	FMC_NBL1	DCMI_D3	-	EVENT OUT
	PE2	TRACE CLK	-	SAI1_CK1	-	-	SPI4_SCK	SAI1_MCLK_A	-	SAI4_ MCLK_A	QUADSPI_ BK1_IO2	SAI4_CK1	ETH_MII_TX D3	FMC_A23	-	-	EVENT OUT
	PE3	TRACE D0	-	-	-	TIM15_BKIN	-	SAI1_SD_B	-	SAI4_SD_B	-	-	-	FMC_A19	-	-	EVENT OUT
	PE4	TRACE D1	-	SAI1_D2	DFSDM1_ DATIN3	TIM15_CH1N	SPI4_NSS	SAI1_FS_A	-	SAI4_FS_A	-	SAI4_D2	-	FMC_A20	DCMI_D4	LCD_B0	EVENT OUT
	PE5	TRACE D2	-	SAI1_CK2	DFSDM1_ CKIN3	TIM15_CH1	SPI4_ MISO	SAI1_SCK_A	-	SAI4_SCK_A	-	SAI4_CK2	-	FMC_A21	DCMI_D6	LCD_G0	EVENT OUT
	PE6	TRACE D3	TIM1_BKIN2	SAI1_D1	-	TIM15_CH2	SPI4_ MOSI	SAI1_SD_A	-	SAI4_SD_A	SAI4_D1	SAI2_ MCLK_B	TIM1_BKIN2_COMP12	FMC_A22	DCMI_D7	LCD_G1	EVENT OUT
	PE7	-	TIM1_ETR	-	DFSDM1_ DATIN2	-	-	-	UART7_RX	-	-	QUADSPI_ BK2_IO0	-	FMC_D4/ FMC_DA4	-	-	EVENT OUT
	PE8	-	TIM1_CH1N	-	DFSDM1_ CKIN2	-	-	-	UART7_TX	-	-	QUADSPI_ BK2_IO1	-	FMC_D5/ FMC_DA5	COMP2_ OUT	-	EVENT OUT
	PE9	-	TIM1_CH1	-	DFSDM1_ CKOUT	-	-	-	UART7_RTS/ UART7_DE	-	-	QUADSPI_ BK2_IO2	-	FMC_D6/ FMC_DA6	-	-	EVENT OUT
	PE10	-	TIM1_CH2N	-	DFSDM1_ DATIN4	-	-	-	UART7_ CTS	-	-	QUADSPI_ BK2_IO3	-	FMC_D7/ FMC_DA7	-	-	EVENT OUT
	PE11	-	TIM1_CH2	-	DFSDM1_ CKIN4	-	SPI4_NSS	-	-	-	-	SAI2_SD_B	-	FMC_D8/ FMC_DA8	-	LCD_G3	EVENT OUT
	PE12	-	TIM1_CH3N	-	DFSDM1_ DATIN5	-	SPI4_SCK	-	-	-	-	SAI2_SCK_B	-	FMC_D9/ FMC_DA9	COMP1_ OUT	LCD_B4	EVENT OUT
	PE13	-	TIM1_CH3	-	DFSDM1_ CKIN5	-	SPI4_ MISO	-	-	-	-	SAI2_FS_B	-	FMC_D10/ FMC_DA10	COMP2_ OUT	LCD_DE	EVENT OUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/ SPDIFRX1	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX1	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD/CRS	I2C4/UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/ OTG1_FS/ LCD	TIM1/ DCMI/LCD/ COMP	UART5/ LCD	SYS
Prot E	PE14	-	TIM1_CH4	-	-	-	SPI4_ MOSI	-	-	-	-	SAI2_MCLK_B	-	FMC_D11/ FMC_DA11	-	LCD_CLK	EVENT OUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	-	FMC_D12/ FMC_DA12	TIM1_BKIN_COMP12/ COMP_ TIM1_BKIN	LCD_R7	EVENT OUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/ SPDIFRX1	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX1	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD/CRS	I2C4/UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/ OTG1_FS/ LCD	TIM1/ DCMI/LCD/ COMP	UART5/ LCD	SYS
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FMC_A0	-	-	EVENT OUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FMC_A1	-	-	EVENT OUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FMC_A2	-	-	EVENT OUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	EVENT OUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A4	-	-	EVENT OUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	EVENT OUT
	PF6	-	TIM16_CH1	-	-	-	SPI5_NSS	SAI1_SD_B	UART7_RX	SAI4_SD_B	QUADSPI_ BK1_IO3	-	-	-	-	-	EVENT OUT
	PF7	-	TIM17_CH1	-	-	-	SPI5_SCK	SAI1_MCLK_B	UART7_TX	SAI4_ MCLK_B	QUADSPI_ BK1_IO2	-	-	-	-	-	EVENT OUT
	PF8	-	TIM16_CH1N	-	-	-	SPI5_ MISO	SAI1_SCK_B	UART7_RTS/ UART7_DE	SAI4_SCK_B	TIM13_CH1	QUADSPI_ BK1_IO0	-	-	-	-	EVENT OUT
	PF9	-	TIM17_CH1N	-	-	-	SPI5_ MOSI	SAI1_FS_B	UART7_ CTS	SAI4_FS_B	TIM14_CH1	QUADSPI_ BK1_IO1	-	-	-	-	EVENT OUT
	PF10	-	TIM16_BKIN	SAI1_D3	-	-	-	-	-	-	QUADSPI_ CLK	SAI4_D3	-	-	DCMI_D11	LCD_DE	EVENT OUT
	PF11	-	-	-	-	-	SPI5_ MOSI	-	-	-	-	SAI2_SD_B	-	FMC_ SDNRAS	DCMI_D12	-	EVENT OUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVENT OUT
	PF13	-	-	-	DFSDM1_ DATIN6	I2C4_SMBA	-	-	-	-	-	-	-	FMC_A7	-	-	EVENT OUT
	PF14	-	-	-	DFSDM1_ CKIN6	I2C4_SCL	-	-	-	-	-	-	-	FMC_A8	-	-	EVENT OUT
	PF15	-	-	-	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_A9	-	-	EVENT OUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/ SPDIFRX1	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX1	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD/CRS	I2C4/UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/ OTG1_FS/ LCD	TIM1/ DCMI/LCD/ COMP	UART5/ LCD	SYS
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVENT OUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVENT OUT
	PG2	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	TIM8_BKIN_COMP12	FMC_A12	-	-	EVENT OUT
	PG3	-	-	-	TIM8_BKIN2	-	-	-	-	-	-	-	TIM8_BKIN2_COMP12	FMC_A13	-	-	EVENT OUT
	PG4	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-	TIM1_BKIN2_COMP12	FMC_A14/ FMC_BA0	-	-	EVENT OUT
	PG5	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	-	FMC_A15/ FMC_BA1	-	-	EVENT OUT
	PG6	-	TIM17_ BKIN	HRTIM_ CHE1	-	-	-	-	-	-	-	QUADSPI_ BK1_NCS	-	FMC_NE3	DCMI_D12	LCD_R7	EVENT OUT
	PG7	-	-	HRTIM_ CHE2	-	-	-	SAI1_MCLK_A	USART6_ CK	-	-	-	-	FMC_INT	DCMI_D13	LCD_CLK	EVENT OUT
	PG8	-	-	-	TIM8_ETR	-	SPI6_NSS	-	USART6_ RTS/ USART6_DE	SPDIFRX1_ IN3	-	-	ETH_PPS_ OUT	FMC_ SDCLK	-	LCD_G7	EVENT OUT
	PG9	-	-	-	-	-	SPI1_ MISO/I2S1_SDI	-	USART6_ RX	SPDIFRX1_ IN4	QUADSPI_ BK2_IO2	SAI2_FS_B	-	FMC_NE2/ FMC_NCE	DCMI_ VSYNC	-	EVENT OUT
	PG10	-	-	HRTIM_ FLT5	-	-	SPI1_NSS/ I2S1_WS	-	-	-	LCD_G3	SAI2_SD_B	-	FMC_NE3	DCMI_D2	LCD_B2	EVENT OUT
	PG11	-	LPTIM1_IN2	HRTIM_ EEV4	-	-	SPI1_SCK/ I2S1_CK	-	-	SPDIFRX1_ IN1	-	SDMMC2_ D2	ETH_MII_ TX_EN/ETH_RMII_TX_EN	-	DCMI_D3	LCD_B3	EVENT OUT
	PG12	-	LPTIM1_IN1	HRTIM_ EEV5	-	-	SPI6_ MISO	-	USART6_ RTS/ USART6_DE	SPDIFRX1_IN2	LCD_B4	-	ETH_MII_TX D1/ETH_ RMII_TXD1	FMC_NE4	-	LCD_B1	EVENT OUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/ SPDIFRX1	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX1	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD/CRS	I2C4/UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/ OTG1_FS/ LCD	TIM1/ DCMI/LCD/ COMP	UART5/ LCD	SYS
Port G	PG13	TRACED0	LPTIM1_OUT	HRTIM_EEV10	-	-	SPI6_SCK	-	USART6_CTS/ USART6_NSS	-	-	-	ETH_MII_TXD0/ETH_RMII_TXD0	FMC_A24	-	LCD_R0	EVENTOUT
	PG14	TRACED1	LPTIM1_ETR	-	-	-	SPI6_MOSI	-	USART6_TX	-	QUADSPI_BK2_IO3	-	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_A25	-	LCD_B0	EVENTOUT
	PG15	-	-	-	-	-	-	-	USART6_CTS/ USART6_NSS	-	-	-	-	FMC_SDNCAS	DCMI_D13	-	EVENTOUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD/CRS	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	LPTIM1_IN2	-	-	-	-	-	-	-	QUADSPI_BK2_IO0	SAI2_SCK_B	ETH_MII_CRS	FMC_SDCKE0	-	LCD_R0	EVENTOUT
	PH3	-	-	-	-	-	-	-	-	-	QUADSPI_BK2_IO1	SAI2_MCLK_B	ETH_MII_COL	FMC_SDNE0	-	LCD_R1	EVENTOUT
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	LCD_G5	OTG_HS_ULPI_NXT	-	-	-	LCD_G4	EVENTOUT
	PH5	-	-	-	-	I2C2_SDA	SPI5_NSS	-	-	-	-	-	-	FMC_SDNWE	-	-	EVENTOUT
	PH6	-	-	TIM12_CH1	-	I2C2_SMBA	SPI5_SCK	-	-	-	-	-	ETH_MII_RXD2	FMC_SDNE1	DCMI_D8	-	EVENTOUT
	PH7	-	-	-	-	I2C3_SCL	SPI5_MISO	-	-	-	-	-	ETH_MII_RXD3	FMC_SDCKE1	DCMI_D9	-	EVENTOUT
	PH8	-	-	TIM5_ETR	-	I2C3_SDA	-	-	-	-	-	-	-	FMC_D16	DCMI_HSYNC	LCD_R2	EVENTOUT
	PH9	-	-	TIM12_CH2	-	I2C3_SMBA	-	-	-	-	-	-	-	FMC_D17	DCMI_D0	LCD_R3	EVENTOUT
	PH10	-	-	TIM5_CH1	-	I2C4_SMBA	-	-	-	-	-	-	-	FMC_D18	DCMI_D1	LCD_R4	EVENTOUT
	PH11	-	-	TIM5_CH2	-	I2C4_SCL	-	-	-	-	-	-	-	FMC_D19	DCMI_D2	LCD_R5	EVENTOUT
	PH12	-	-	TIM5_CH3	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_D20	DCMI_D3	LCD_R6	EVENTOUT
	PH13	-	-	-	TIM8_CH1N	-	-	-	-	UART4_TX	FDCAN1_TX	-	-	FMC_D21	-	LCD_G2	EVENTOUT
	PH14	-	-	-	TIM8_CH2N	-	-	-	-	UART4_RX	FDCAN1_RX	-	-	FMC_D22	DCMI_D4	LCD_G3	EVENTOUT
	PH15	-	-	-	TIM8_CH3N	-	-	-	-	-	FDCAN1_TXFD_MODE	-	-	FMC_D23	DCMI_D11	LCD_G4	EVENTOUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD/CRS	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	FDCAN1_RXFD_MODE	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENTOUT
	PI1	-	-	-	TIM8_BKIN2	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	TIM8_BKIN2_COMP12	FMC_D25	DCMI_D8	LCD_G6	EVENTOUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO/I2S2_SDI	-	-	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENTOUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SDO	-	-	-	-	-	-	FMC_D27	DCMI_D10	-	EVENTOUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	SAI2_MCLK_A	TIM8_BKIN_COMP12	FMC_NBL2	DCMI_D5	LCD_B4	EVENTOUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	SAI2_SCK_A	-	FMC_NBL3	DCMI_VSYNC	LCD_B5	EVENTOUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	SAI2_SD_A	-	FMC_D28	DCMI_D6	LCD_B6	EVENTOUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	SAI2_FS_A	-	FMC_D29	DCMI_D7	LCD_B7	EVENTOUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI9	-	-	-	-	-	-	-	-	UART4_RX	FDCAN1_RX	-	-	FMC_D30	-	LCD_VSYNC	EVENTOUT
	PI10	-	-	-	-	-	-	-	-	-	FDCAN1_RXFD_MODE	-	ETH_MII_RX_ER	FMC_D31	-	LCD_HSYNC	EVENTOUT
	PI11	-	-	-	-	-	-	-	-	-	LCD_G6	OTG_HS_ULPI_DIR	-	-	-	-	EVENTOUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_HSYNC	EVENTOUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VSYNC	EVENTOUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENTOUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	-	LCD_R0	EVENTOUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD/CRS	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port J	PJ0	-	-	-	-	-	-	-	-	-	LCD_R7	-	-	-	-	LCD_R1	EVENTOUT
	PJ1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R2	EVENTOUT
	PJ2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R3	EVENTOUT
	PJ3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R4	EVENTOUT
	PJ4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R5	EVENTOUT
	PJ5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	EVENTOUT
	PJ6	-	-	-	TIM8_CH2	-	-	-	-	-	-	-	-	-	-	LCD_R7	EVENTOUT
	PJ7	TRGIN	-	-	TIM8_CH2N	-	-	-	-	-	-	-	-	-	-	LCD_G0	EVENTOUT
	PJ8	-	TIM1_CH3N	-	TIM8_CH1	-	-	-	-	UART8_TX	-	-	-	-	-	LCD_G1	EVENTOUT
	PJ9	-	TIM1_CH3	-	TIM8_CH1N	-	-	-	-	UART8_RX	-	-	-	-	-	LCD_G2	EVENTOUT
	PJ10	-	TIM1_CH2N	-	TIM8_CH2	-	SPI5_MOSI	-	-	-	-	-	-	-	-	LCD_G3	EVENTOUT
	PJ11	-	TIM1_CH2	-	TIM8_CH2N	-	SPI5_μMISO	-	-	-	-	-	-	-	-	LCD_G4	EVENTOUT
	PJ12	TRGOUT	-	-	-	-	-	-	-	-	LCD_G3	-	-	-	-	LCD_B0	EVENTOUT
	PJ13	-	-	-	-	-	-	-	-	-	LCD_B4	-	-	-	-	LCD_B1	EVENTOUT
	PJ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B2	EVENTOUT
	PJ15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B3	EVENTOUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/ SPDIFRX1	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX1	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD/CRS	I2C4/UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/ OTG1_FS/ LCD	TIM1/ DCMI/LCD/ COMP	UART5/ LCD	SYS
Port K	PK0	-	TIM1_CH1N	-	TIM8_CH3	-	SPI5_SCK	-	-	-	-	-	-	-	-	LCD_G5	EVENT OUT
	PK1	-	TIM1_CH1	-	TIM8_CH3N	-	SPI5_NSS	-	-	-	-	-	-	-	-	LCD_G6	EVENT OUT
	PK2	-	TIM1_BKIN	-	TIM8_BKIN	-	-	-	-	-	-	TIM8_BKIN_COMP12	TIM1_BKIN_COMP12	-	-	LCD_G7	EVENT OUT
	PK3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B4	EVENT OUT
	PK4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B5	EVENT OUT
	PK5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B6	EVENT OUT
	PK6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B7	EVENT OUT
	PK7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DE	EVENT OUT

1.4.2 ESC Sub-system Pin Description

Following abbreviations are used in "Type" column of below pin description tables. Note that some I/O pins with multiple signal definitions on the same pin may have different attributes in "Type" column for different signal definition

A	Analog	**PU**	Internal Pull-Up
B5	Bi-directional I/O, 3.3V with 5V tolerant	**PD**	Internal Pull-Down
I5	Input, 3.3V with 5V tolerant	**P**	Power/Ground pin
O5	Output, 3.3V with 5V tolerant	**S**	Schmitt Trigger
B3	Bi-directional I/O, 3.3V	**T**	Tri-state
I3	Input, 3.3V	**4m**	4mA driving strength
O3	Output, 3.3V	**8m**	8mA driving strength

The multi-function pin settings are configured by the I^2C Hardware Configuration EEPROM (HWCFGEE). Please refer to Section **2.45.4.2** for details.

Pin No	Pin Name	Type	Description
E12	TEST	I5/PD/S	Test mode enable For normal operation, please always tie to logic low or NC.
F12	NC	I3	Reserved. Please connect to GND.
C13	RSTn	I5/PU/S	Reset Input, active low RST_N is the hardware reset input used to reset this chip. This input is logic AND with internal Power-On-Reset (POR) circuit, which generates the main system reset for this chip.
B13	RSTO\ RSTO_POL	O5/8m	Reset Output This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the RSTO polarity, please refer to Section 2.45.4.1.
M1	LED_RUN\ EEP_SIZE	B5/4m	RUN LED This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the EEPROM size configuration, please refer to Section 2.45.4.1.
M2	LED_ERR\ 3PORT_MODE	B5/4m	Error LED This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the Port 2 MII enable configuration, please refer to Section 2.45.4.1.
L14	P0_ACT\ P0_FIBER	B5/4m	PHY 0 Link/Activity LED This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the PHY 0 media mode, please refer to Section 2.45.4.1.
M13	P1_ACT\ P1_FIBER	B5/4m	PHY 1 Link/Activity LED This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the PHY 1 media mode, please refer to Section 2.45.4.1.
G4	SYNC_LATCH[1]	B5/8m	Distributed Clocks SyncSignal output or LatchSignal input 1
F4	SYNC_LATCH[0]	B5/8m	Distributed Clocks SyncSignal output or LatchSignal input 0
M3	EEP_DONE	O5/8m	This pin asserted high indicates that the EEPROM

Pin No	Pin Name	Type	Description
			is successfully loaded (Checksum matched) and the PDI can be used.
C11	PDI_EMU	I5	PDI Emulation enable
A8	OE_EXT	I5	Output Enable
	LRDn	I5	Local bus Read
	SCLK	I5	SPI Clock
C2	SOF	O5/8m	Start-of-Frame
	LECSn	I5	Local bus ESC Chip Select
	SCS_ESC	I5	SPI Chip Select for ESC
C5	OUTVLD	O5/8m	Output data Valid/Output event
	LWRn	I5	Local bus Write
	MOSI	I5	SPI data MOSI
D4	EOF	O5/8m	End-of-Frame
	LFCSn	I5	Local bus Function Chip Select
	SCS_FUNC	I5	SPI Chip Select for Function
D5	WD_TRIG	O5/8m	Watchdog Trigger
	LINT	O5/T	Local bus Interrupt
	SINT	O5/T	SPI Interrupt
D11	SCL	O5/T/4m /S	I2C Serial Clock line for I2C master controller SCL is a tri-stateable output, which requires an external pull-up resistor.
A10	SDA	B5/T/4m /S	I2C Serial Data line for I2C master controller. SDA is a tri-stateable output, which requires an external pull-up resistor.
H4	LAT_IN	I5	external data Latch
	LRDY	O5/T	Local bus Ready
	MISO	O5	SPI data MISO
J11	IO[0]	B5/8m	Digital /General Purpose I/O[7:0]
	LDA[0]	B5	Local bus Data bus [7:0]
	MSCLK	O5	SPI Master SCLK
J12	IO[1]	B5/8m	Digital /General Purpose I/O[7:0]
	LDA[1]	B5	Local bus Data bus [7:0]
	MMOSI	O5	SPI Master MOSI
G5	IO[2]	B5/8m	Digital /General Purpose I/O[7:0]
	LDA[2]	B5	Local bus Data bus [7:0]
	MMISO	I5	SPI Master MISO
E11	IO[4]	B5/8m	Digital /General Purpose I/O[7:0]
	LDA[4]	B5	Local bus Data bus [7:0]
	MSS[0]	O5	SPI Master Slave Select
K11	IO[16]	B5/8m	Digital /General Purpose I/O[23:16]
	LA[8]	I5	Local bus Address bus
	LINK	I5	LINK Provided by the PHY if a 100 Mbps (Full Duplex) link is established.
H11	IO[17]	B5/8m	Digital /General Purpose I/O[23:16]
	LA[9]	I5	Local bus Address bus
	PULAB	O5	Pulse AB, toggle when programmable point A and B
	MDIO	B5	PHY Management Interface data
H12	IO[18]	B5/8m	Digital /General Purpose I/O[23:16]
	LA[10]	I5	Local bus Address bus

Pin No	Pin Name	Type	Description
	PULC	O5	Pulse C, PWM period central point
	MDC	O5	PHY Management Interface clock
G12	IO[19]	B5/8m	Digital /General Purpose I/O[23:16]
	LA[11]	I5	Local bus Address bus
	PULZ	O5	Pulse Z, PWM period start point
	TXD[0] \ LINK_POL	O5	Transmit data [0] These pins are input direction during chip reset use to bootstrap the mode setting to decide external PHY's LINK polarity.
L11	IO[20]	B5/8m	Digital /General Purpose I/O[23:16]
	LA[12]	I5	Local bus Address bus
	PULB	O5	Pulse B, programmable point B
	TXD[1] TXD[2:1]\ TX_SH[1:0]	O5	Transmit data [2:1] This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the external PHY's TXD phase shift, please refer to Section 2.45.4.1.
E8	IO[21]	B5/8m	Digital /General Purpose I/O[23:16]
	LA[13]	I5	Local bus Address bus
	PULA	O5	Pulse A, programmable point A
	TXD[2] TXD[2:1]\ TX_SH[1:0]	O5	Transmit data [2:1] This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the external PHY's TXD phase shift, please refer to Section 2.45.4.1.
D8	IO[22]	B5/8m	Digital /General Purpose I/O[23:16]
	LBHE	I5	Local bus Byte High Enable (16-bit width only)
	PWM3H	O5/T	PWM 3 High pin
	TXD[3]	O5	Transmit data [3]
C8	IO[23]	B5/8m	Digital /General Purpose I/O[23:16]
	PWM3L	O5/T	PWM 3 Low pin
	TX_EN	O5	Transmit enable
C4	IO[24]	B5/8m	Digital/General Purpose I/O[31:24]
	LDA[8]	B5	Local bus Data bus [15:8]
	PWM2H	O5/T	PWM 2 High pin
	RXD[0]	I5	Receive data
F5	IO[25]	B5/8m	Digital/General Purpose I/O[31:24]
	LDA[9]	B5	Local bus Data bus [15:8]
	PWM2L	O5/T	PWM 2 Low pin
	RXD[1]	I5	Receive data
E5	IO[26]	B5/8m	Digital/General Purpose I/O[31:24]
	LDA[10]	B5	Local bus Data bus [15:8]
	PWM1H	O5/T	PWM 1 High pin or DIR pin
	RXD[2]	I5	Receive data
H5	IO[27]	B5/8m	Digital/General Purpose I/O[31:24]
	LDA[11]	B5	Local bus Data bus [15:8]
	PWM1L	O5/T	PWM 1 Low pin or STEP pin
	RXD[3]	I5	Receive data
J5	IO[28]	B5/8m	Digital/General Purpose I/O[31:24]
	LDA[12]	B5	Local bus Data bus [15:8]
	EMn	I5	Emergency input, active low

Pin No	Pin Name	Type	Description
	RX_ER	I5	Receive error
K5	IO[29]	B5/8m	Digital/General Purpose I/O[31:24]
	LDA[13]	B5	Local bus Data bus [15:8]
	ENCA	I5	ENC input A, Sin., CW, CLK, or HALL A
	RX_DV	I5	Receive data valid
L5	IO[30]	B5/8m	Digital/General Purpose I/O[31:24]
	LDA[14]	B5	Local bus Data bus [15:8]
	ENCB	I5	ENC input B, Cos., CCW, DIR, or HALL B
	RX_CLK	I5	Receive Clock
L4	IO[31]	B5/8m	Digital/General Purpose I/O[31:24]
	LDA[15]	B5	Local bus Data bus [15:8]
	ENCZ	I5	ENC input Z, Zero point or HALL C
	MCLK	O5	MII Clock 25 MHz clock source for Ethernet PHYs
P6	P1_TXON	A	PHY 1 differential Transmitted Negative signal
P7	P1_RXIN	A	PHY 1 differential Received Negative signal
P8	P1_SD	A	PHY 1 fiber mode Signal Detect Same P0_SD description
P9	P0_TXON	A	PHY 0 differential Transmitted Negative signal
P10	P0_RXIN	A	PHY 0 differential Received Negative signal
P11	P0_SD	A	PHY 0 fiber mode Signal Detect SD < 0.2V, Copper mode- 1.0V < SD < 1.8V, Fiber mode without detected signal. Generate far-end fault SD > 2.4V, Fiber mode with detected signal
P12	P0_XSCI	A	Crystal 25MHz Input
R12	P0_XSCO	A	Crystal 25MHz Output
R6	P1_TXOP	A	PHY 1 differential Transmitted Positive signal Same as PHY0 TXOP/ON description
R7	P1_RXIP	A	PHY 1 differential Received Positive signal Same as PHY0 RXIP/IN description
R9	P0_TXOP	A	PHY 0 differential Transmitted Positive signal In the copper mode, the differential data is transmitted to the media on the TXOP/TXON signal pair in the MDI mode. In the fiber mode, the signal pair should be connected to the TX+/TX- pin of the fiber transceiver.
R10	P0_RXIP	A	PHY 0 differential Received Positive signal In the copper mode, the differential data from the media is received on the RXIP/RXIN signal pair in the MDI mode. In the fiber mode, the signal pair should be connected to the RX+/RX- pin of the fiber transceiver.
L9	P0_RSET_BG	A	PHY off-chip Bias Resistor Connects an external resistor of 12 KΩ ± 1% to the PCB analog ground.

1.4.3 Power/Ground Pin Description

Pin No	Pin Name	Type	Description
C6, D6, E6, F6, G6, H6, J6, J10, K6, K7, K10	VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
K15	VSSSMPS	S	
J15	VLXSMPS	S	
H15	VDDSMPS	S	
H14	VFBSMPS	S	
C1, N1, R14	VCAP	S	
A1, R1, R15	VDDLDO	S	
A15	VSSA	S	
A14	VREF+	S	
B14	VREF-	S	
B15	VDDA	S	
K14	VBAT	S	
J1	VDD50USB	S	
H1	VDD33USB	S	
B1, C9, D9, E9, F8, F9, F11, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J14, K8, K9, N6, N7, N8, N9, N10, P1, P5, P15	GND (VSS)	P	Ground for all Analog and Digital Power.
C10, D10, E10, F10	VCCK	P	Digital Power for core, 1.2V Please add a 0.1uF bypass capacitor between each VCCK and GND.
D15	VCC12A_PLL	P	Analog Power for PLL, 1.2V. Please add a 0.1uF bypass capacitor between VCC12A_PLL and GND.
C7, D7, E7, F7	VCC3IO	P	Digital Power for I/O pins, 3.3V Please add a 0.1uF bypass capacitor between each VCC3IO and GND.
R5, R8, R11	VCC33A	P	Analog Power for Ethernet PHY, 3.3V Please add a 0.1uF bypass capacitor between VCC33A and GND.

2 Function Description

2.1 Dual STM32 Arm® Cortex® cores

The industrial AX58400 device embed two STM32 Arm® cores, a Cortex®-M7 and a Cortex®- M4. The Cortex®-M4 offers optimal performance for real-time applications while the Cortex®-M7 core can execute high-performance tasks in parallel.

The two cores belong to separate power domains. This allows designing gradual high- power efficiency solutions in combination with the low-power modes already available on this AX58400 device.

2.1.1 Arm® Cortex®-M7 with FPU

The Arm® Cortex®-M7 with double-precision FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and optimized power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard architecture with L1 caches (16 Kbytes of I-cache and 16 Kbytes of D-cache)
- 64-bit AXI interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The following memory interfaces are supported:

- Separate Instruction and Data buses (Harvard Architecture) to optimize CPU latency
- Tightly Coupled Memory (TCM) interface designed for fast and deterministic SRAM accesses
- AXI Bus interface to optimize Burst transfers
- Dedicated low-latency AHB-Lite peripheral bus (AHBP) to connect to peripherals.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It also supports single and double precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

Figure 1.2-1 shows the general block diagram of the AX58400 device.

Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

2.1.2 Arm® Cortex®-M4 with FPU

The Arm® Cortex®-M4 processor is a high-performance embedded processor which supports DSP instructions. It was developed to provide an optimized power consumption MCU, while delivering outstanding computational performance and low interrupt latency.

The Arm® Cortex®-M4 processor is a highly efficient MCU featuring:

- 3-stage pipeline with branch prediction
- Harvard architecture
- 32-bit System (S-BUS) interface
- 32-bit I-BUS interface
- 32-bit D-BUS interface

The Arm® Cortex®-M4 processor also features a dedicated hardware adaptive real-time accelerator (ST ART Accelerator™). This is an instruction cache memory composed of sixty- four 256-bit lines, a 256-bit cache buffer connected to the 64-bit AXI interface and a 32-bit interface for non-cacheable accesses.

2.2 Memory protection unit (MPU)

The devices feature two memory protection units. Each MPU manages the CPU access rights and the attributes of the system resources. It has to be programmed and enabled before use. Its main purposes are to prevent an untrusted user program to accidentally corrupt data used by the OS and/or by a privileged task, but also to protect data processes or read-protect memory regions.

The MPU defines access rules for privileged accesses and user program accesses. It allows defining up to 16 protected regions that can in turn be divided into up to 8 independent subregions, where region address, size, and attributes can be configured. The protection area ranges from 32 bytes to 4 Gbytes of addressable memory.

When an unauthorized access is performed, a memory management exception is generated.

2.3 Memories

2.3.1 Embedded Flash memory

The AX58400 device embeds 2 Mbytes of Flash memory that can be used for storing programs and data.

The Flash memory is organized as 266-bit Flash words memory that can be used for storing both code and data constants. Each word consists of:

- One Flash word (8 words, 32 bytes or 256 bits)
- 10 ECC bits.

The Flash memory is divided into two independent banks. Each bank is organized as follows:

- 1 Mbyte of user Flash memory block containing eight user sectors of 128 Kbytes (4 K Flash memory words)
- 128 Kbytes of System Flash memory from which the device can boot
- 2 Kbytes (64 Flash words) of user option bytes for user configuration

2.3.2 Secure access mode

In addition to other typical memory protection mechanism (RDP, PCROP), AX58400 device introduces the Secure access mode, a new enhanced security feature. This mode allows developing user-defined secure services by ensuring, on the one hand code and data protection and on the other hand code safe execution.

Two types of secure services are available:

- Root Secure Services:

  These services are embedded in System memory. They provide a secure solution for firmware and third-party modules installation. These services rely on cryptographic algorithms based on a device unique private key.

- User-defined secure services:

  These services are embedded in user Flash memory. Examples of user secure services are proprietary user firmware update solution, secure Flash integrity check or any other sensitive applications that require a high level of protection.

  The secure firmware is embedded in specific user Flash memory areas configured through option bytes.

Secure services are executed just after a reset and preempt all other applications to guarantee protected and safe execution. Once executed, the corresponding code and data are no more accessible.

The above secure services are available only for Cortex®-M7 core operating in Secure access mode. The other masters cannot access the option bytes involved in Secure access mode settings or the Flash secured areas.

2.3.3 Embedded SRAM

All devices feature around 1 Mbyte of RAM with hardware ECC. The RAM is divided as follows:

- 512 Kbytes of AXI-SRAM mapped onto AXI bus on D1 domain.
- SRAM1 mapped on D2 domain: 128 Kbytes
- SRAM2 mapped on D2 domain: 128 Kbytes
- SRAM3 mapped on D2 domain: 32 Kbytes
- SRAM4 mapped on D3 domain: 64 Kbytes
- 4 Kbytes of backup SRAM

  The content of this area is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

- RAM mapped to TCM interface (ITCM and DTCM):

  Both ITCM and DTCM RAMs are 0 wait state memories. They can be accessed either from the Arm® Cortex®-M7 CPU or the MDMA (even in Sleep mode) through a specific AHB slave of the Cortex®-M7(AHBS):

  – 64 Kbytes of ITCM-RAM (instruction RAM)

    This RAM is connected to ITCM 64-bit interface designed for execution of critical real-times routines by the Cortex®-M7.

  – 128 Kbytes of DTCM-RAM (2x 64-Kbyte DTCM-RAMs on 2x32-bit DTCM ports)

    The DTCM-RAM could be used for critical real-time data, such as interrupt service routines or stack/heap memory. Both DTCM-RAMs can be used in parallel (for load/store operations) thanks to the Cortex®-M7 dual issue capability.

    The MDMA can be used to load code or data in ITCM or DTCM RAMs.

Error code correction (ECC)

Over the product lifetime, and/or due to external events such as radiations, invalid bits in memories may occur. They can be detected and corrected by ECC. This is an expected behavior that has to be managed at final-application software level in order to ensure data integrity through ECC algorithms implementation.

SRAM data are protected by ECC:

- 7 ECC bits are added per 32-bit word.
- 8 ECC bits are added per 64-bit word for AXI-SRAM and ITCM-RAM.

The ECC mechanism is based on the SECDED algorithm. It supports single-error correction and double-error detection.

2.3.4 ST ART™ accelerator

The ART™ (adaptive real-time) accelerator block speeds up instruction fetch accesses of the Cortex®-M4 core from D1-domain internal memories (Flash memory bank 1, Flash memory bank 2, AXI SRAM) and from D1-domain external memories attached via Quad-SPI controller and Flexible memory controller (FMC).

The ART™ accelerator is a 256-bit cache line using 64-bit WRAP4 accesses from the 64-bit AXI D1 domain. The acceleration is achieved by loading selected code into an embedded cache and making it instantly available to Cortex®-M4 core, thus avoiding latency due to memory wait states.

Figure 2.3-1shows the block schematic and the environment of the ART accelerator.

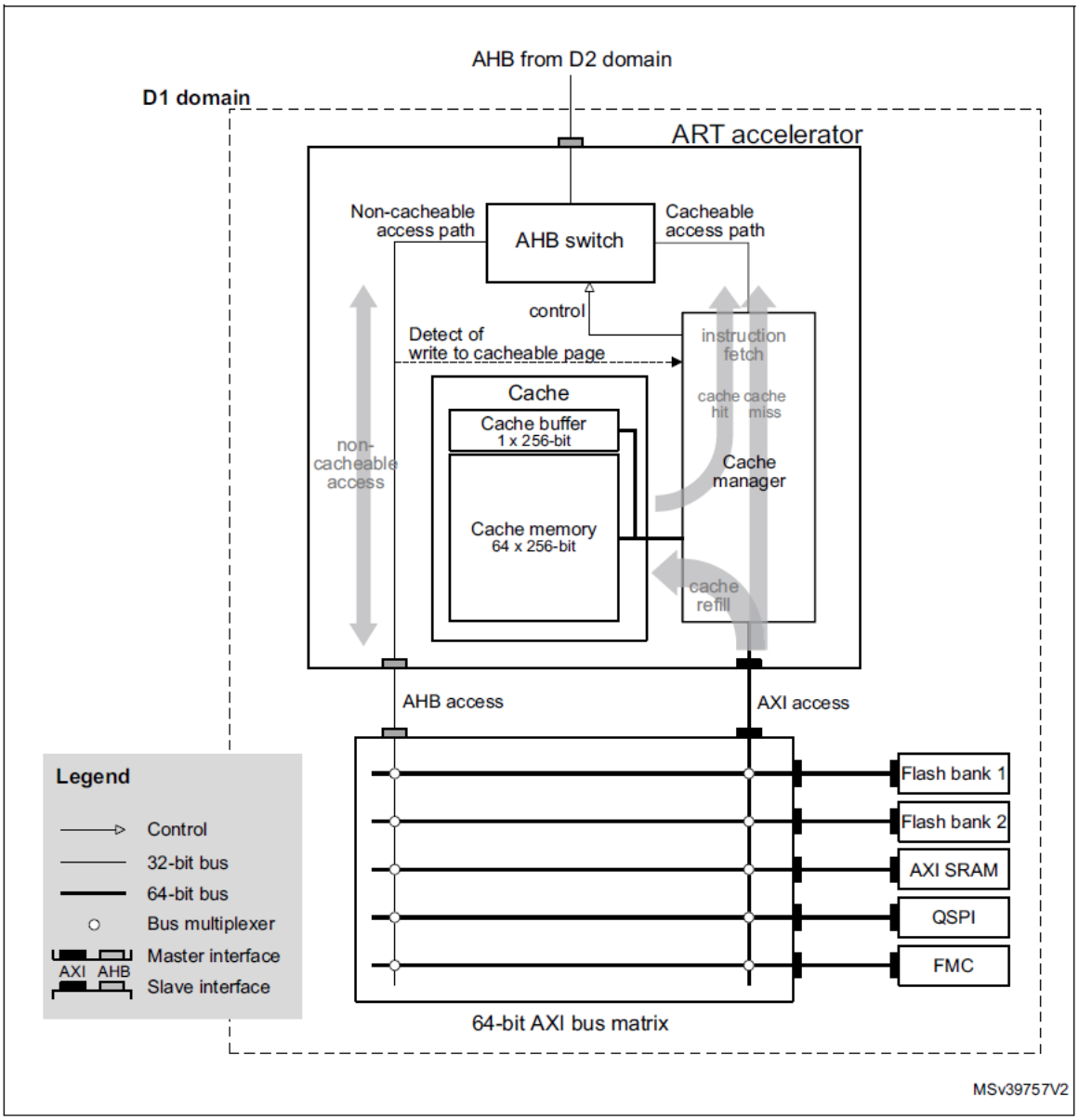


Figure 2.3-1: ST ART™ accelerator schematic and environment

2.4 Boot modes

By default, the boot codes are executed simultaneously by both cores. However, by programming the appropriate Flash user option byte, it is possible to boot from one core while clock-gating the other core.

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space
- Flash memory and SRAMs (except for ITCM /DTCM RAMs which cannot be accessed by the Cortex®-M4 core)

The bootloader is located in non-user System memory. It is used to reprogram the Flash memory through a serial interface (USART, I2C, SPI, USB-DFU).

2.5 Power supply management

2.5.1 Power supply scheme

AX58400 power supply voltages are the following:

- V_{DD} = 1.62 to 3.6 V: external power supply for I/Os, provided externally through VDD pins.
- V_{DDLDO} = 1.62 to 3.6 V: supply voltage for the internal regulator supplying VCORE
- V_{DDA} = 1.62 to 3.6 V: external analog power supplies for ADC, DAC, COMP and OPAMP.
- $V_{DD33USB}$ and $V_{DD50USB}$:
- $V_{DD50USB}$ can be supplied through the USB cable to generate the $V_{DD33USB}$ via the USB internal regulator. This allows supporting a V_{DD} supply different from 3.3 V.

  The USB regulator can be bypassed to supply directly $V_{DD33USB}$ if V_{DD} = 3.3 V.
- V_{BAT} = 1.2 to 3.6 V: power supply for the V_{SW} domain when V_{DD} is not present.
- V_{CAP}: V_{CORE} supply voltage, which values depend on voltage scaling (1.0 V, 1.1 V, 1.2 V or 1.35 V). They are configured through VOS bits in PWR_D3CR register and ODEN bit in the SYSCFG_PWRCR register. The V_{CORE} domain is split into the following power domains that can be independently switch off.
  - D1 domain containing some peripherals and the Cortex®-M7 core.
  - D2 domain containing a large part of the peripherals and the Cortex®-M4 core.
  - D3 domain containing some peripherals and the system control.
- V_{DDSMPS}= 1.62 V to 3.6 V: SMPS step-down converter power supply

  V_{DDSMPS} must be kept at the same voltage level as V_{DD}.
- V_{LXSMPS} = SMPS step-down converter output coupled to an inductor.
- V_{FBSMPS} = V_{CORE}, 1.8 V or 2.5 V external SMPS step-down converter feedback voltage sense input.

During power-up and power-down phases, the following power sequence requirements must be respected (see Figure 2.5-1):

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, $V_{DD33USB}$, $V_{DD50USB}$) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent (except for V_{DDSMPS}, which must remain at the same level as V_{DD}).

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the microcontroller remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

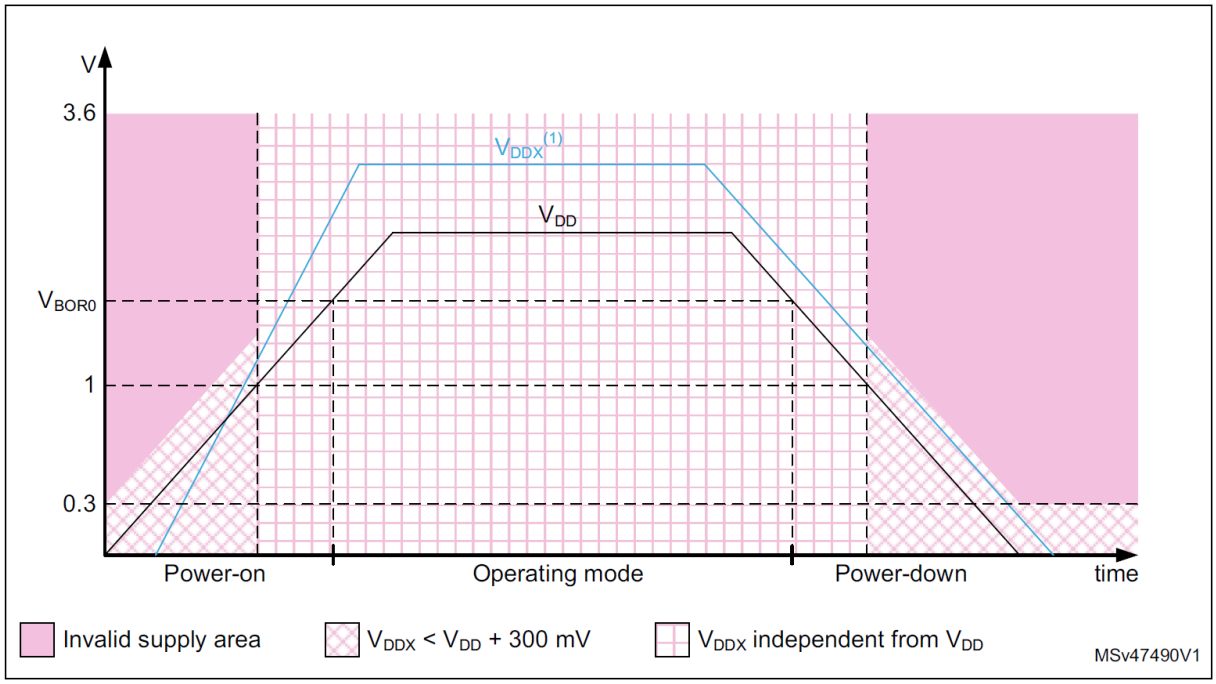


Figure 2.5-1: Power-up/power-down sequence

1. V_{DDx} refers to any power supply among V_{DDA}, $V_{DD33USB}$, $V_{DD50USB}$.
2. V_{DD} and V_{DDSMPS} must be wired together into order to follow the same voltage sequence.

2.5.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry:

- Power-on reset (POR)

  The POR supervisor monitors V_{DD} power supply and compares it to a fixed threshold. The devices remain in Reset mode when V_{DD} is below this threshold,

- Power-down reset (PDR)

  The PDR supervisor monitors V_{DD} power supply. A reset is generated when V_{DD} drops below a fixed threshold.

  The PDR supervisor can be enabled/disabled through PDR_ON pin.

- Brownout reset (BOR)

  The BOR supervisor monitors V_{DD} power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when V_{DD} drops below this threshold.

2.5.3 Voltage regulator (SMPS step-down converter and LDO)

The same voltage regulator supplies the 3 power domains (D1, D2 and D3). D1 and D2 can be independently switched off.

Voltage regulator output can be adjusted according to application needs through 6 power supply levels:

- Run mode (VOS0 to VOS3)
  - Scale 0: boosted performance (available only with LDO regulator)
  - Scale 1: high performance
  - Scale 2: medium performance and consumption
  - Scale 3: optimized performance and low-power consumption

Note: For AX58400 sales types (industrial temperature range) the voltage regulator output can be set only to VOS2 or VOS3 in Run mode (VOS0 and VOS1 are not available for industrial temperature range).

- Stop mode (SVOS3 to SVOS5)
  - Scale 3: peripheral with wakeup from Stop mode capabilities (UART, SPI, I2C, LPTIM) are operational
  - Scale 4 and 5 where the peripheral with wakeup from Stop mode is disabled

    The peripheral functionality is disabled but wakeup from Stop mode is possible through GPIO or asynchronous interrupt.

2.5.4 SMPS step-down converter

The built-in SMPS step-down converter is a highly power-efficient DC/DC non-linear switching regulator that provides lower power consumption than a conventional voltage regulator (LDO).

The SMPS step-down converter can be used for the following purposes:

- Direct supply of the V_{CORE} domain
  - the SMPS step-down converter operating modes follow the device system operating modes (Run, Stop, Standby).
  - the SMPS step-down converter output voltage are set according to the selected VOS and SVOS bits (voltage scaling)
- Delivery of an intermediate voltage level to supply the internal voltage regulator (LDO)
  - SMPS step-down converter operating modes

    When the SDEXTHP bit is equal to 0 in the PWR_CR3 register, the SMPS step- down converter follows the device system operating modes (Run, Stop and Standby).

    When the SDEXTHP bit is equal to 1 in PWR_CR3, the SMPS step-down converter is forced to High-performance mode and does not follow the device system operating modes (Run, Stop and Standby).
  - The SMPS step-down converter output equals 1.8 V or 2.5 V according to the selected SD level
- Delivery of an external supply
  - The SMPS step-down converter is forced to High-performance mode (provided SDEXTHP bit is equal to 1 in PWR_CR3)
  - The SMPS step-down converter output equals 1.8 V or 2.5 V according to the selected SD level

2.6 Low-power strategy

There are several ways to reduce power consumption on AX58400:

- Select the SMPS step-down converter as V_{CORE} supply voltage source, as it allows to enhance power efficiency.
- Select the adequate voltage scaling
- Decrease the dynamic power consumption by slowing down the system clocks even in Run mode, and by individually clock gating the peripherals that are not used.
- Save power consumption when one or both CPUs are idle, by selecting among the available low-power mode according to the user application needs. This allows achieving the best compromise between short startup time, low-power consumption, as well as available wakeup sources.

The devices feature several low-power modes:

- CSleep (CPU clock stopped)
- CStop (CPU sub-system clock stopped)
- DStop (Domain bus matrix clock stopped)
- Stop (System clock stopped)
- DStandby (Domain powered down)
- Standby (System powered down)

CSleep and CStop low-power modes are entered by the MCU when executing the WFI (Wait for Interrupt) or WFE (Wait for Event) instructions, or when the SLEEPONEXIT bit of the Cortex®-Mx core is set after returning from an interrupt service routine.

A domain can enter low-power mode (DStop or DStandby) when the processor, its subsystem and the peripherals allocated in the domain enter low-power mode. For instance, D1 or D2 domain enters DStop/DStandby mode when the CPU of the domain is in CStop mode AND the other CPU has no peripheral allocated in that domain, or if it is in CStop mode too. D3 domain can enter DStop/DStandby mode if both core subsystems do not have active peripherals in D3 domain, and D3 is not forced in Run mode.

If part of the domain is not in low-power mode, the domain remains in the current mode.

Finally the system can enter Stop or Standby when all EXTI wakeup sources are cleared and the power domains are in DStop or DStandby mode.

The clock system can be re-initialize by a master CPU (either the Cortex®-M4 or -M7) after exiting Stop mode while the slave CPU is held in low-power mode. Once the master CPU has re-initialized the system, the slave CPU can receive a wakeup interrupt and proceed with the interrupt service routine.

System power mode	D1 domain power mode	D2 domain power mode	D3 domain power mode
Run	DRun/DStop/DStandby	DRun/DStop/DStandby	DRun
Stop	DStop/DStandby	DStop/DStandby	DStop
Standby	DStandby	DStandby	DStandby

Table 2.6-1: System vs domain low-power mode

2.7 Reset and clock controller (RCC)

The clock and reset controller is located in D3 domain. The RCC manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides a high flexibility in the choice of clock sources and allows to apply clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the baudrate.

2.7.1 Clock management

The devices embed four internal oscillators, two oscillators with external crystal or resonator, two internal oscillators with fast startup time and three PLLs.

The RCC receives the following clock source inputs:

- Internal oscillators:
  - 64 MHz HSI clock
  - 48 MHz RC oscillator
  - 4 MHz CSI clock
  - 32 KHz LSI clock
- External oscillators:
  - HSE clock: 4-50 MHz (generated from an external source) or 4-48 MHz (generated from a crystal/ ceramic resonator)
  - LSE clock: 32.768 KHz

The RCC provides three PLLs: one for system clock, two for kernel clocks.

The system starts on the HSI clock. The user application can then select the clock configuration.

2.7.2 System reset sources

Power-on reset initializes all registers while system reset reinitializes the system except for the debug, part of the RCC and power controller status registers, as well as the backup power domain.

A system reset is generated in the following cases:

- Power-on reset (pwr_por_rst)
- Brownout reset
- Low level on NRST pin (external reset)
- Independent watchdog 1 (from D1 domain)
- Independent watchdog 2 (from D2 domain)
- Window watchdog 1 (from D1 domain)
- Window watchdog 2 (from D2 domain)
- Software reset
- Low-power mode security reset
- Exit from Standby

2.8 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

After reset, all GPIOs (except debug pins) are in Analog mode to reduce power consumption (refer to GPIOs register reset values in the device reference manual).

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.9 Bus-interconnect matrix

The devices feature an AXI bus matrix, two AHB bus matrices and bus bridges that allow interconnecting bus masters with bus slaves (see Figure 2.9-1).

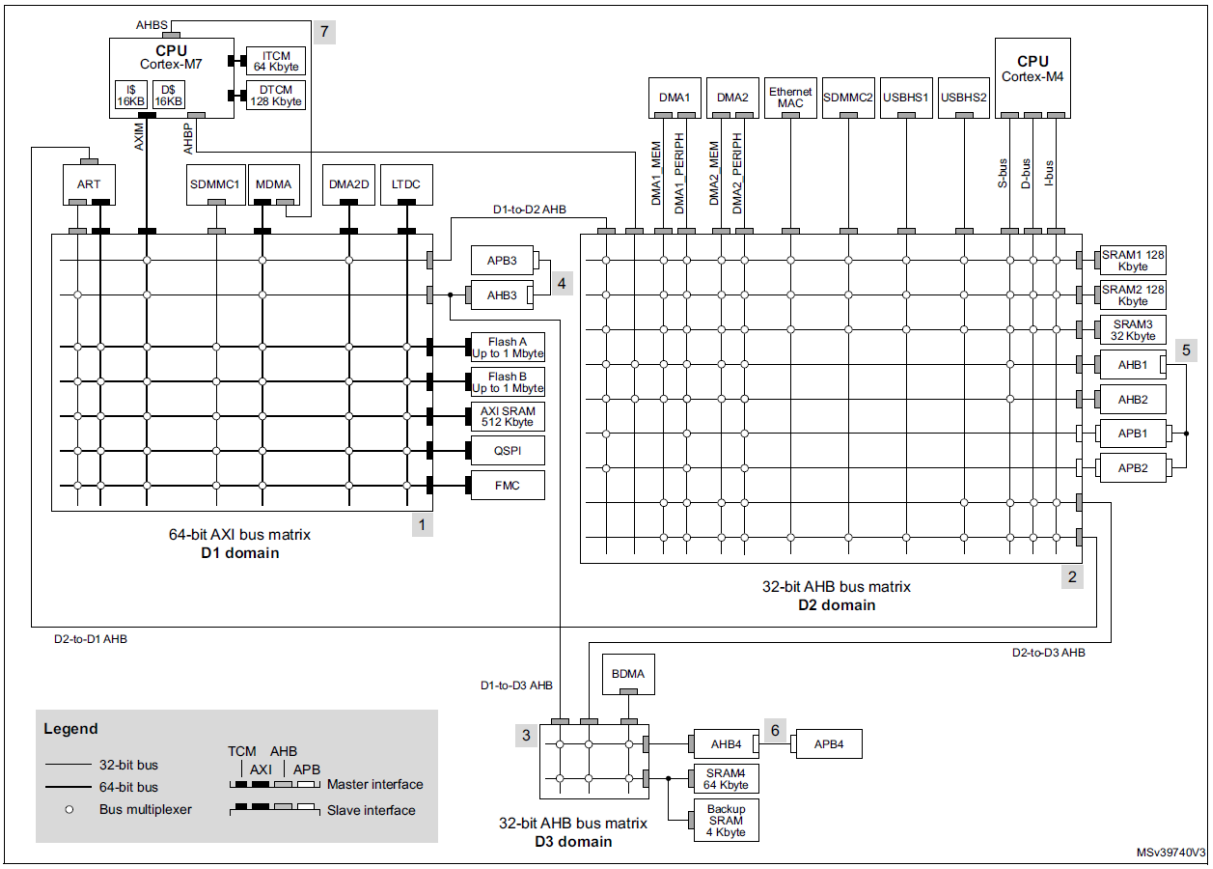


Figure 2.9-1: AX58400 Bus matrix

2.10 DMA controllers

The devices feature four DMA instances to unload CPU activity:

- A master direct memory access (MDMA)

  The MDMA is a high-speed DMA controller, which is in charge of all types of memory transfers (peripheral to memory, memory to memory, memory to peripheral), without any CPU action. It features a master AXI interface and a dedicated AHB interface to access Cortex®-M7 TCM memories.

  The MDMA is located in D1 domain. It is able to interface with the other DMA controllers located in D2 domain to extend the standard DMA capabilities, or can manage peripheral DMA requests directly.

  Each of the 16 channels can perform single block transfers, repeated block transfers and linked list transfers.

- Two dual-port DMAs (DMA1, DMA2) located in D2 domain, with FIFO and request router capabilities.
- One basic DMA (BDMA) located in D3 domain, with request router capabilities.

The DMA request router could be considered as an extension of the DMA controller. It routes the DMA peripheral requests to the DMA controller itself. This allowing managing the DMA requests with a high flexibility, maximizing the number of DMA requests that run concurrently, as well as generating DMA requests from peripheral output trigger or DMA event.

2.11 ST Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphical accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables. The DMA2D also supports block based YCbCr to handle JPEG decoder output.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

2.12 Nested vectored interrupt controller (NVIC)

Both Cortex®-M7 (CPU1) and Cortex®-M4 (CPU2) cores have their own nested vector interrupt controller (respectively NVIC1 and NVIC2). Each NVIC instance is able to manage 16 priority levels, and handle up to 150 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor context automatically saved on interrupt entry, and restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

2.13 Extended interrupt and event controller (EXTI)

The EXTI controller performs interrupt and event management. In addition, it can wake up the processors, power domains and/or D3 domain from Stop mode.

The EXTI handles up to 89 independent event/interrupt lines split as 28 configurable events and 61 direct events (including two interrupt lines for inter-core management).

Configurable events have dedicated pending flags, active edge selection, and software trigger capable.

Direct events provide interrupts or events from peripherals having a status flag.

2.14 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link- time and stored at a given memory location.

2.15 Flexible memory controller (FMC)

The FMC controller main features are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is the FMC kernel clock divided by 2.

2.16 Quad-SPI memory interface (QUADSPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting Single, Dual or Quad-SPI Flash memories. It supports both single and double datarate operations.

It can operate in any of the following modes:

- Direct mode through registers
- External Flash status register polling mode
- Memory mapped mode.

Up to 256 Mbytes of external Flash memory can be mapped, and 8-, 16- and 32-bit data accesses are supported as well as code execution.

The opcode and the frame format are fully programmable.

2.17 Analog-to-digital converters (ADCs)

The AX58400 device embeds three analog-to-digital converters, which resolution can be configured to 16, 14, 12, 10 or 8 bits.

Each ADC shares up to 20 external channels, performing conversions in the Single-shot or Scan mode. In Scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller, thus allowing to automatically transfer ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM6, TIM8, TIM15, HRTIM1 and LPTIM1 timer.

2.18 Temperature sensor

AX58400 device embeds a temperature sensor that generates a voltage (VTS) that varies linearly with the temperature. This temperature sensor is internally connected to ADC3_IN18. The conversion range is between 1.7 V and 3.6 V. It can measure the device junction temperature ranging from − 40 up to +140 °C.

The temperature sensor has a good linearity, but it has to be calibrated to obtain a good overall accuracy of the temperature measurement. As the temperature sensor offset varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only. To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated. The temperature sensor factory calibration data are stored in the System memory area, which is accessible in Read-only mode.

2.19 V_{BAT} operation

The V_{BAT} power domain contains the RTC, the backup registers and the backup SRAM.

To optimize battery duration, this power domain is supplied by V_{DD} when available or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} dropped below the PDR level.

The voltage on the VBAT pin could be provided by an external battery, a supercapacitor or directly by V_{DD}, in which case, the V_{BAT} mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is connected to V_{SS} (Internal Reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

2.20 Digital-to-analog converters (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- external triggers for conversion
- input voltage reference VREF+ or internal VREFBUF reference.

The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.21 Ultra-low-power comparators (COMP)

AX58400 device embeds two rail-to-rail comparators (COMP1 and COMP2). They feature programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) as well as selectable output polarity.

The reference voltage can be one of the following:

- An external I/O
- A DAC output channel
- An internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers, and be combined into a window comparator.

2.22 Operational amplifiers (OPAMP)

AX58400 device embeds two rail-to-rail operational amplifiers (OPAMP1 and OPAMP2) with external or internal follower routing and PGA capability.

The operational amplifier main features are:

- PGA with a non-inverting gain ranging of 2, 4, 8 or 16 or inverting gain ranging of -1, -3, -7 or -15
- One positive input connected to DAC
- Output connected to internal ADC
- Low input bias current down to 1 nA

- Low input offset voltage down to 1.5 mV
- Gain bandwidth up to 7.3 MHz

The devices embed two operational amplifiers (OPAMP1 and OPAMP2) with two inputs and one output each. These three I/Os can be connected to the external pins, thus enabling any type of external interconnections. The operational amplifiers can be configured internally as a follower, as an amplifier with a non-inverting gain ranging from 2 to 16 or with inverting gain ranging from -1 to -15.

2.23 Digital filter for sigma-delta modulators (DFSDM)

The devices embed one DFSDM with 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 8 internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. DFSDM features optional parallel data stream inputs from internal ADC peripherals or microcontroller memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - configurable SPI interface to connect various SD modulator(s)
  - configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for SD modulator(s): 0..20 MHz
- alternative inputs from 8 internal digital parallel channels (up to 16 bit input resolution):
  - internal sources: ADC data or memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - integrator: oversampling ratio (1..256)
- up to 24-bit output data resolution, signed output data format
- automatic data offset correction (offset stored in register by user)
- continuous or single conversion
- start-of-conversion triggered by:
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM0)
- analog watchdog feature:

  - low value and high value data threshold registers
  - dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - input from final output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion
- short circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
  - monitoring continuously each input serial channel
- break signal generation on analog watchdog event or on short circuit detector event
- extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- "regular" or "injected" conversions:
  - "regular" conversions can be requested at any time or even in Continuous mode without having any impact on the ti ming of "injected" conversions
  - "injected" conversions for precise timing and with high conversion priority

DFSDM features	DFSDM1
Number of filters	4
Number of input transceivers/channels	8
Internal ADC parallel input	X
Number of external triggers	16
Regular channel information in identification register	X

Table 2.23-1: DFSDM implementation

2.24 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can achieve a data transfer rate up to 105 Mbyte/s using a 60 MHz pixel clock. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports Continuous mode or Snapshot (a single frame) mode
- Capability to automatically crop the image

2.25 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x64-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface with burst of 16 words

2.26 JPEG Codec (JPEG)

The JPEG Codec can encode and decode a JPEG stream as defined in the ISO/IEC 10918- 1 specification. It provides an fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features are as follows:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Support for single greyscale component
- Ability to enable/disable header processing
- Fully synchronous design
- Configuration for High-speed decode mode

2.27 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

2.28 Cryptographic acceleration (CRYP and HASH)

The devices embed a cryptographic processor that supports the advanced cryptographic algorithms usually required to ensure confidentiality, authentication, data integrity and non- repudiation when exchanging messages with a peer:

- Encryption/Decryption
  - DES/TDES (data encryption standard/triple data encryption standard): ECB (electronic codebook) and CBC (cipher block chaining) chaining algorithms, 64-, 128- or 192-bit key
  - AES (advanced encryption standard): ECB, CBC, GCM, CCM, and CTR (Counter mode) chaining algorithms, 128, 192 or 256-bit key
- Universal HASH
  - SHA-1 and SHA-2 (secure HASH algorithms)
  - MD5
  - HMAC

The cryptographic accelerator supports DMA request generation.

2.29 Timers and watchdogs

The devices include one high-resolution timer, two advanced-control timers, ten general- purpose timers, two basic timers, five low-power timers, two watchdogs and a SysTick timer.

All timer counters can be frozen in Debug mode.

Table 2.29-1 compares the features of the advanced-control, general-purpose and basic timers.

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz) (1)(2)
High-resolution timer	HRTIM1	16-bit	Up	/1 /2 /4 (x2 x4 x8 x16 x32, with DLL)	Yes	10	Yes	480(2)	480
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between1 and 65536	Yes	4	Yes	120	240

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz) (1)(2)
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	120	240
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	120	240
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	120	240
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	120	240
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1	120	240
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1	120	240
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	120	240
Low-power timer	LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	No	0	No	120	240

Table 2.29-1: Timer feature comparison

1. The maximum timer clock is up to 480 MHz depending on TIMPRE bit in the RCC_CFGR register and D2PRE1/2 bits in RCC_D2CFGR register.
2. On AX58400 sales types (extended industrial temperature range), the maximum clock frequency is 300 MHz for the high-resolution timer and 150 MHz for the other timers.

2.29.1 High-resolution timer (HRTIM1)

The high-resolution timer (HRTIM1) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of 6 timers, 1 master and 5 slaves, totaling 10 high-resolution outputs, which can be coupled by pairs for deadtime insertion. It also features 5 fault inputs for protection purposes and 10 inputs to handle external events such as current limitation, zero voltage or zero current switching.

The HRTIM1 timer is made of a digital kernel clocked at 480 MHz(a) The high-resolution is available on the 10 outputs in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multi-switch complex converters or operate independently to manage multiple independent converters.

The waveforms are defined by a combination of user-defined timings and external events such as analog or digital feedbacks signals.

HRTIM1 timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, Burst mode controller, Push-pull and Resonant mode.

It supports many topologies including LLC, Full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

a. Up to 300 MHz for AX58400 sales types (extended industrial temperature range).

2.29.2 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (Edge- or Center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0- 100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

2.29.3 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the AX58400 device (see Table 2.29-1 for differences).

- TIM2, TIM3, TIM4, TIM5

  The devices include 4 full-featured general-purpose timers: TIM2, TIM3, TIM4 and TIM5. TIM2 and TIM5 are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. All timers feature 4 independent channels for input capture/output compare, PWM or One-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  TIM2, TIM3, TIM4 and TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- TIM12, TIM13, TIM14, TIM15, TIM16, TIM17

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM or One-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers or used as simple timebases.

2.29.4 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

2.29.5 Low-power timers (LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5)

The low-power timers have an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit auto-reload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / One-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

2.29.6 Independent watchdogs

There are two independent watchdogs, one per domain. Each independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

2.29.7 Window watchdogs

There are two window watchdogs, one per domain. Each window watchdog is based on a 7- bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device or each respective domain (configurable in the RCC register), when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in Debug mode.

2.29.8 SysTick timer

The devices feature two SysTick timers, one per CPU. These timers are dedicated to real- time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

2.30 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- A 32.768 KHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 KHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

All RTC events (Alarm, Wakeup Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

2.31 Inter-integrated circuit interface (I2C)

AX58400 device embeds four I^2C interfaces.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I^2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and Master modes, multi-master capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBusTM) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

2.32 Universal synchronous/asynchronous receiver transmitter (USART)

AX58400 device has four embedded universal synchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7 and UART8). Refer to Table 2.32-1for a summary of USARTx and UARTx features.

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire Half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 12.5 Mbit/s.

USART1, USART2, USART3 and USART6 also provide Smartcard mode (ISO 7816 compliant) and SPI-like communication capability.

The USARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

All USART have a clock domain independent from the CPU clock, allowing the USARTx to wake up the MCU from Stop mode. The wakeup from Stop mode is programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled. All USART interfaces can be served by the DMA controller.

USART modes/features[1]	USART1/2/3/6	UART4/5/7/8
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (Master/Slave)	X	-
Smartcard mode	X	-
Single-wire Half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain and wakeup from low power mode	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver Enable	X	X
USART data length	7, 8 and 9 bits	
Tx/Rx FIFO	X	X
Tx/Rx FIFO size	16	

1. X = supported.

Table 2.32-1: USART features

2.33 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART (LPUART1). The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode. The wakeup from Stop mode are programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

Only a 32.768 KHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

2.34 Serial peripheral interface (SPI)/inter-integrated sound interfaces (I2S)

The devices feature up to six SPIs (SPI2S1, SPI2S2, SPI2S3, SPI4, SPI5 and SPI6) that allow communicating up to 150 Mbits/s in Master and Slave modes, in Half-duplex, Full- duplex and Simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. All SPI interfaces support NSS pulse mode, TI mode, Hardware CRC calculation and 8x 8-bit embedded Rx and Tx FIFOs with DMA capability.

Three standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in Master or Slave mode, in Simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 KHz up to 192 KHz are supported. When either or both of the I^2S interfaces is/are configured in Master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All I^2S interfaces support 16x 8- bit embedded Rx and Tx FIFOs with DMA capability.

2.35 Serial audio interfaces (SAI)

The devices embed 4 SAIs (SAI1, SAI2, SAI3 and SAI4) that allow designing many stereo or mono audio protocols such as I2S, LSB or MSB-justified, PCM/DSP, TDM or AC'97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, the SAI contains two independent audio sub-blocks. Each block has it own clock generator and I/O line controller.

Audio sampling frequencies up to 192 KHz are supported.

In addition, up to 8 microphones can be supported thanks to an embedded PDM interface. The SAI can work in master or slave configuration. The audio sub-blocks can be either receiver or transmitter and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

2.36 SPDIFRX Receiver Interface (SPDIFRX)

The SPDIFRX peripheral is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main SPDIFRX features are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 KHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIFRX will re-sample the incoming signal, decode the Manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

2.37 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- Full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling SWPMI can be served by the DMA controller.

2.38 Management Data Input/Output (MDIO) slaves

The devices embed an MDIO slave interface it includes the following features:

- 32 MDIO Registers addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIO read-only output data registers
  - 32 x 16-bit firmware read-only, MDIO write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
  - MDIO Register write
  - MDIO Register read
  - MDIO protocol error
- Able to operate in and wake up from Stop mode

2.39 SD/SDIO/MMC card host interfaces (SDMMC)

Two SDMMC host interfaces are available. They support *MultiMediaCard System Specification Version 4.51* in three different databus modes: 1 bit (default), 4 bits and 8 bits.

Both interfaces support the *SD memory card specifications version 4.1.* and the *SDIO card specification version 4.0.* in two different databus modes: 1 bit (default) and 4 bits.

Each SDMMC host interface supports only one SD/SDIO/MMC card at any one time and a stack of MMC Version 4.51 or previous.

The SDMMC host interface embeds a dedicated DMA controller allowing high-speed transfers between the interface and the SRAM.

2.40 Controller area network (FDCAN1, FDCAN2)

The controller area network (CAN) subsystem consists of two CAN modules, a shared message RAM memory and a clock calibration unit.

Both CAN modules (FDCAN1 and FDCAN2) are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

FDCAN1 supports time triggered CAN (TT-FDCAN) specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10-Kbyte message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers (and triggers for TT-FDCAN). This message RAM is shared between the two FDCAN1 and FDCAN2 modules.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for both FDCAN1 and FDCAN2 from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

2.41 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed two USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. OTG-HS1 supports both full-speed and high-speed operations, while OTG-HS2 supports only full-speed operations. They both integrate the transceivers for full-speed operation (12 Mbit/s) and are able to operate from the internal HSI48 oscillator. OTG-HS1 features a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG-HS1 in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripherals are compliant with the USB 2.0 specification and with the OTG 2.0 specification. They have software-configurable endpoint setting and supports suspend/resume. The USB OTG controllers require a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The main features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 9 bidirectional endpoints (including EP0)
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode (OTG_HS1 only)

The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.

- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.42 Ethernet MAC interface with dedicated DMA controller (ETH)

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)

- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

2.43 High-definition multimedia interface (HDMI)-consumer electronics control (CEC)

The devices embed a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wakeup the MCU from Stop mode on data reception.

2.44 Debug infrastructure

The devices offer a comprehensive set of debug and trace features on both cores to support software development and system integration.

- Breakpoint debugging
- Code execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output
- Serial-wire trace port
- Trace port
- Arm® CoreSight™ debug and trace components

The debug can be controlled via a JTAG/Serial-wire debug access port, using industry standard debugging tools. The debug infrastructure allows debugging one core at a time, or both cores in parallel.

The trace port performs data capture for logging and analysis.

A 4-Kbyte embedded trace FIFO (ETF) allows recording data and sending them to any com port. In Trace mode, the trace is transferred by DMA to system RAM or to a high-speed interface (such as SPI or USB). It can even be monitored by a software running on one of the cores. Unlike hardware FIFO mode, this mode is invasive since it uses system resources which are shared by the processors.

2.45 ESC (EtherCAT) Sub-system

2.45.1 Overview

The AX58400 implements a 2/3-port EtherCAT slave controller (ESC), licensed from Beckhoff Automation, with 9 Kbytes Process Data RAM, 8 Fieldbus Memory Management Units (FMMUs), 8 Sync-Managers and a 64-bit Distributed Clock.

Port 0 and 1 integrate embedded Ethernet PHYs, and port 2 is an optional MII interface which are multi-function pins shared with other interfaces (i.e. PWM, Hall, etc.). Packets are forwarded in the following order: **Port 0->EtherCAT Processing Unit->Port 1->Port 2**.

The AX58400 supports function register mirror from/to ESC memory space. The mirror registers located at process data memory address from 0x3000 to 0x33FF.

For detailed information about the EtherCAT technology, the EtherCAT core mechanisms, and major features, we refer to the official standard documentations and guidelines available from ETG (www.ethercat.org, ETG.1000), IEC (http://www.iec.ch, IEC61158, IEC61784-2, IEC 61800-7), and Beckhoff (http://www.beckhoff.de, technical specification) web sites.

The AX58400 requires a crystal (25MHz, ±25 PPM at room temperature) as the clock source. Internal PLL generates the 100MHz clock for EtherCAT Slave Controller (ESC) and also for other functions.

The AX58400 has three reset sources. First, during the VCCK power-on, the internal Power-On-Reset (POR) can generate a reset pulse to reset all the function blocks when the VCCK power pin rises to a certain threshold voltage level. The second reset is RSTn pin, which is to do the fundamental reset. And third, EtherCAT command reset, the EtherCAT master can send reset sequence to force AX58400 reset. AX58400 also supports a reset output RSTO polarity bootstrap configuration (RSTO_POL).

2.45.2 Features

- 2/3-port EtherCAT Slave Controller (ESC) with 2 Integrated Fast Ethernet PHYs
- Standard EtherCAT Slave Controller (ESC)
  - 8 Fieldbus Memory Management Units (FMMUs)
  - 8 Sync Managers
  - 64-bit distributed clock
  - 9K bytes RAM
- Integrated Fast Ethernet PHYs
  - Compliant with IEEE 802.3/802.3u 100BASE-TX/100BASE-FX
  - PHY loopback mode
  - Supports twisted pair crossover detection and auto-correction (HP Auto-MDIX)
  - Automatic polarity detection and correction
- 3rd Ethernet MII Port for Flexible EtherCAT Network Configurations
- SPI Slave Interface for PDI and Function Access
- 3-channel PWM Controller for simple Motion Control
- Step & Direction Controller for simple Motion Control
- Incremental and Hall Encoder Interface for simple Motion Control
- Emergency Stop Input
- Configurable Watchdog for Outputs and Inputs Monitoring
- IRQ Event Output
- SPI Master Interface for ADC/DAC application
- Supports I2C Master Interface

2.45.3 Block Diagram

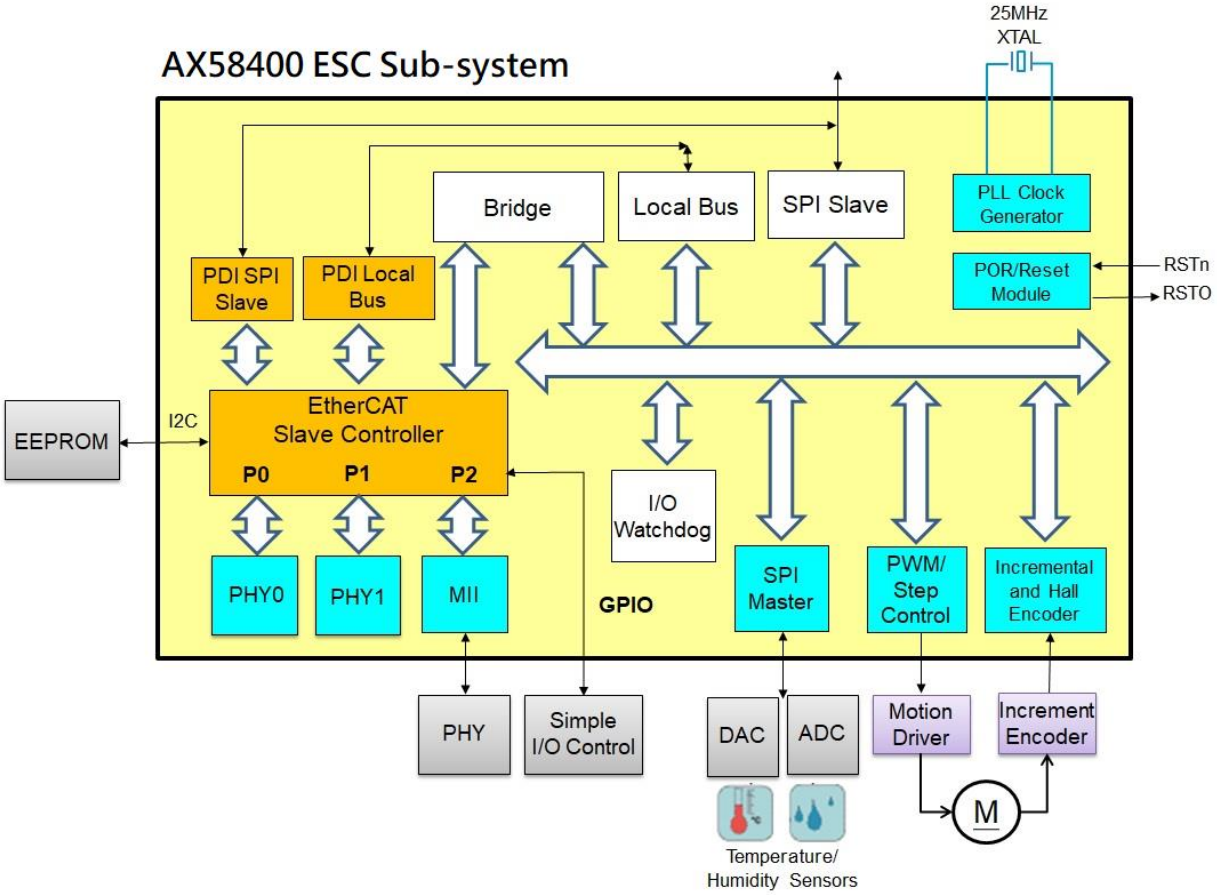


Figure 2.45-1: ESC Sub-system Block Diagram

2.45.4 ESC Configuration

2.45.4.1 Bootstrap Pins for Chip Configuration

The AX58400 supports five multi-function bootstrap pins (pin M1, M2, C11, L14 and M13) for five hardware configurations, i.e. external I^2C EEPROM size, ESC supported port number, RSTO polarity and integrated port 0/1 PHY media mode; and it also supports other three multi-function bootstrap pins (pin L11, E8, G12) for the configuration of port 2 MII signals. User needs to utilize an external resistor to pull up / down these bootstrap pins.

Pins	Signal Name	Description
M1	EEP_SIZE	I^2C EEPROM Size 0: 1 Kbit to 16Kbit 1: 32Kbit to 4Mbit
M2	3PORT_MODE	ESC port number 0: 2 ports mode 1: 3 ports mode
B13	RSTO_POL	RSTO Reset Output Polarity 0: Active Low 1: Active High
C11	PDI_EMU	Device emulation (0x0141.0) 0: Device status register is controlled by PDI 1: Device status register is identical to device control register
L14	P0_FIBER	Port 0 PHY media mode 0: Copper mode 1: Fiber mode
M13	P1_FIBER	Port 1 PHY Media mode 0: Copper mode 1: Fiber mode
L11	TX_SH [1]	Port 2 MII TXD Align position 2‘b00: Align with MCLK, 2’b01: Delay 1/4 phase with MCLK 2’b10: Delay 1/2 phase with MCLK 2’b11: Delay 3/4 phase with MCLK
E8	TX_SH [0]	
G12	LINK_POL	Port 2 MII LINK Polarity 0: Active Low 1: Active High

Table 2.45-1: ESC Bootstrap Pins Configuration

2.45.4.2 Hardware Configuration EEPROM (HWCFGEE)

The AX58400 I²C master controller supports the communication to external I²C devices and an I²C Hardware Configuration EEPROM Loader to support loading the EtherCAT Slave Information (ESI) from external I²C EEPROM during chip reset. The AX58400 supports I²C EEPROM with EEPROM size from 1 Kbit (128 bytes) to 4 Mbit (500Kbytes).

The AX58400 I²C Hardware Configuration EEPROM layout is shown in following table.

EEPROM Byte Offset	EEPROM Word Offset	Parameter	ESC Register Offset
ESC Configuration Area			
0x00	0x00	PDI Control	0x0140
0x01		ESC Configuration (bit 2 is also mapped to ESC register 0x0110.2)	0x0141
0x02	0x01	PDI Configuration	0x0150
0x03		Sync/Latch [1:0] Configuration	0x0151
0x05 - 0x04	0x02	Pulse Length of SyncSignals	0x0983 - 0x0982
0x07 - 0x06	0x03	Extended PDI Configuration	0x0153 - 0x0152
0x09 - 0x08	0x04	Configured Station Alias	0x0013 - 0x0012
0x0A	0x05	Host Interface Extend Setting and Drive Strength	
0x0B		Reserved, shall be zero	
0x0C	0x06	Reserved, shall be zero	
0x0D		Multi-Function Select and Drive Strength	
0x0F - 0x0E	0x07	Checksum	
0x13 - 0x10	0x09 – 0x08	Vendor ID	
0x17 - 0x14	0x0B – 0x0A	Product Code	
0x1B - 0x18	0x0D – 0x0C	Revision Number	
0x1F - 0x1C	0x0F – 0x0E	Serial Number	
0x27 - 0x20	0x13 – 0x10	Reserved	
Bootstrap Mailbox Config			
0x29 - 0x28	0x14	Bootstrap Receive Mailbox Offset	
0x2B - 0x2A	0x15	Bootstrap Receive Mailbox Size	
0x2D - 0x2C	0x16	Bootstrap Send Mailbox Offset	
0x2F - 0x2E	0x17	Bootstrap Send Mailbox Size	
Mailbox Sync Man Config			
0x31 - 0x30	0x18	Standard Receive Mailbox Offset	
0x33 - 0x32	0x19	Standard Receive Mailbox Size	
0x35 - 0x34	0x1A	Standard Send Mailbox Offset	
0x37 - 0x36	0x1B	Standard Send Mailbox Size	
0x39 - 0x38	0x1C	Mailbox Protocol	
0x3F - 0x3A	0x1F – 0x1D	Reserved	
0x7B - 0x40	0x3D – 0x20	Reserved	
0x7D - 0x7C	0x3E	Size	
0x7F - 0x7E	0x3F	Version	
ESC Category 1 (for AX58400 Bridge Access Configuration if used) *Note1			
0x81 ~ 0x80	0x40	Category 1 Type (Default: **0x0001**)	
0x83 ~ 0x82	0x41	Category 1 Data Size (words) (Default: **0x0021**)	
0x84	0x42	MCTLR Access Control	0x0580

EEPROM Byte Offset	EEPROM Word Offset	Parameter	ESC Register Offset
0x85		PXCFGR Access Control	0x0581
0x86	0x43	PTAPPR Access Control	0x0582
0x87		PTBPPR Access Control	0x0583
0x88	0x44	PPCR Access Control	0x0584
0x89		PBBMR Access Control	0x0585
0x8A	0x45	P1CTRLR Access Control	0x0586
0x8B		P1SHR Access Control	0x0587
0x8C	0x46	P1HPWR Access Control	0x0588
0x8D		P2CTRLR Access Control	0x0589
0x8E	0x47	P2SHR Access Control	0x058A
0x8F		P2HPWR Access Control	0x058B
0x90	0x48	P3CTRLR Access Control	0x058C
0x91		P3SHR Access Control	0x058D
0x92	0x49	P3HPWR Access Control	0x058E
0x93		SGTR Access Control	0x058F
0x94	0x4A	SHPWR Access Control	0x0590
0x95		TDLYR Access Control	0x0591
0x96	0x4B	STNR Access Control	0x0592
0x97		SCFGR Access Control	0x0593
0x98	0x4C	SCTRLR Access Control	0x0594
0x99		SCNTR Access Control	0x0595
0x9A	0x4D	ECNTVR Access Control	0x0596
0x9B		ECNSTR Access Control	0x0597
0x9C	0x4E	ELATR Access Control	0x0598
0x9D		EMODR Access Control	0x0599
0x9E	0x4F	ECLRR Access Control	0x059A
0x9F		HALSTR Access Control	0x059B
0xA0	0x50	WTR Access Control	0x059C
0xA1		WCFGR Access Control	0x059D
0xA2	0x51	WTPVCR Access Control	0x059E
0xA3		WMSPR Access Control	0x059F
0xA4	0x52	WMMR Access Control	0x05A0
0xA5		WOMR Access Control	0x05A1
0xA6	0x53	WOER Access Control	0x05A2
0xA7		WOPR Access Control	0x05A3
0xA8	0x54	WTPVR Access Control	0x05A4
0xA9		SPICFGR Access Control	0x05A5
0xAA	0x55	SPIBRR Access Control	0x05A6
0xAB		SPIDBSR Access Control	0x05A7
0xAC	0x56	SPIDTR Access Control	0x05A8
0xAD		SPIRPTR Access Control	0x05A9
0xAE	0x57	SPILTR Access Control	0x05AA
0xAF		SPIPRLR Access Control	0x05AB
0xB0	0x58	SPI01BCR Access Control	0x05AC
0xB1		SPI23BCR Access Control	0x05AD
0xB2	0x59	SPI45BCR Access Control	0x05AE
0xB3		SPI67BCR Access Control	0x05AF
0xB4	0x5A	SPI03SSR Access Control	0x05B0

EEPROM Byte Offset	EEPROM Word Offset	Parameter	ESC Register Offset
0xB5		SPI47SSR Access Control	0x05B1
0xB6	0x5B	SPIINTSR Access Control	0x05B2
0xB7		SPITSR Access Control	0x05B3
0xB8	0x5C	SPIPOSR Access Control	0x05B4
0xB9		SPI Data Status (SPIDSR and SPIDSMR) Access Control	0x05B5
0xBA	0x5D	SPIC0DR Access Control	0x05B6
0xBB		SPIC1DR Access Control	0x05B7
0xBC	0x5E	SPIC2DR Access Control	0x05B8
0xBD		SPIC3DR Access Control	0x05B9
0xBE	0x5F	SPIC4DR Access Control	0x05BA
0xBF		SPIC5DR Access Control	0x05BB
0xC0	0x60	SPIC6DR Access Control	0x05BC
0xC1		SPIC7DR Access Control	0x05BD
0xC2	0x61	SPIMCR Access Control	0x05BE
0xC3		INTCR Access Control	0x05BF
0xC4	0x62	INTSR Access Control	0x05C0
0xC5		Function Mirror Enable	0x05C1
Other ESC Categories Information (Subdivided in Categories)			
		…	
		Category Strings	
		Category Generals	
		Category FMMU	
		Category SyncManager	
		Category Tx - / RxPDO for each PDO	

Table 2.45-2: ESC I²C EEPROM Layout

Note 1: Reserved words or reserved bits of the ESC Configuration Area should be filled with 0.

Note 2: When (re-) configuring the EEPROM from an EtherCAT master system special care must be taken. Not every master allows writing a category 1 entry to the EEPROM. There are different ways to write this into the EEPROM for automatically loading access control configuration when AX58400 booting.

1. Use preprogrammed I²C EEPROM.
2. Use a different category, e.g., 2049, first. Then overwrite the upper byte with 0 with a single EEPROM byte writes.

The AX58400 HWCFGEE contents from offset 0x00 to 0x7F are mandatory, as well as the general category (at least the minimum I2C EEPROM size is 2Kbit, and for the complex devices with many categories should be equipped with 32 Kbit EEPROMs or larger one). The ESC Configuration Area is used for AX58400 hardware configuration. All other areas are used by the EtherCAT master or the local application.

The ESC Configuration Area (EEPROM offset 0x00 to 0x0F) is automatically read by AX58400 after power-on or reset. It contains the PDI configuration, Distributed Clocks settings, and Configured Station Alias. The consistency of the ESC Configuration Area data is secured with a checksum.

The EtherCAT Master can invoke reloading the EEPROM contents. In this case, the Configured Station Alias register 0x0012:0x0013 and ESC Configuration register bits 0x0141 [1,4,5,6,7] (enhanced link detection) are not transferred into the registers. They are only transferred at the initial EEPROM loading after power-on or reset.

To use AX58400 bridge functionalities, users should define the Bridger Access Configuration parameters in the first category located at EEPROM offset 0x80. The Category Type must be 0x0001and the Category Data Size must be 0x0021 so the AX58400 will automatically load the EEPROM Bridger Access Configuration parameters into the Bridge Access Configuration registers memory area starting at 0x0580 after power-on or reset.

2.45.4.3 EEPROM Contents Detailed Descriptions

PDI Control (0x00)

Bit	Description
7:0	PDI Control [7:0] 0x00: Interface deactivated (no PDI) 0x04: Digital I/O 0x05: SPI Slave 0x08: 16-bit Asynchronous Local Bus 0x09: 8-bit Asynchronous Local Bus Others: reserved

ESC Configuration (0x01)

Bit	Description
0	Device emulation enables (control of AL status)
1	Enhanced Link detection all ports
3:2	Reserved
4	Enhanced Link port 0
5	Enhanced Link port 1
6	Enhanced Link port 2
7	Reserved

PDI Configuration (0x02)

Digital I/O

Bit	Description
0	OUTVALID polarity
1	OUTVALID mode
2	Unidirectional/Bidirectional mode
3	Watchdog behavior
5:4	Input DATA is sampled
7:6	Output DATA is updated

SPI Slave

Bit	Description
1:0	SPI mode
3:2	SPI_IRQ output driver/polarity
4	SPI_SEL polarity
5	Data Out sample mode
7:6	Reserved

Asynchronous Local Bus

Bit	Description
1:0	BUSY/RDY driver/polarity
3:2	IRQ driver/polarity
4	BHE/Byte Enable polarity
7:5	Reserved

Sync/Latch[1:0] Configuration (0x03)

Bit	Description
1:0	SYNC0 output driver/polarity
2	SYNC0/LATCH0 configuration
3	SYNC0 mapped to AL Event Request
5:4	SYNC1 output driver/polarity
6	SYNC1/LATCH1 configuration
7	SYNC1 mapped to AL Event Request

Pulse Length SyncSignals (0x05 - 0x04)

Bit	Description
15:0	Pulse length of SyncSignal

Extended PDI Configuration (0x07 - 0x06)

Digital I/O / SPI Slave (for GPIO)

Bit	Description
0	Digital I/O or GPIO Digital I/O or GPIO are configured in pairs (1:0) as inputs or outputs: 0: Input 1: Output
1	3:2 pair (0: Input, 1: Output)
2	5:4 pair (0: Input, 1: Output)
3	7:6 pair (0: Input, 1: Output)
4	9:8 pair (0: Input, 1: Output)
5	11:10 pair (0: Input, 1: Output)
6	13:12 pair (0: Input, 1: Output)
7	15:14 pair (0: Input, 1: Output)
8	17:16 pair (0: Input, 1: Output)
9	19:18 pair (0: Input, 1: Output)
10	21:20 pair (0: Input, 1: Output)
11	23:22 pair (0: Input, 1: Output)
12	25:24 pair (0: Input, 1: Output)
13	27:26 pair (0: Input, 1: Output)
14	29:28 pair (0: Input, 1: Output)
15	31:30 pair (0: Input, 1: Output)

Asynchronous Local Bus

Bit	Description
0	Read BUSY delay
1	Perform internal write
10:2	Reserved
11	23:22 pair (data bus 8-bit width only) (0: Input, 1: Output)
12	25:24 pair (data bus 8-bit width only) (0: Input, 1: Output)
13	27:26 pair (data bus 8-bit width only) (0: Input, 1: Output)
14	29:28 pair (data bus 8-bit width only) (0: Input, 1: Output)
15	31:30 pair (data bus 8-bit width only) (0: Input, 1: Output)

Configured Station Alias (0x09 - 0x08)

Bit	Description
15:0	Alias Address used for node addressing

Host Interface Extend Setting and Drive Strength (0x0A)

Digital I/O

Bit	Description
4:0	Reserved
5	Control Driving Select: 0: 4mA 1: 8mA
6	IO [9:0] Driving Select: 0: 4mA 1: 8mA
7	IO [15:10] Driving Select: 0: 4mA 1: 8mA

SPI Slave / Asynchronous Local Bus

Bit	Description
3:0	Interrupt Edge Pulse Length (INTP_LEN) Interrupt Edge Pulse = (INTP_LEN+1) * 100ns
4	The trigger type of interrupt signal, SINT / LINT 0: Level trigger. 1: Edge trigger.
5	Control Driving Select: 0: 4mA 1: 8mA
6	IO [9:0] Driving Select: 0: 4mA 1: 8mA
7	IO [15:10] Driving Select: 0: 4mA 1: 8mA

Multi-Function Select and Drive Strength (0x0D)

Bit	Description
0	IO [9:0] select: 0: IO [9:0] 1: MTRG, MDRLD, MSS [3:0], MINT, MMISO, MMOSI, MSCLK, Note: in Local Bus mode this bit no function
1	IO [15:10] (SPI slave separates) select: 0: IO [15:10] 1: IO [15:14], FMOSI, FSCLK, FMISO, SFINT Note: in Local Bus mode this bit no function
2	IO [21:16] select: 0: IO [21:16] 1: PULA, PULB, PULZ, PULZ, PULAB, IO [16] Note: in Local Bus mode this bit no function
3	IO [25:22] select: 0: IO [25:22] 1: PWM2L, PWM2H, PWM3L, PWM3H Note: in Local Bus 16 bits mode this bit no function
4	IO [28:26] select: 0: IO [28:26] 1: EM, PWM1L, PWM1H Note: in Local Bus 16 bits mode this bit no function
5	IO [31:29] select: 0: IO [31:29] 1: ENCZ, ENCB, ENCA Note: in Local Bus 16 bits mode this bit no function

6	IO [21:16] Driving Select: 0: 4mA 1: 8mA
7	IO [31:22] Driving Select: 0: 4mA 1: 8mA

Note: When MII port 2 enable, the IO [31:16] pins are forced to MII port 2

Checksum (0x0F - 0x0E)

Bit	Description
15:0	Checksum Low byte contains remainder of division of EEPROM offset 0x00 to 0x0D as unsigned number divided by the polynomial X^8+X^2+X+1 (initial value 0xFF) For debugging purposes, it is possible to disable the checksum validation with a checksum value of 0x88A4. **Note that NEVER use this for production!**

Category 1 Type (0x81 - 0x80)

Bit	Description
15:0	Category 1 Type MUST be 0x0001

Category 1 Data Size (0x83 - 0x82)

Bit	Description
15:0	Category 1 Data Size (words) MUST be 0x0021

MCTLR Access Control (0x84)

Bit	Description
3:0	Sync. Source Select 0x0: Always triggered 0x1: Start Of Frame (SOF) 0x2: End Of Frame (EOF) 0x3: SYNC0 signal 0x4: LATCH0 signal 0x5: SYNC1 signal 0x6: LATCH1 signal 0x7: After write access 0x8: Trigger when data value changes 0x9: PDI Chip Select Assert 0xA: PDI Chip Select De-assert 0xB: FUNC Chip Select Assert 0xC: FUNC Chip Select De-assert 0xD: Trigger at start of MFC PWM cycle Others: Always triggered
4	ESC Access Enable 0: Writeable with Function Host Interface 1: Writeable with ESC
7:5	Reserved

The Bit Definitions of the other parameters from EEPROM offset 0x85 to 0xC4 are the same as the Bit Definitions of EEPROM offset 0x84.

Function mirror enable (0xC5)

Bit	Description
0	PWM function register mirror: 0: Disable PWM function register mirror 1: Enable PWM function register mirror
1	ENC function register mirror: 0: Disable ENC function register mirror 1: Enable ENC function register mirror
2	SPI Master function register mirror: 0: Disable SPI Master function register mirror 1: Enable SPI Master function register mirror
3	IO Watchdog function register mirror: 0: Disable IO Watchdog function register mirror 1: Enable IO Watchdog function register mirror
7:4	Reserved

2.45.5 Memory Map

This section introduces the memory mapping in AX58400. AX58400 provides SPI and Local Bus slave interfaces for both ESC PDI and Function to access the internal registers. Section 2.45.5.1 introduces the ESC memory map which can be accessed by PDI SPI or Local bus interface ,and section 2.45.5.2 introduces the Function register map which can be accessed by Function SPI or Local Bus interface. Due to the Function registers can be accessed by PDI interface and EtherCAT Master directly. So, section 2.45.5.3 introduces the relationship between Function and ESC PDI through the Bridge function.

2.45.5.1 ESC Memory Map

ESC Address	Length (Bytes)	Description
ESC Information		
0x0000	1	Type
0x0001	1	Revision
0x0002	2	Build
0x0004	1	FMMUs supported
0x0005	1	SyncManagers supported
0x0006	1	RAM Size
0x0007	1	Port Descriptor
0x0008	2	ESC Features supported
Station Address		
0x0010	2	Configured Station Address
0x0012	2	Configured Station Alias
Write Protection		
0x0020	1	Write Register Enable
0x0021	1	Write Register Protection
0x0030	1	ESC Write Enable
0x0031	1	ESC Write Protection
Data Link Layer		
0x0040	1	ESC Reset ECAT
0x0041	1	ESC Reset PDI
0x0100	4	ESC DL Control
0x0108	2	Physical Read/Write Offset
0x0110	2	ESC DL Status
Application Layer		
0x0120	2	AL Control
0x0130	2	AL Status
0x0134	2	AL Status Code
0x0138	1	RUN LED Override
0x0139	1	ERR LED Override
PDI		
0x0140	1	PDI Control
0x0141	1	ESC Configuration
0x0150	1	PDI Configuration
0x0151	1	Sync/Latch PDI Configuration
0x0152	2	Extended PDI Configuration
Interrupts		
0x0200	2	ECAT Event Mask
0x0204	4	AL Event Mask
0x0210	2	ECAT Event Request
0x0220	4	AL Event Request
Error Counters		
0x0300	4x2	RX Error Counter [3:0]
0x0308	4x1	Forwarded RX Error counter [3:0]

0x030C	1	ECAT Processing Unit Error Counter
0x030D	1	PDI Error Counter
0x030E	1	PDI Error Code
0x0310	4x1	Lost Link Counter [3:0]
Watchdogs		
0x0400	2	Watchdog Divider
0x0410	2	Watchdog Time PDI
0x0420	2	Watchdog Time Process Data
0x0440	2	Watchdog Status Process Data
0x0442	1	Watchdog Counter Process Data
0x0443	1	Watchdog Counter PDI
I^2C EEPROM Interface		
0x0500	1	EEPROM Configuration
0x0501	1	EEPROM PDI Access State
0x0502	2	EEPROM Control/Status
0x0504	4	EEPROM Address
0x0508	4	EEPROM Data
MII Management Interface		
0x0510	2	MII Management Control/Status
0x0512	1	PHY Address
0x0513	1	PHY Register Address
0x0514	2	PHY Data
0x0516	1	MII Management ECAT Access State
0x0517	1	MII Management PDI Access State
Bridge Access Configuration		
0x0580	1	MCTLR Access Control Register
0x0581	1	PXCFGR Access Control Register
0x0582	1	PTAPPR Access Control Register
0x0583	1	PTBPPR Access Control Register
0x0584	1	PPCR Access Control Register
0x0585	1	PBBMR Access Control Register
0x0586	1	P1CTRLR Access Control Register
0x0587	1	P1SHR Access Control Register
0x0588	1	P1HPWR Access Control Register
0x0589	1	P2CTRLR Access Control Register
0x058A	1	P2SHR Access Control Register
0x058B	1	P2HPWR Access Control Register
0x058C	1	P3CTRLR Access Control Register
0x058D	1	P3SHR Access Control Register
0x058E	1	P3HPWR Access Control Register
0x058F	1	Step Gap Time Access Control Register
0x0590	1	SHPWR Access Control Register
0x0591	1	TDLYR Access Control Register
0x0592	1	Step Target Number Access Control Register
0x0593	1	SCFGR Access Control Register
0x0594	1	SCTRLR Access Control Register
0x0595	1	Step Counter Content Access Control Register
0x0596	1	Encoder Counter Value Access Control Register
0x0597	1	Encoder Constant Access Control Register
0x0598	1	Encoder Latched Access Control Register
0x0599	1	EMODR Access Control Register
0x059A	1	ECLRR Access Control Register
0x059B	1	HALSTR Access Control Register
0x059C	1	Watchdog Timer Access Control Register
0x059D	1	WCFGR Access Control Register
0x059E	1	WTPVCR Access Control Register

0x059F	1	Watchdog monitored Polarity Access Control Register
0x05A0	1	Watchdog monitored Mask Access Control Register
0x05A1	1	Watchdog Output Mask Access Control Register
0x05A2	1	Watchdog Output Enable Access Control Register
0x05A3	1	Watchdog Output Polarity Access Control Register
0x05A4	1	Watchdog Timer Peak value Access Control Register
0x05A5	1	SPICFGR Access Control Register
0x05A6	1	SPIBRR Access Control Register
0x05A7	1	SPIDBSR Access Control Register
0x05A8	1	SPIDTR Access Control Register
0x05A9	1	SPIRPTR Access Control Register
0x05AA	1	SPILTR Access Control Register
0x05AB	1	SPIPRLR Access Control Register
0x05AC	1	SPI01BCR Access Control Register
0x05AD	1	SPI23BCR Access Control Register
0x05AE	1	SPI45BCR Access Control Register
0x05AF	1	SPI67BCR Access Control Register
0x05B0	1	SPI03SSR Access Control Register
0x05B1	1	SPI47SSR Access Control Register
0x05B2	1	SPINTSR Access Control Register
0x05B3	1	SPITSR Access Control Register
0x05B4	1	SPIPOSR Access Control Register
0x05B5	1	SPI Data Status (SPIDSR and SPIDSMR) Access Control Register
0x05B6	1	SPIC0DR Access Control Register
0x05B7	1	SPIC1DR Access Control Register
0x05B8	1	SPIC2DR Access Control Register
0x05B9	1	SPIC3DR Access Control Register
0x05BA	1	SPIC4DR Access Control Register
0x05BB	1	SPIC5DR Access Control Register
0x05BC	1	SPIC6DR Access Control Register
0x05BD	1	SPIC7DR Access Control Register
0x05BE	1	SPIMCR Access Control Register
0x05BF	1	INTCR Access Control Register
0x05C0	1	INTSR Access Control Register
0x05C1	1	Function Mirror Enable Register
0x0600:0x067F	**FMMU[7:0]**	
+0x0	4	Logical Start Address
+0x4	2	Length
+0x6	1	Logical Start bit
+0x7	1	Logical Stop bit
+0x8	2	Physical Start Address
+0xA	1	Physical Start bit
+0xB	1	Type
+0xC	1	Activate
+0xD	3	Reserved
0x0800:0x083F	**SyncManager[7:0]**	
+0x0	2	Physical Start Address
+0x2	2	Length
+0x4	1	Control Register
+0x5	1	Status Register
+0x6	1	Activate
+0x7	1	PDI Control
0x0900:0x09FF	**Distributed Clocks (DC)**	
DC – Receive Times		
0x0900	4	Receive Time Port 0
0x0904	4	Receive Time Port 1

0x0908	4	Receive Time Port 2
0x090C	4	Receive Time Port 3
DC – Time Loop Control Unit		
0x0910	4(W)/8(R)	System Time
0x0918	8	Receive Time ECAT Processing Unit
0x0920	8	System Time Offset
0x0928	4	System Time Delay
0x092C	4	System Time Difference
0x0930	2	Speed Counter Start
0x0932	2	Speed Counter Diff
0x0934	1	System Time Difference Filter Depth
0x0935	1	Speed Counter Filter Depth
DC – Cyclic Unit Control		
0x0980	1	Cyclic Unit Control
DC – SYNC Out Unit		
0x0981	1	Activation
0x0982	2	Pulse Length of SyncSignals
0x0984	1	Activation Status
0x098E	1	SYNC0 Status
0x098F	1	SYNC1 Status
0x0990	8	Start Time Cyclic Operation/Next SYNC0 Pulse
0x0998	8	Next SYNC1 Pulse
0x09A0	4	SYNC0 Cycle Time
0x09A4	4	SYNC1 Cycle Time
DC – Latch In Unit		
0x09A8	1	Latch0 Control
0x09A9	1	Latch1 Control
0x09AE	1	Latch0 Status
0x09AF	1	Latch1 Status
0x09B0	8	Latch0 Time Positive Edge
0x09B8	8	Latch0 Time Negative Edge
0x09C0	8	Latch1 Time Positive Edge
0x09C8	8	Latch1 Time Negative Edge
DC – SyncManager Event Times		
0x09F0	4	EtherCAT Buffer Change Event Time
0x09F8	4	PDI Buffer Start Event Time
0x09FC	4	PDI Buffer Change Event Time
ESC specific		
0x0E00	8	Product ID
0x0E08	8	Vendor ID
Digital Input/Output		
0x0F00	4	Digital I/O Output Data
0x0F10	4	General Purpose Outputs
0x0F18	4	General Purpose Inputs
User RAM/Extended ESC features		
0x0F80	128	User RAM/Extended ESC Features
Process Data RAM		
0x1000	4	Digital I/O Input Data
0x1000	8KB	Process Data RAM
Function Register Mirror (Refer to Section 2.45.5.2)		
Write / Read		
0x3000	2	Motor Control Register
0x3002	2	PWM Pulse X Configure Register
0x3004	2	PWM Trigger A Pulse Position Register
0x3006	2	PWM Trigger B Pulse Position Register
0x3008	2	PWM Period Cycle Register

0x300A	2	PWM Pulse Break Before Make Register
0x300C	2	PWM1Control Register
0x300E	2	PWM1 Counter Shift Register
0x3010	2	PWM1 High Pulse Width Register
0x3012	2	PWM2 Control Register
0x3014	2	PWM2 Shift Register
0x3016	2	PWM2 High Pulse Width Register
0x3018	2	PWM3 Control Register
0x301A	2	PWM3 Counter Shift Register
0x301C	2	PWM3 High Pulse Width Register
0x3020	4	Step Gap Time Register
0x3024	2	Step High Pulse Width Register
0x3026	2	Direction Transform Delay Step Register
0x3028	4	Step Target Number Register
0x302C	2	Step Configure Register
0x302E	2	Step Control Register
0x3040	4	Encoder Counter Value Register
0x3044	4	Encoder Constant Register
0x304C	2	Encoder Mode configuration Register
0x304E	2	Encoder Clear Register
0x3060	4	Watchdog Timer Register
0x3064	2	Watchdog Control Register
0x3066	2	Watchdog Timer Peak Value Clear Register
0x3068	4	Watchdog Monitored Signals Polarity Register
0x306C	4	Watchdog Monitored Signals Mask Register
0x3070	4	Watchdog Output Mask Register
0x3074	4	Watchdog Output Enable Register
0x3078	4	Watchdog Output Polarity Register
0x3080	2	SPI Configure Register
0x3082	2	SPI Baud Rate Register
0x3084	2	SPI Delay Byte and SS Register
0x3086	2	SPI Delay Transfer Register
0x3088	2	SPI RDY / Pulse Time Register
0x308A	2	SPI LDAC Time Register
0x308C	2	SPI Pulse/ RDY/ LDAC Register
0x3090	2	SPI 0/1 Byte Count Register
0x3092	2	SPI 2/3 Byte Count Register
0x3094	2	SPI 4/5 Byte Count Register
0x3096	2	SPI 6/7 Byte Count Register
0x3098	2	SPI 0/1/2/3 slave Select Register
0x309A	2	SPI 4/5/6/7 slave Select Register
0x30B0	8	SPI Channel 0 Data Register
0x30B8	8	SPI Channel 1 Data Register
0x30C0	8	SPI Channel 2 Data Register
0x30C8	8	SPI Channel 3 Data Register
0x30D0	8	SPI Channel 4 Data Register
0x30D8	8	SPI Channel 5 Data Register
0x30E0	8	SPI Channel 6 Data Register
0x30E8	8	SPI Channel 7 Data Register
0x30F2	2	SPI Master Control Register
0x3100	2	Interrupt Configure Register
0x3102	2	Interrupt Status Register
Read Only		
0x3230	4	Step Counter Content Register
0x3248	4	Encoder Latched Register
0x3250	2	Hall State Register

0x327C	4	Watchdog Timer Peak Value Register
0x32A8	2	SPI Interrupt Status Register
0x32AA	2	SPI Timeout Status Register
0x32AC	2	SPI Pulse Overrun Status Register
0x32AE	2	SPI Data Status Register
0x32B0	8	SPI Channel 0 Data Register
0x32B8	8	SPI Channel 1 Data Register
0x32C0	8	SPI Channel 2 Data Register
0x32C8	8	SPI Channel 3 Data Register
0x32D0	8	SPI Channel 4 Data Register
0x32D8	8	SPI Channel 5 Data Register
0x32E0	8	SPI Channel 6 Data Register
0x32E8	8	SPI Channel 7 Data Register
0x32F0	2	SPI Data Status Mirror Register

Table 2.45-3: ESC Memory Map

2.45.5.2 Function Register Map

Address Offset	Name	Description
0x000	MCTLR	Motor Control Register
0x002	PXCFGR	PWM Pulse X Configure Register
0x004	PTAPPR	PWM Trigger A Pulse Position Register
0x006	PTBPPR	PWM Trigger B Pulse Position Register
0x008	PPCR	PWM Period Cycle Register
0x00A	PBBMR	PWM Pulse Break Before Make Register
0x00C	P1CTRLR	PWM1Control Register
0x00E	P1SHR	PWM1 Counter Shift Register
0x010	P1HPWR	PWM1 High Pulse Width Register
0x012	P2CTRLR	PWM2 Control Register
0x014	P2SHR	PWM2 Shift Register
0x016	P2HPWR	PWM2 High Pulse Width Register
0x018	P3CTRLR	PWM3 Control Register
0x01A	P3SHR	PWM3 Counter Shift Register
0x01C	P3HPWR	PWM3 High Pulse Width Register
0x020	SGTLR	Step Gap Time Low Register
0x022	SGTHR	Step Gap Time High Register
0x024	SHPWR	Step High Pulse Width Register
0x026	TDLYR	direction Transform Delay step Register
0x028	STNLR	Step Target Number Low Word Register
0x02A	STNHR	Step Target Number High Word Register
0x02C	SCFGR	Step Configure Register
0x02E	SCTRLR	Step Control Register
0x030	SCNTLR	Step Counter Content Low Register
0x032	SCNTHR	Step Counter Content High Register
0x040	ECNTVLR	Encoder Counter value Low Register
0x042	ECNTVHR	Encoder Counter value High Register
0x044	ECNSTLR	Encoder Constant Low Register
0x046	ECNSTHR	Encoder Constant High Register
0x048	ELATLR	Encoder Latched Low Register
0x04A	ELATHR	Encoder Latched High Register
0x04C	EMODR	Encoder Mode Configuration Register
0x04E	ECLRR	Encoder Clear Register
0x050	HALSTR	Hall State Register
0x060	WTLR	Watchdog Timer Low Register
0x062	WTHR	Watchdog Timer High Register
0x064	WCFGR	Watchdog Configure Register
0x066	WTPVCR	Watchdog Timer Peak Value Clear Register
0x068	WMPLR	Watchdog Monitored Polarity Low Register
0x06A	WMPHR	Watchdog Monitored Polarity High Register
0x06C	WMMLR	Watchdog Monitored Mask Low Register
0x06E	WMMHR	Watchdog Monitored Mask High Register
0x070	WOMLR	Watchdog Output Mask Low Register
0x072	WOMHR	Watchdog Output Mask High Register
0x074	WOELR	Watchdog Output Enable Low Register
0x076	WOEHR	Watchdog Output Enable High Register
0x078	WOPLR	Watchdog Output Polarity Low Register
0x07A	WOPHR	Watchdog Output Polarity High Register
0x07C	WTPVLR	Watchdog Timer Peak Value Low Register
0x07E	WTPVHR	Watchdog Timer Peak Value High Register
0x080	SPICFGR	SPI Configure Register
0x082	SPIBRR	SPI Baud Rate Register
0x084	SPIDBSR	SPI Delay Byte and SS Register

Address Offset	Name	Description
0x086	SPIDTR	SPI Delay Transfer Register
0x088	SPIRPTR	SPI RDY / Pulse Time Register
0x08A	SPILTR	SPI LDAC Time Register
0x08C	SPIPRLR	SPI Pulse/ RDY/ LDAC Register
0x090	SPI01BCR	SPI 0/1 Byte Count Register
0x092	SPI23BCR	SPI 2/3 Byte Count Register
0x094	SPI45BCR	SPI 4/5 Byte Count Register
0x096	SPI67BCR	SPI 6/7 Byte Count Register
0x098	SPI03SSR	SPI 0/1/2/3 slave Select Register
0x09A	SPI47SSR	SPI 4/5/6/7 slave Select Register
0x0A8	SPINTSR	SPI Interrupt Status Register
0x0AA	SPITSR	SPI Timeout Status Register
0x0AC	SPIPOSR	SPI Pulse Overrun Status Register
0x0AE	SPIDSR	SPI Data Status Register
0x0B0	SPIC0DR	SPI Channel 0 Data Register
0x0B8	SPIC1DR	SPI Channel 1 Data Register
0x0C0	SPIC2DR	SPI Channel 2 Data Register
0x0C8	SPIC3DR	SPI Channel 3 Data Register
0x0D0	SPIC4DR	SPI Channel 4 Data Register
0x0D8	SPIC5DR	SPI Channel 5 Data Register
0x0E0	SPIC6DR	SPI Channel 6 Data Register
0x0E8	SPIC7DR	SPI Channel 7 Data Register
0x0F0	SPIDSMR	SPI Data Status Mirror Register
0x0F2	SPIMCR	SPI Master Control Register
0x100	INTCR	Interrupt Configure Register
0x102	INTSR	Interrupt Status Register
0x104	ESTOR	ESC State Override register
0x106	HSTSR	Host interface Status Register
Others	Reserved	Reserved

Table 2.45-4: ESC Function Register Map

2.45.5.3 Memory Map between ESC Memory and Function Registers

Function Address	ESC Address		Name	Description
	R/W	RO		
0x000	0x3000	-	MCTLR	Motor Control Register
0x002	0x3002	-	PXCFGR	PWM Pulse X Configure Register
0x004	0x3004	-	PTAPPR	PWM Trigger A Pulse Position Register
0x006	0x3006	-	PTBPPR	PWM Trigger B Pulse Position Register
0x008	0x3008	-	PPCR	PWM Period Cycle Register
0x00A	0x300A	-	PBBMR	PWM Pulse Break Before Make Register
0x00C	0x300C	-	P1CTRLR	PWM1Control Register
0x00E	0x300E	-	P1SHR	PWM1 Counter Shift Register
0x010	0x3010	-	P1HPWR	PWM1 High Pulse Width Register
0x012	0x3012	-	P2CTRLR	PWM2 Control Register
0x014	0x3014	-	P2SHR	PWM2 Shift Register
0x016	0x3016	-	P2HPWR	PWM2 High Pulse Width Register
0x018	0x3018	-	P3CTRLR	PWM3 Control Register
0x01A	0x301A	-	P3SHR	PWM3 Counter Shift Register
0x01C	0x301C	-	P3HPWR	PWM3 High Pulse Width Register
0x020	0x3020	-	SGTLR	Step Gap Time Low Register
0x022			SGTHR	Step Gap Time High Register
0x024	0x3024	-	SHPWR	Step High Pulse Width Register
0x026	0x3026	-	TDLYR	direction Transform Delay step Register
0x028	0x3028	-	STNLR	Step Target Number Low Word Register
0x02A			STNHR	Step Target Number High Word Register
0x02C	0x302C	-	SCFGR	Step Configure Register
0x02E	0x302E	-	SCTRLR	Step Control Register
0x030	-	0x3230	SCNTLR	Step Counter Content Low Register
0x032			SCNTHR	Step Counter Content High Register
0x040	0x3040	-	ECNTVLR	Encoder Counter value Low Register
0x042			ECNTVHR	Encoder Counter value High Register
0x044	0x3044	-	ECNSTLR	Encoder Constant Low Register
0x046			ECNSTHR	Encoder Constant High Register
0x048	-	0x3248	ELATLR	Encoder Latched Low Register
0x04A			ELATHR	Encoder Latched High Register
0x04C	0x304C	-	EMODR	Encoder Mode Configuration Register
0x04E	0x304E	-	ECLRR	Encoder Clear Register
0x050	-	0x3250	HALSTR	Hall State Register
0x060	0x3060	-	WTLR	Watchdog Timer Low Register
0x062			WTHR	Watchdog Timer High Register
0x064	0x3064	-	WCFGR	Watchdog Configure Register
0x066	0x3066	-	WTPVCR	Watchdog Timer Peak Value Clear Register
0x068	0x3068	-	WMPLR	Watchdog Monitored Polarity Low Register
0x06A			WMPHR	Watchdog Monitored Polarity High Register
0x06C	0x306C	-	WMMLR	Watchdog Monitored Mask Low Register
0x06E			WMMHR	Watchdog Monitored Mask High Register
0x070	0x3070	-	WOMLR	Watchdog Output Mask Low Register
0x072			WOMHR	Watchdog Output Mask High Register
0x074	0x3074	-	WOELR	Watchdog Output Enable Low Register
0x076			WOEHR	Watchdog Output Enable High Register
0x078	0x3078	-	WOPLR	Watchdog Output Polarity Low Register
0x07A			WOPHR	Watchdog Output Polarity High Register
0x07C	-	0x327C	WTPVLR	Watchdog Timer Peak Value Low Register
0x07E			WTPVHR	Watchdog Timer Peak Value High Register
0x080	0x3080	-	SPICFGR	SPI Configure Register
0x082	0x3082	-	SPIBRR	SPI Baud Rate Register
0x084	0x3084	-	SPIDBSR	SPI Delay Byte and SS Register

Function Address	ESC Address		Name	Description
	R/W	RO		
0x086	0x3086	-	SPIDTR	SPI Delay Transfer Register
0x088	0x3088	-	SPIRPTR	SPI RDY / Pulse Time Register
0x08A	0x308A	-	SPILTR	SPI LDAC Time Register
0x08C	0x308C	-	SPIPRLR	SPI Pulse/ RDY/ LDAC Register
0x090	0x3090	-	SPI01BCR	SPI 0/1 Byte Count Register
0x092	0x3092	-	SPI23BCR	SPI 2/3 Byte Count Register
0x094	0x3094	-	SPI45BCR	SPI 4/5 Byte Count Register
0x096	0x3096	-	SPI67BCR	SPI 6/7 Byte Count Register
0x098	0x3098	-	SPI03SSR	SPI 0/1/2/3 slave Select Register
0x09A	0x309A	-	SPI47SSR	SPI 4/5/6/7 slave Select Register
0x0A8	-	0x32A8	SPINTSR	SPI Interrupt Status Register
0x0AA	-	0x32AA	SPITSR	SPI Timeout Status Register
0x0AC	-	0x32AC	SPIPOSR	SPI Pulse Overrun Status Register
0x0AE	-	0x32AE	SPIDSR	SPI Data Status Register
0x0B0	0x30B0	0x32B0	SPIC0DR	SPI Channel 0 Data Register
0x0B8	0x30B8	0x32B8	SPIC1DR	SPI Channel 1 Data Register
0x0C0	0x30C0	0x32C0	SPIC2DR	SPI Channel 2 Data Register
0x0C8	0x30C8	0x32C8	SPIC3DR	SPI Channel 3 Data Register
0x0D0	0x30D0	0x32D0	SPIC4DR	SPI Channel 4 Data Register
0x0D8	0x30D8	0x32D8	SPIC5DR	SPI Channel 5 Data Register
0x0E0	0x30E0	0x32E0	SPIC6DR	SPI Channel 6 Data Register
0x0E8	0x30E8	0x32E8	SPIC7DR	SPI Channel 7 Data Register
0x0F0	-	0x32F0	SPIDSMR	SPI Data Status Mirror Register
0x0F2	0x30F2	-	SPIMCR	SPI Master Control Register
0x100	0x3100	-	INTCR	Interrupt Configure Register
0x102	0x3102	-	INTSR	Interrupt Status Register

Table 2.45-5: ESC Memory and Function Registers Mirror Mapping Table

3 Electrical Specifications

3.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to GND(V_{SS}).

3.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with an junction temperature at T_J = 25 °C and T_J = T_{Jmax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

3.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

3.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

3.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 3.1-1.

3.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 3.1-2.

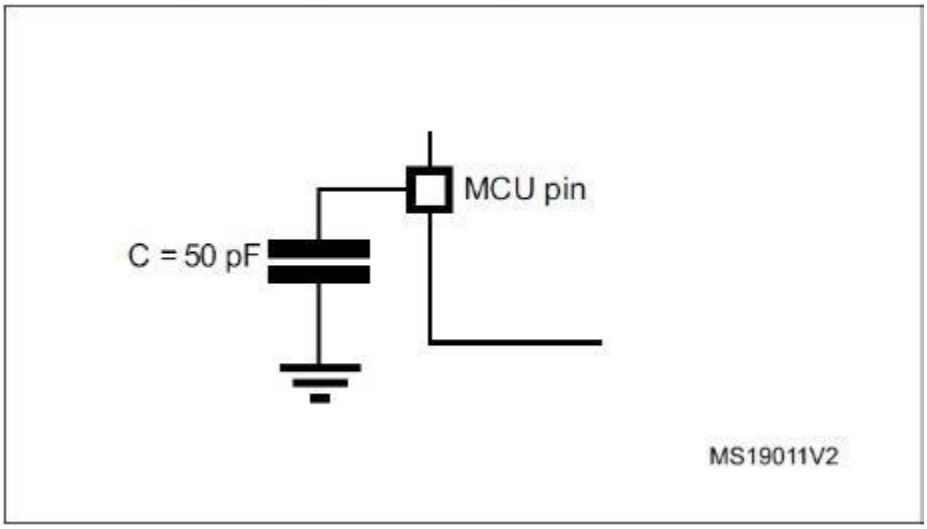


Figure 3.1-1: Pin loading conditions

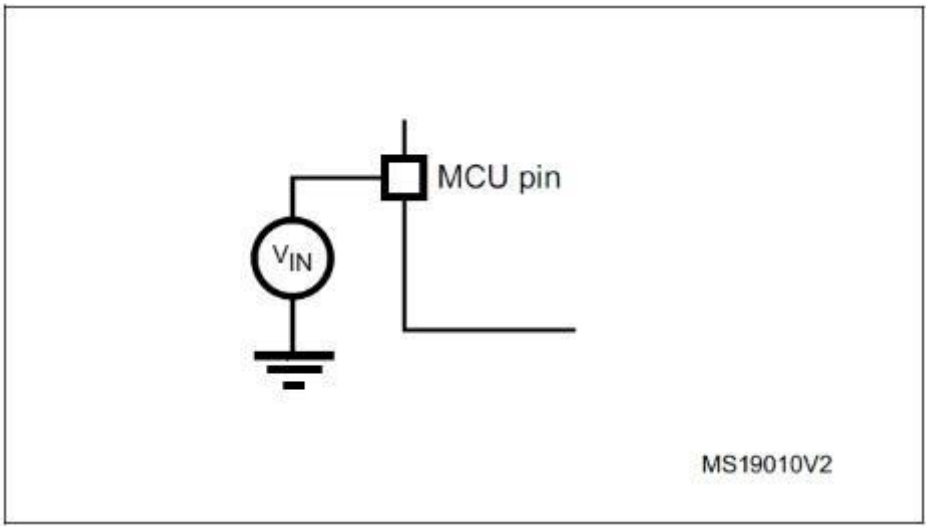
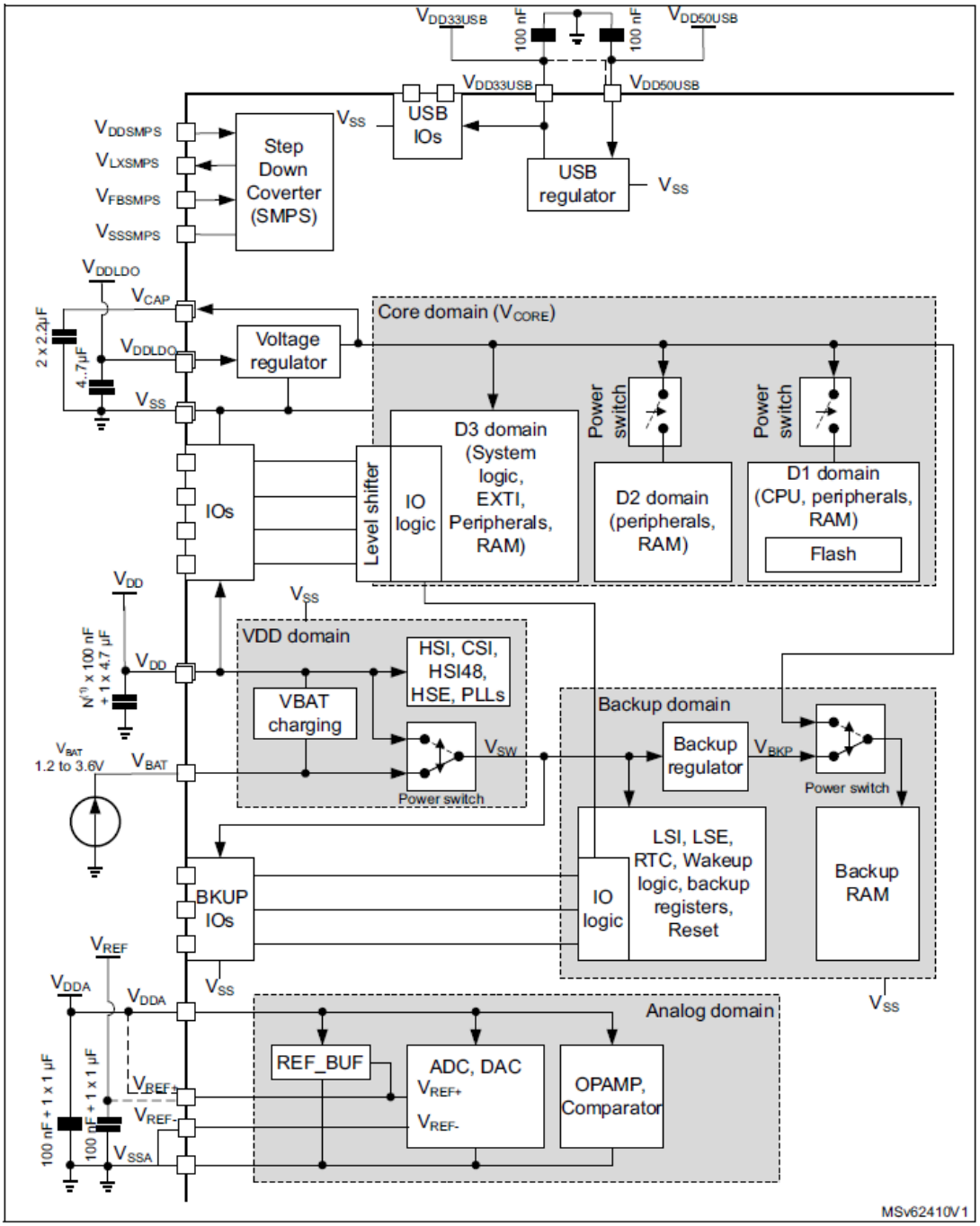


Figure 3.1-2: Pin input voltage

3.1.6 Power supply scheme



1. N corresponds to the number of VDD pins available on the package.
2. A tolerance of +/- 20% is acceptable on decoupling capacitors.

Figure 3.1-3: Power supply scheme

Caution: Each power supply pair (V_{DD}/GND(V_{SS}), V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

3.1.7 Current consumption measurement

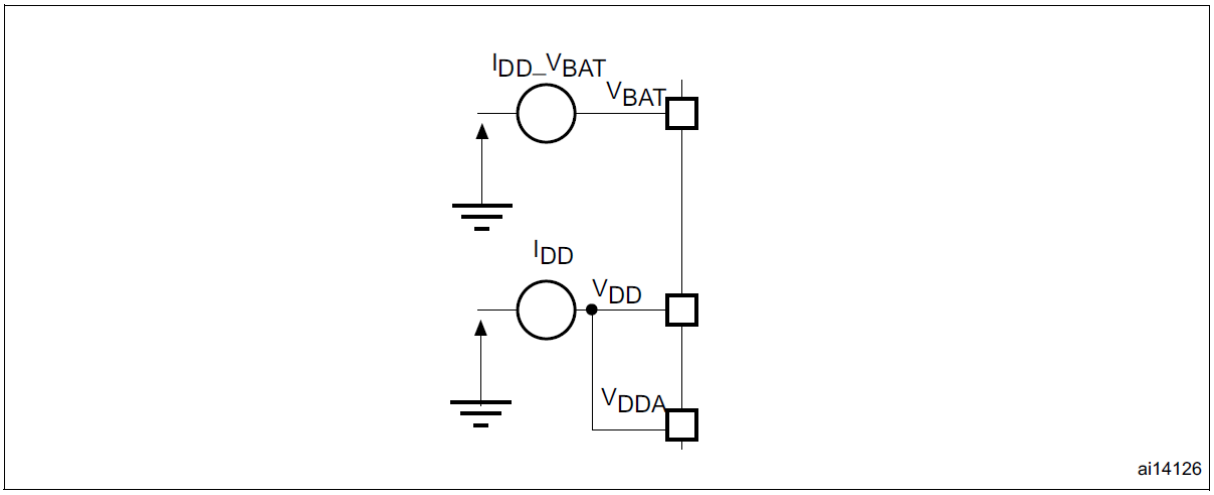


Figure 3.1-4: Current consumption measurement scheme

3.2 Absolute Maximum Ratings

Stresses above the absolute maximum ratings listed in Table 3.2-1: Voltage characteristics(1), Table 3.2-2: Current characteristics, and Table 3.2-3: Thermal characteristics may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbols	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDLDO}, V_{DDSMPS}, V_{DDA}, $V_{DD33USB}$, V_{BAT})	−0.3	4.0	V
VCC3IO, VCC33A	Power supply of 3.3V I/O for ESC sub-system and Ethernet PHY	−0.3	4.0	V
VCCK	Digital core power supply for ESC sub-system	−0.5	1.6	V
VCC12A_PLL	Analog power supply for PLL for ESC sub-system	−0.5	1.6	V
V_{IN}(2)	Input voltage on FT_xxx pins	GND−0.3	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{BAT}) +4.0(3)(4)	V
	Input voltage on TT_xx pins	GND -0.3	4.0	V
	Input voltage on BOOT0 pin	GND	9.0	V
	Input voltage on any other pins	GND -0.3	4.0	V
	Input voltage of 3.3V I/O with 5V tolerant(VCC3IO domain).	GND -0.3	5.5	V
$\|\Delta V_{DDX}\|$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins	-	50	mV
I_{IN}	DC input current (VCC3IO domain).		50	mA
I_{OUT}	Output short circuit current (VCC3IO domain).		50	mA

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{DDSMPS}, V_{BAT}) and ground (GND, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to Table 3.3-46: I/O current injection susceptibility(1) for the maximum allowed injected current values.
3. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
4. To sustain a voltage higher than 4V the internal pull-up/pull-down resistors must be disabled.

Table 3.2-1: Voltage characteristics(1)

Symbols	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines(source)(1)	620	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines(sink)(1)	620	
IV_{DD}	Maximum current into each V_{DD} power pin (source)(1)	100	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, RST and B pins except PA4, PA5	−5/+0	
	Injected current on PA4, PA5	−0/0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$) and ground (GND, V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by VIN>VDD while a negative injection is induced by VIN<VSS. IINJ(PIN) must never be exceeded. Refer also to Table 3.2-1: Voltage characteristics(1) for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum ∑IINJ(PIN) is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 3.2-2: Current characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	– 65 to +150	℃
T_J	Maximum junction temperature	125	

Table 3.2-3: Thermal characteristics

3.3 Recommended Operating Conditions for Main System

3.3.1 General operating conditions

Symbol	Parameter	Operatingconditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	-	1.62(1)	-	3.6	V
V_{DDLDO}	Supply voltage for the internal regulator	$V_{DDLDO} \leq V_{DD}$	1.62(1)	-	3.6	V
			1.2(2)	-	3.6	
V_{DDSMPS}	Supply voltage for the internal SMPS Step-down converter	$V_{DDSMPS} = V_{DD}$	1.62(1)	-	3.6	V
$V_{DD33USB}$	Standard operating voltage, USB domain	USB used	3.0	-	3.6	V
		USB not used	0	-	3.6	
V_{DDA}	Analog operating voltage	ADC or COMP used	1.62	-	3.6	
		DAC used	1.8	-		
		OPAMP used	2.0	-		
		VREFBUF used	1.8	-		
		ADC, DAC, OPAMP, COMP, VREFBUFnot used	0	-		
V_{IN}	I/O Input voltage	TT_xx I/O	−0.3	-	V_{DD}+0.3	V
		BOOT0	0	-	9	
		All I/O except BOOT0 and TT_xx	−0.3	-	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$) +3.6V < 5.5V(3)(4)	
V_{CORE}	Internal regulator ON (LDO)	VOS3 (max frequency 200 MHz)	0.95	1.0	1.26	V
		VOS2 (max frequency 300 MHz)	1.05	1.10	1.26	
		VOS1 (max frequency 400 MHz)	1.15	1.20	1.26	
		VOS0(5) (max frequency 480 MHz(6))	1.26	1.35	1.40	
	Internal regulator ON (SMPS step- down converter)(7)	VOS3 (max frequency 200 MHz)	0.95	1.0	1.26	
		VOS2 (max frequency 300 MHz)	1.05	1.10	1.26	
		VOS1 (max frequency 400 MHz)	1.15	1.20	1.26	
	Regulator OFF: external V_{CORE} voltage must be supplied from external regulator on two VCAP pins	VOS3 (max frequency 200 MHz)	0.98	1.03	1.26	
		VOS2 (max frequency 300 MHz)	1.08	1.13	1.26	
		VOS1 (max frequency 400 MHz)	1.17	1.23	1.26	
		VOS0 (max frequency 480 MHz(6))	1.37	1.38	1.40	

Symbol	Parameter	Operatingconditions	Min	Typ	Max	Unit
f_{CPU1}	Arm® Cortex®-M7 clock frequency	VOS3	-	-	200	MHz
		VOS2	-	-	300	
		VOS1	-	-	400	
		VOS0	-	-	480(6)	
f_{CPU2}	Arm® Cortex®-M4 clock frequency	VOS3	-	-	200	
		VOS2	-	-	150	
		VOS1	-	-	200	
		VOS0	-	-	240(6)	
f_{ACLK}	AXI clock frequency	VOS3	-	-	100	
		VOS2	-	-	150	
		VOS1	-	-	200	
		VOS0	-	-	240(6)	
f_{HCLK}	AHB clock frequency	VOS3	-	-	100	
		VOS2	-	-	150	
		VOS1	-	-	200	
		VOS0	-	-	240(6)	
f_{PCLK}	APB clock frequency	VOS3	-	-	50(8)	
		VOS2	-	-	75	
		VOS1	-	-	100	
		VOS0	-	-	120(6)	

1. When RESET is released functionality is guaranteed down to V_{BOR0} min
2. Only for power-up sequence when the SMPS step-down converter is configured to supply the LDO and T_{JMax} = 105 °C.
3. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
4. For operation with voltage higher than Min (V_{DD}, V_{DDA}, $V_{DD33USB}$) +0.3V, the internal Pull-up and Pull-Down resistors must be disabled.
5. VOS0 is available only when the LDO regulator is ON.
6. T_{Jmax} = 105 °C.
7. At startup, the external V_{CORE} voltage must remain higher or equal to 1.10 V before disabling the internal regulator (LDO).
8. Maximum APB clock frequency when at least one peripheral is enabled.

Table 3.3-1: General operating conditions

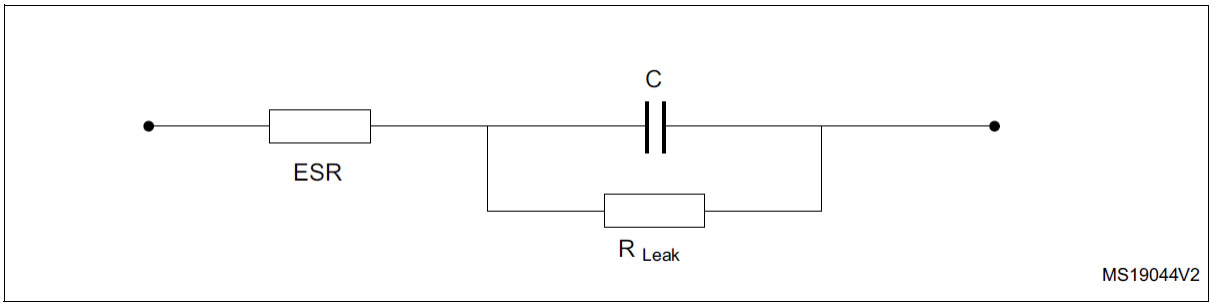
Power scale	V_{CORE} source	Max T_J (°C)	Max frequency (MHz)	Min V_{DD} (V)
VOS0	LDO	105	480	1.7
	SMPS step-down converter(1)	-	-	-
VOS1	LDO	125	400	1.62
	SMPS step-down converter			
VOS2	LDO	125	300	1.62
	SMPS step-down converter	125		
		140		
VOS3	LDO(2)	105	64	1.2(2)
	LDO	125	200	1.62
	SMPS step-down converter	125		
		140(3)		
SVOS4	LDO	105	N/A	1.62
	SMPS step-down converter	125		
		140(3)		
SVOS5	LDO	105	N/A	1.62
	SMPS step-down converter	125		
		140(3)		

1. VOS0 (power scale 0) is not available when the SMPS step-down converter directly supplies V_{CORE}.
2. Only for power-up sequence when the SMPS step-down converter supplies the LDO.
3. Extended Industrial temperature range sales types (range 3).

Table 3.3-2: Supply voltage and maximum frequency configuration

3.3.2 VCAP external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP pin. C_{EXT} is specified in Table 3.3-3. Two external capacitors can be connected to VCAP pins.



1. Legend: ESR is the equivalent series resistance.

Figure 3.3-1: External capacitor C_{EXT}

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF(2)
ESR	ESR of external capacitor	< 100 mΩ

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.
2. This value corresponds to CEXT typical value. A variation of +/-20% is tolerated.

Table 3.3-3: VCAP operating conditions(1)

3.3.3 SMPS step-down converter

The devices embed a high power efficiency SMPS step-down converter. SMPS characteristics for external usage are given in Table 3.3-5. The SMPS step-down converter requires external components that are specified in Figure 3.3-2 and Table 3.3-4.

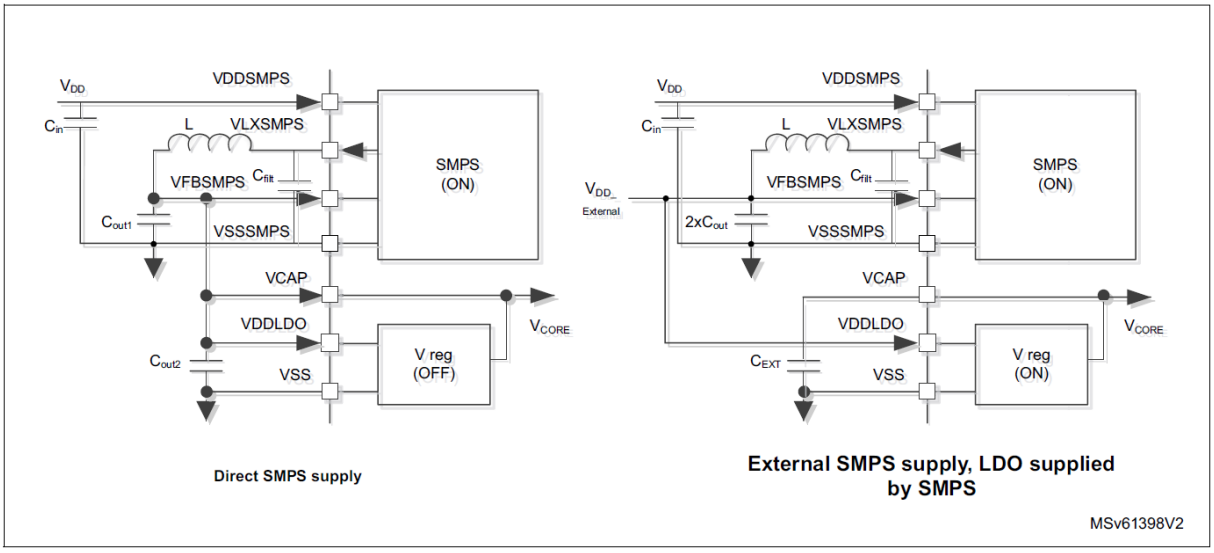


Figure 3.3-2: External components for SMPS step-down converter

Symbol	Parameter	Conditions
C_{in}	Capacitance of external capacitor on V_{DDSMPS}	4.7 µF
	ESR of external capacitor	100 mΩ
C_{filt}	Capacitance of external capacitor on V_{LXSMPS} pin	220 pF
C_{OUT}	Capacitance of external capacitor on V_{FBSMPS} pin	10 µF
	ESR of external capacitor	20 mΩ
L	Inductance of external Inductor on V_{LXSMPS} pin	2.2 µH
-	Serial DC resistor	150 mΩ
I_{SAT}	DC current at which the inductance drops 30% from its value without current.	1.7 A
I_{RMS}	Average current for a 40 °C rise: rated current for which the temperature of the inductor is raised 40°C by DC current	1.4 A

Table 3.3-4: Characteristics of SMPS step-down converter external components

Parameters	Conditions	Min	Typ	Max	Unit
V_{DDSMPS}(1)	V_{OUT} = 1.8 V	2.3	-	3.6	V
	V_{OUT} = 2.5 V	3	-	3.6	
V_{OUT} (2)	Iout=600 mA	2.25	2.5	2.75	V
		1.62	1.8	1.98	
I_{OUT}	internal and external usage	-	-	600	mA
	External usage only(3)	-	-	600	
RDS_{ON}	-	-	100	120	mΩ
I_{DDSMPS_Q}	Quiescent current	-	220	-	µA
T_{SMPS_START}	V_{OUT} = 1.8 V	-	-	225	µs
	V_{OUT} = 2.5 V	-	-	300	

1. The switching frequency is 2.4 MHz±10%

2. Including line transient and load transient.

3. These characteristics are given for SDEXTHP bit is set in the PWR_CR3 register.

Table 3.3-5: SMPS step-down converter characteristics for external usage

3.3.4 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10	∞	
t_{VDDA}	V_{DDA} rise time rate	0	∞	
	V_{DDA} fall time rate	10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	0	∞	
	V_{DDUSB} fall time rate	10	∞	

Table 3.3-6: Operating conditions at power-up / power-down (regulator ON)

3.3.5 Embedded reset and power control block characteristics

The parameters given in Table 3.3-7 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 3.3-1: General operating conditions.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization after BOR0 released	-	-	377	-	µs
V_{BOR0}	Brown-out reset threshold 0	Rising edge(1)	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.04	2.10	2.15	
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.34	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.63	2.70	2.78	
		Falling edge	2.54	2.61	2.68	
V_{PVD0}	Programmable Voltage Detector threshold 0	Rising edge	1.90	1.96	2.01	
		Falling edge	1.81	1.86	1.91	
V_{PVD1}	Programmable Voltage Detector threshold 1	Rising edge	2.05	2.10	2.16	
		Falling edge	1.96	2.01	2.06	
V_{PVD2}	Programmable Voltage Detector threshold 2	Rising edge	2.19	2.26	2.32	
		Falling edge	2.10	2.15	2.21	
V_{PVD3}	Programmable Voltage Detector threshold 3	Rising edge	2.35	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{PVD4}	Programmable Voltage Detector threshold 4	Rising edge	2.49	2.56	2.62	
		Falling edge	2.39	2.45	2.51	
V_{PVD5}	Programmable Voltage Detector threshold 5	Rising edge	2.64	2.71	2.78	
		Falling edge	2.55	2.61	2.68	
V_{PVD6}	Programmable Voltage	Rising edge	2.78	2.86	2.94	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Detector threshold 6	Falling edge in Run mode	2.69	2.76	2.83	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BOR (unless BOR0) and PVD	Hysteresis in Run mode	-	100	-	mV
$I_{DD\_BOR\_PVD}$(1)	BOR(2) (unless BOR0) and PVD consumption from V_{DD}	-	-		0.630	µA
V_{AVM_0}	Analog voltage detector for V_{DDA} threshold 0	Rising edge	1.66	1.71	1.76	V
		Falling edge	1.56	1.61	1.66	
V_{AVM_1}	Analog voltage detector for V_{DDA} threshold 1	Rising edge	2.06	2.12	2.19	
		Falling edge	1.96	2.02	2.08	
V_{AVM_2}	Analog voltage detector for V_{DDA} threshold 2	Rising edge	2.42	2.50	2.58	
		Falling edge	2.35	2.42	2.49	
V_{AVM_3}	Analog voltage detector for V_{DDA} threshold 3	Rising edge	2.74	2.83	2.91	
		Falling edge	2.64	2.72	2.80	
V_{hyst_VDDA}	Hysteresis of V_{DDA} voltage detector	-	-	100	-	mV
I_{DD_PVM}	PVM consumption from $V_{DD(1)}$	-	-	--	0.25	µA
V_{DD_VDDA}	Voltage detector consumption on V_{DD} (1)	Resistor bridge	-	-	2.5	µA

1. Guaranteed by design.
2. BOR0 is enabled in all modes and its consumption is therefore included in the supply current characteristics tables (refer to Section 3.3.7: Supply current characteristics).

Table 3.3-7: Reset and power control block characteristics

3.3.6 Embedded reference voltage

The parameters given in Table 3.3-8 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 3.3-1: General operating conditions.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltages	-40°C < TJ < 140 °C, V_{DD} = 3.3 V	1.180	1.216	1.255	V
$t_{S\_vrefint}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
t_{S_vbat}(1)(2)	VBAT sampling time when reading the internal VBAT reference voltage	-	9	-	-	
I_{refbuf}(2)	Reference Buffer consumption for ADC	V_{DDA}=3.3 V	9	13.5	23	µA
ΔV_{REFINT}(2)	Internal reference voltage spread over the temperature range	-40°C < T_J < 140 °C	-	5	15	mV
T_{coeff}(2)	Average temperature coefficient	Average temperature coefficient	-	20	70	ppm/°C
$V_{DDcoeff}$(2)	Average Voltage coefficient	3.0V < V_{DD} < 3.6V	-	10	1370	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	-	25	-	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage	-	-	50	-	
V_{REFINT_DIV3}	3/4 reference voltage	-	-	75	-	

1. The shortest sampling time for the application can be determined by multiple iterations.
2. Guaranteed by design.

Table 3.3-8: Embedded reference voltage

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C, V_{DDA} = 3.3 V	1FF1E860 - 1FF1E861

Table 3.3-9: Internal reference voltage calibration values

3.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in Figure 3.1-4: Current consumption measurement scheme.

All the run-mode current consumption measurements given in this section are performed with a CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.

- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{ACLK} frequency (refer to the table "Number of wait states according to CPU clock ($f_{rcc\_c\_ck}$) frequency and V_{CORE} range" available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU1 frequency divided by 2 and the APB clock frequency is AHB clock frequency divided by 2.

The parameters given in the below tables are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 3.3-1: General operating conditions.

Symbol	Parameter	Conditions		Arm Cortex-M7 f_{CPU1} (MHz)	Arm Cortex-M4 f_{CPU2} (MHz)	Typ	Max(3)					Unit
							Tj= 25 °C	Tj= 85 °C	Tj= 105°C	Tj= 125°C	Tj= 140°C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0	480	240	179	272	387	498			mA
				400	200	151	-	-	-			
			VOS1	400	200	132	181	292	382	502		
			VOS2	300	150	91	122	211	281	377		
			VOS3	200	100	56	79	150	206	284	382	
		All peripherals enabled	VOS0	480	240	247	374	462	571			
				400	200	208	-	-	-			
			VOS1	400	200	181	232	337	422	541		
			VOS2	300	150	126	163	248	318	414		
			VOS3	200	100	78	104	173	229	307	406	

1. Data are in DTCM for best computation performance, the cache has no influence on consumption in this case.
2. The grayed cells correspond to the forbidden configurations.
3. Guaranteed by characterization results, unless otherwise specified.

Table 3.3-10: Typical and maximum current consumption in Run mode, code with data processing running from ITCM for Cortex-M7 core, and Flash memory for Cortex-M4(ART accelerator ON), LDO regulator ON(1)(2)

Symbol	Parameter	Conditions		Arm Cortex-M7 f_{CPU1} (MHz)	Arm Cortex-M4 f_{CPU2} (MHz)	Typ	Max					Unit
							Tj= 25 °C	Tj= 85 °C	Tj= 105°C	Tj= 125°C	Tj= 140°C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS1	400	200	58.3	79.0	129.0	175.1	236.0	-	mA
			VOS2	300	150	37.0	50.2	84.7	115.6	161.1	218.4	
			VOS3	200	100	21.5	29.9	56.1	77.1	107.6	152.3	
		All peripherals enabled	VOS1	400	200	78.1	100.1	148.9	193.4	254.3	-	
			VOS2	300	150	51.2	65.5	100.8	130.9	176.9	235.5	
			VOS3	200	100	29.5	39.4	63.9	86.7	116.3	161.9	

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors.

Table 3.3-11: Typical and maximum current consumption in Run mode, code with data processing running from ITCM for Arm Cortex-M7 and Flash memory for Arm Cortex-M4, ART accelerator ON, SMPS regulator(1)

Symbol	Parameter	Conditions		Arm Cortex -M7 f_{CPU1} (MHz)	Arm Cortex-M4 f_{CPU2} (MHz)	Typ	Max(2)					Unit
							Tj= 25 °C	Tj= 85 °C	Tj= 105°C	Tj= 125°C	Tj= 140°C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0	480	240	173	268	385	496			mA
				400	200	147	-	-	-			
			VOS1	400	200	128	175	288	379	499		
			VOS2	300	150	88	120	209	279	374		
			VOS3	200	100	55	77	149	205	283	381	
		All peripherals enabled	VOS0	480	240	242	368	459	569			
			VOS1	400	200	178	229 (3)	334	419(3)	537		
			VOS2	300	150	123	161	246	316	412		
			VOS3	200	100	77	102	172	228	306	405	

1. The grayed cells correspond to the forbidden configurations.
2. Guaranteed by characterization results, unless otherwise specified.
3. Guaranteed by tests in production.

Table 3.3-12: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, both cores running, cache ON, ART accelerator ON, LDO regulator ON(1)

Symbol	Parameter	Conditions		Arm Cortex -M7 f_{CPU1} (MHz)	Arm Cortex -M4 f_{CPU2} (MHz)	Typ	Max(2)					Unit
							Tj= 25 °C	Tj= 85 °C	Tj= 105°C	Tj= 125°C	Tj= 140°C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0	480	240	109	191	330	444			mA
			VOS1	400	200	96	149	256	347	468		
			VOS2	300	150	67	95	187	257	354		
			VOS3	200	100	43	62	136	192	270	368	
		All peripherals enabled	VOS0	480	240	178	291	403	517			
			VOS1	400	200	147	224	310	401	523		
			VOS2	300	150	103	136	224	295	392		
			VOS3	200	100	64	87	159	215	293	392	

1. The grayed cells correspond to the forbidden configurations.
2. Guaranteed by characterization results, unless otherwise specified.

Table 3.3-13: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, both cores running, cache OFF, ART accelerator OFF, LDO regulator ON(1)

Symbol	Parameter	Conditions		f_{CPU1} (MHz)	Typ	Max(3)					Unit
						Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	Tj=140 °C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0	480	148	226	307	390			mA
				400	125	-	-	-			
			VOS1	400	110	168	230	296	384		
				300	84	-	-	-	-		
			VOS2	300	76	114	170	224	297		
				216	56	88	152	205	278		
				200	53	-	-	-	-		
			VOS3	200	47	71	121	164	223	295	
				180	43	64	116	159	218	291	
				168	40	63	115	158	217	290	
				144	35	55	109	153	212	284	
				60	16	36	92	135	194	267	
				25	12	24	83	126	185	257	
		All peripherals enabled	VOS0	480	226	222	439	550			
				400	190	-	-	-			
			VOS1	400	167	222	327	416	536		
				300	135	-	-	-	-		
			VOS2	300	122	160	248	320	419		
				200	85	-	-	-	-		
			VOS3	200	76	103	174	233	313	413	

1. Data are in DTCM for best computation performance, the cache has no influence on consumption in this case.
2. The grayed cells correspond to the forbidden configurations.
3. Guaranteed by characterization results, unless otherwise specified.

Table 3.3-14: Typical and maximum current consumption in Run mode, code with data processing running from ITCM, only Arm Cortex-M7 running, LDO regulator ON(1)(2)

Symbol	Parameter	Conditions		f_{CPU1} (MHz)	Typ	Max					Unit
						Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	Tj=140 °C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS1	400	48.6	73.3	100.4	132.4	176.0		mA
			VOS2	300	31.3	46.3	68.3	90.0	122.2	164.5	
			VOS3	200	18.0	26.9	45.3	60.6	82.4	111.7	
		All peripherals enabled	VOS1	400	72.9	95.8	144.5	190.7	252.0		
			VOS2	300	49.6	64.3	99.6	131.7	179.1	238.2	
			VOS3	200	28.8	38.5	64.3	88.3	118.6	164.7	

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors
2. The grayed cells correspond to the forbidden configurations.

Table 3.3-15: Typical and maximum current consumption in Run mode, code with data processing running from ITCM, only Arm Cortex-M7 running, SMPS regulator(1)(2)

Symbol	Parameter	Conditions		f_{CPU1} (MHz)	Typ	Max(2)					Unit
						Tj=25° C	Tj=85° C	Tj=105 °C	Tj=125 °C	Tj=140 °C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0	480	110	222	304	388			mA
				400	91	-	-	-			
			VOS1	400	80	162	228	294	381		
				300	61.5	-	-	-	-		
			VOS2	300	55	111	168	222	294		
				200	38.5	-	-	-	-		
			VOS3	200	34.5	69	120	163	222	294	
		All peripherals enabled	VOS0	480	220	342	436	546			
				400	195	-	-	-			
			VOS1	400	175	264	336	424	544		
				300	135	-	-	-	-		
			VOS2	300	120	180	246	318	418		
				200	83	-	-	-	-		
			VOS3	200	75	114	173	232	312	412	

1. The grayed cells correspond to the forbidden configurations.
2. Guaranteed by characterization results, unless otherwise specified.

Table 3.3-16: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, only Arm Cortex-M7 running, cache ON, LDO regulator ON(1)

Symbol	Parameter	Conditions		f_{CPU1} (MHz)	Typ	Max(2)					Unit
						Tj=25° C	Tj=85° C	Tj=105 °C	Tj=125 °C	Tj=140 °C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0	480	87	157	259	342			mA
			VOS1	400	73	123	201	267	355		
			VOS2	300	52	85	150	204	277		
			VOS3	200	34	54	109	152	212	284	
		All peripherals enabled	VOS0	480	168	276	390	504			
			VOS1	400	135	224	308	397	519		
			VOS2	300	100	154	228	301	401		
			VOS3	200	70	103	167	226	307	407	

1. The grayed cells correspond to the forbidden configurations.
2. Guaranteed by characterization results, unless otherwise specified.

Table 3.3-17: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, only Arm Cortex-M7 running, cache OFF, LDO regulator ON(1)

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ	Max(1)					Unit
						Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	Tj=140 °C	
I_{DD}	Supply current in batch acquisition mode	D1 Standby, D2 Standby, D3 Run	VOS3	64	2.7	4.7	12.9	19.0	27.5	37.8	mA
				8	1.1	-	-	-	-	-	
		D1 Stop, D2 Stop, D3 Run	VOS3	64	5.4	18.4	83.7	132.6	202.4	289.3	
				8	3.8	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

Table 3.3-18: Typical and maximum current consumption batch acquisition mode, LDO regulator ON

Symbol	Parameter	Conditions		f_{CPU2} (MHz)	Typ	Max(2)					Unit
						Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	Tj=140 °C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0	240	121	203	339	453			mA
				200	90	-	-	-			
			VOS1	200	79	123	234	323	444		
				150	61	-	-	-	-		
			VOS2	150	56	85	178	250	350		
			VOS3	100	35	59	131	189	269	369	
		All peripherals enabled	VOS0	240	190	303	412	525			
				200	146	-	-	-			
			VOS1	200	129	195	287	376	499		
			VOS2	150	90	134	214	287	386		
			VOS3	100	61	100	158	216	297	398	

1. The grayed cells correspond to the forbidden configurations.
2. Guaranteed by characterization results, unless otherwise specified.

Table 3.3-19: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, only Arm Cortex-M4 running, ART accelerator ON, LDO regulator ON(1)

Symbol	Parameter	Conditions		Typ	Max					Unit
					Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	Tj=140 °C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS1	35.3	54.3	102.1	144.4	203.5		mA
			VOS2	23.3	35.0	70.6	99.2	145.8	207.0	
			VOS3	13.6	22.3	49.0	69.8	101.9	147.1	
		All peripherals enabled	VOS1	57.0	84.1	126.8	172.3	234.6		
			VOS2	36.6	54.5	84.9	118.1	165.0	223.7	
			VOS3	23.1	37.4	58.4	79.8	112.5	158.7	

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors
2. The grayed cells correspond to the forbidden configurations.

Table 3.3-20: Typical and maximum current consumption in Run mode, code with data processing running from Flash bank 2, only Arm Cortex-M4 running, ART accelerator ON, SMPS regulator(1)(2)

Symbol	Parameter	Conditions		Typ	Max(3)					Unit
					Tj=25°C	Tj=85°C	Tj=105 °C	Tj=125 °C	Tj=140 °C	
$I_{DD\ (Stop)}$	D1 Stop, D2 Stop, D3 Stop	Flash memory OFF, no IWDG	SVOS5	1.27	6.3	42.5	72.0			mA
			SVOS4	1.96	9.4	57.4	94.6			
			SVOS3	2.78	13.8(4)	75.9	121.3(4)	183.8	264.9	
		Flash memory ON, no IWDG	SVOS5	1.27	6.3	42.5	72.0			
			SVOS4	2.25	9.8	57.9	95.2			
			SVOS3	3.07	14.1	76.4	122.0	184.8	266.5	
	D1 Stop, D2 Standby, D3 Stop	Flash memory OFF, no IWDG	SVOS5	0.91	4.6	30.4	51.2			
			SVOS4	1.42	6.8	41.1	67.3			
			SVOS3	2.02	10.0	54.4	86.6	130.0	186.1	
		Flash memory ON, no IWDG	SVOS5	0.91	4.6	30.4	51.2			
			SVOS4	1.70	7.2	41.5	67.9			
			SVOS3	2.31	10.3	54.9	87.1	130.8	187.2	
	D1Standby, D2 Stop, D3 Stop	Flash memory OFF, no IWDG	SVOS5	0.49	2.4	16.5	28.0			
			SVOS4	0.76	3.6	22.2	36.6			
			SVOS3	1.10	5.3	29.3	46.9	71.2	102.2	
	D1Standby, D2Standby, D3 Stop	Flash memory OFF, no IWDG	SVOS5	0.15	0.7(4)	4.3	7.3(4)			
			SVOS4	0.22	1.0	5.8	9.6			
			SVOS3	0.35	1.5(4)	7.8	12.3(4)	18.6	26.6	

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors
2. The grayed cells correspond to the forbidden configurations.
3. Guaranteed by characterization results, unless otherwise specified.
4. Guaranteed by tests in production.

Table 3.3-21: Typical and maximum current consumption in Stop, LDO regulator ON(1)(2)

Symbol	Parameter	Conditions		Typ	Max					Unit
					Tj=25°C	Tj=85°C	Tj=105 °C	Tj=125 °C	Tj=140 °C	
$I_{DD\ (Stop)}$	D1 Stop, D2 Stop, D3 Stop	FlashOFF, no IWDG	SVOS5	0.36	1.73	11.91	21.53	-	-	mA
			SVOS4	0.63	3.05	19.57	33.51	-	-	
			SVOS3	1.00	4.98	29.11	47.13	68.76	100.34	
		FlashON, no IWDG	SVOS5	0.36	1.73	11.91	21.53	-	-	
			SVOS4	0.73	3.18	19.74	33.72	-	-	
			SVOS3	1.11	5.09	29.31	47.40	69.14	100.95	
	D1 Stop, D2 Standby, D3 Stop	FlashOFF, no IWDG	SVOS5	0.25	1.24	8.21	14.00	-	-	
			SVOS4	0.46	2.21	14.01	22.94	-	-	
			SVOS3	0.73	3.57	19.62	32.80	49.24	68.77	
		FlashON, no IWDG	SVOS5	0.25	1.24	8.21	14.00	-	-	
			SVOS4	0.55	2.34	14.15	23.15	-	-	
			SVOS3	0.83	3.67	19.81	32.99	49.55	69.18	
	D1 Standby, D2 Stop, D3 Stop	FlashOFF, no IWDG	SVOS5	0.15	0.67	4.51	7.85	-	-	
			SVOS4	0.26	1.17	7.21	12.32	-	-	
			SVOS3	0.40	1.90	10.57	17.12	26.97	39.20	
	D1 Standby, D2 Standby, D3 Stop	FlashON, no IWDG	SVOS5	0.06	0.20	1.18	2.05	-	-	
			SVOS4	0.08	0.33	1.90	3.11	-	-	
			SVOS3	0.13	0.54	2.80	4.47	6.77	9.58	

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors.

Table 3.3-22: Typical and maximum current consumption in Stop, SMPS regulator(1)

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ	Max(3)					Unit
						Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	Tj=140 °C	
$I_{DD\ (Sleep)}$	Supply current in Sleepmode	All peripherals disabled	VOS0	480	50.7	96.3	253.4	366.1			mA
				400	43.4	87.8	245.5	357.9			
			VOS1	400	35.3	66.5	181.3	265.8	379.6		
				300	27.9	-	-	-	-		
			VOS2	300	24.6	47.3	139.1	207.3	300.4		
				200	18.8	-	-	-	-		
			VOS3	200	16.5	33.6	106.4	160.9	236.1	330.3	
		All peripherals enabled	VOS0	480	136.0	194.7	348.5	464.4			
				400	115.0	169.0	325.9	441.7			
			VOS1	400	97.7	138.2	251.3	338.4	456.4		
				300	74.9	-	-	-	-		
			VOS2	300	67.3	95.8	187.6	257.9	354.1		
				200	52.8	-	-	-	-		
			VOS3	200	47.1	69.3	141.4	197.7	275.1	372.8	

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors
2. The grayed cells correspond to the forbidden configurations.
3. Guaranteed by characterization results, unless otherwise specified.

Table 3.3-23: Typical and maximum current consumption in Sleep mode, LDO regulator ON(1)(2)

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ	Max					Unit
						Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	Tj=140 °C	
I_{DD} (Sleep)	Supply current in Sleep mode	All peripherals disabled	VOS1	400	15.93	29.69	79.01	118.72	173.80		mA
				300	12.58	-	-	-	-		
			VOS2	300	10.21	19.63	56.46	82.14	123.46	177.95	
				200	7.89	-	-	-	-	-	
			VOS3	200	6.50	12.98	39.73	59.35	87.10	125.00	
		All peripherals Enabled	VOS1	400	42.65	59.62	110.88	153.00	211.65	-	
			VOS2	300	27.70	38.94	75.26	102.22	147.38	208.16	
			VOS3	200	17.95	26.14	52.75	72.95	104.09	148.48	

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors.
2. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors
3. The grayed cells correspond to the forbidden configurations.

Table 3.3-24: Typical and maximum current consumption in Sleep mode, SMPS regulator(1)(2)(3)

Symbol	Parameter	Conditions		Typ				Max(1)					Unit
								3 V					
		Backup SRAM	RTC and LSE	1.62 V	2.4 V	3 V	3.3 V	Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	Tj=140 °C	
I_{DD} (Standby)	Supply current in Standby mode	OFF	OFF	1,92	1,95	2,06	2,16	4	18	40	90	140	µA
		ON	OFF	3,33	3,44	3,6	3,79	8.2	47	83	141	230	
		OFF	ON	2,43	2,57	2,77	2,95	-	-	-	-	-	
		ON	ON	3,82	4,05	4,31	4,55	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

Table 3.3-25: Typical and maximum current consumption in Standby

Symbol	Parameter	Conditions		Typ				Max(1)					Unit
								3 V					
		Backup SRAM	RTC and LSE	1.2 V	2 V	3 V	3.4 V	Tj=25 °C	Tj=85 °C	Tj=105 °C	Tj=125 °C	Tj=140 °C	
I_{DD} (VBAT)	Supply current in V_{BAT} mode	OFF	OFF	0,02	0,02	0,03	0,05	0,5	4,1	10	24	47	µA
		ON	OFF	1,33	1,45	1,58	1,7	4,4	22	48	87	132	
		OFF	ON	0,46	0,57	0,75	0,87	-	-	-	-	-	
		ON	ON	1,77	2	2,3	2,5	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

Table 3.3-26: Typical and maximum current consumption in V_{BAT} mode

Typical SMPS efficiency versus load current and temperature

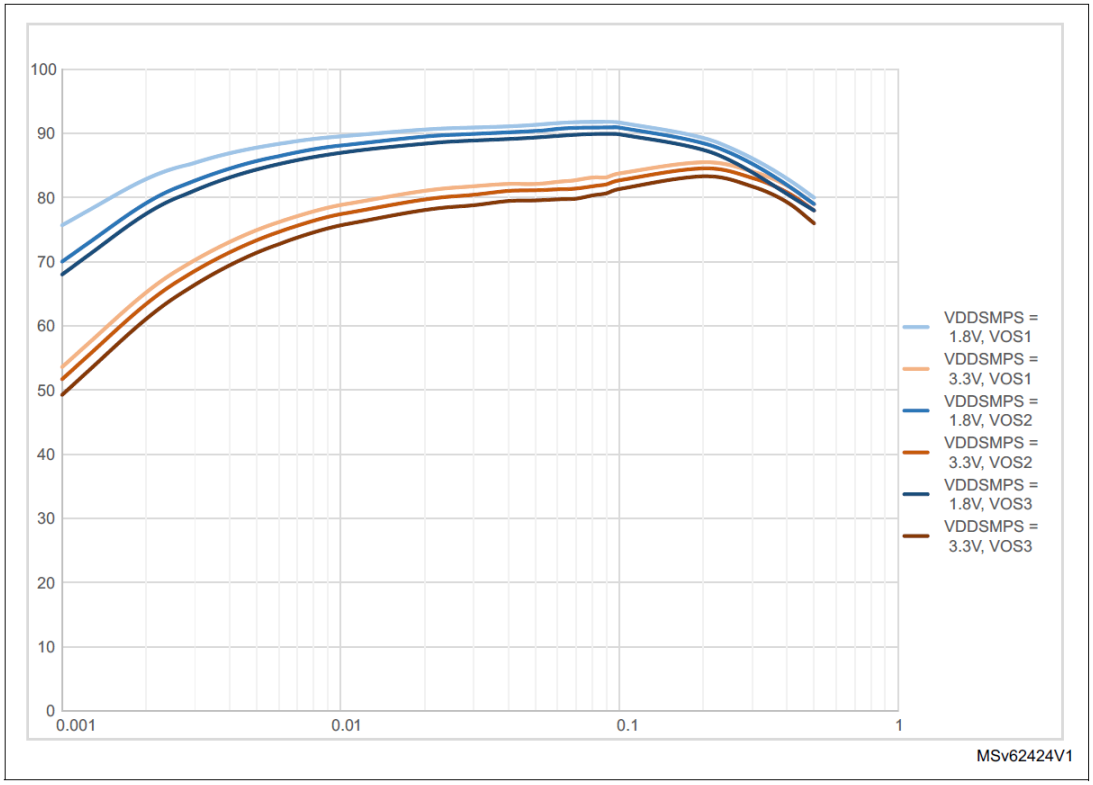


Figure 3.3-3: Typical SMPS efficiency (%) vs load current (A) in Run mode at T_J = 30 °C

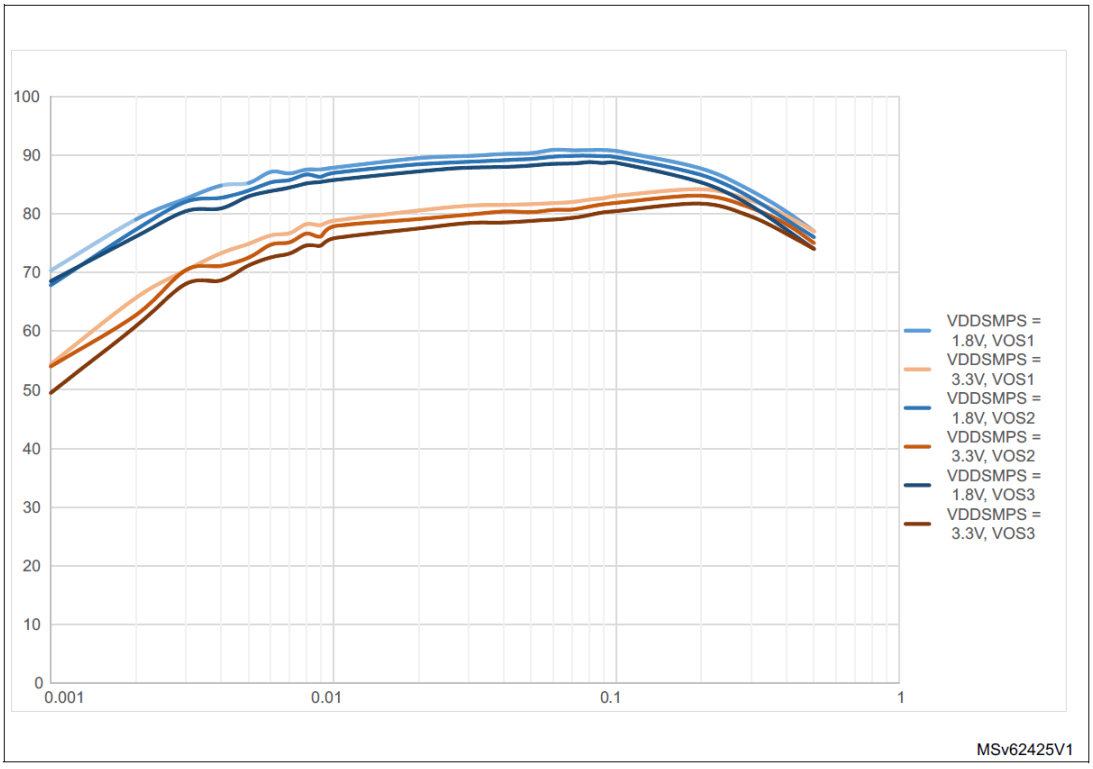


Figure 3.3-4: Typical SMPS efficiency (%) vs load current (A) in Run mode at $T_J = T_{Jmax}$

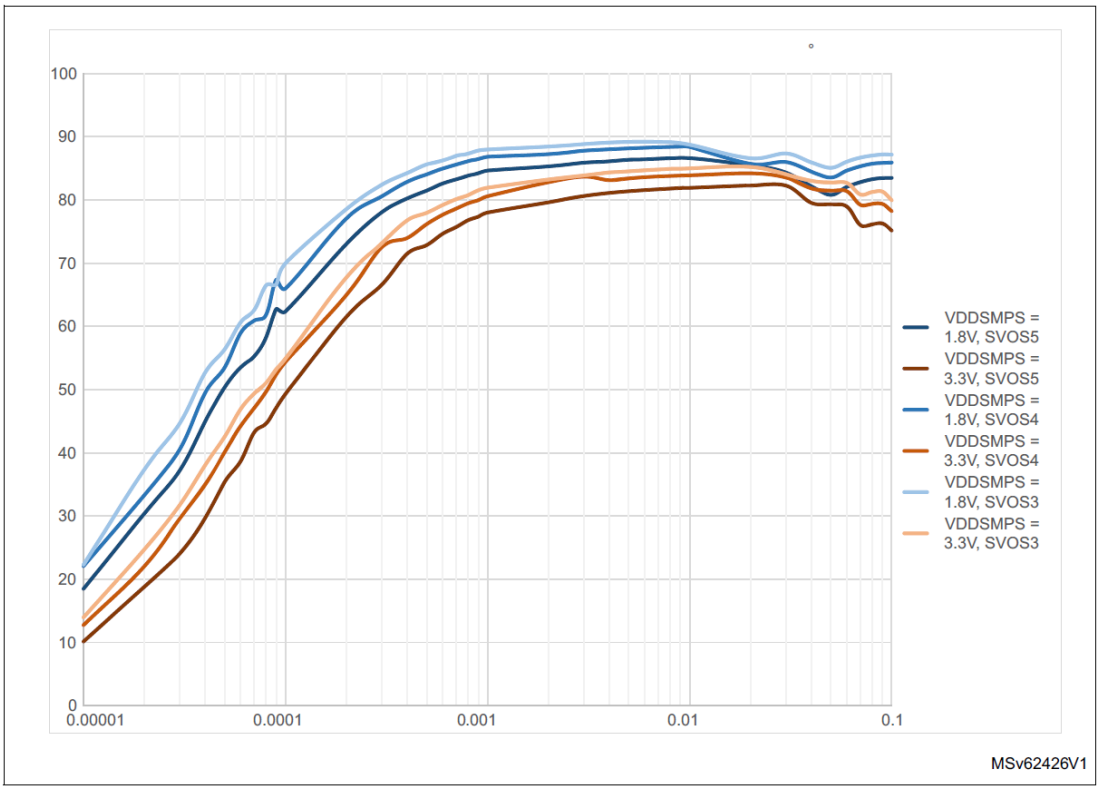


Figure 3.3-5: Typical SMPS efficiency (%) vs load current (A) in low-power mode at T_J = 30 °C

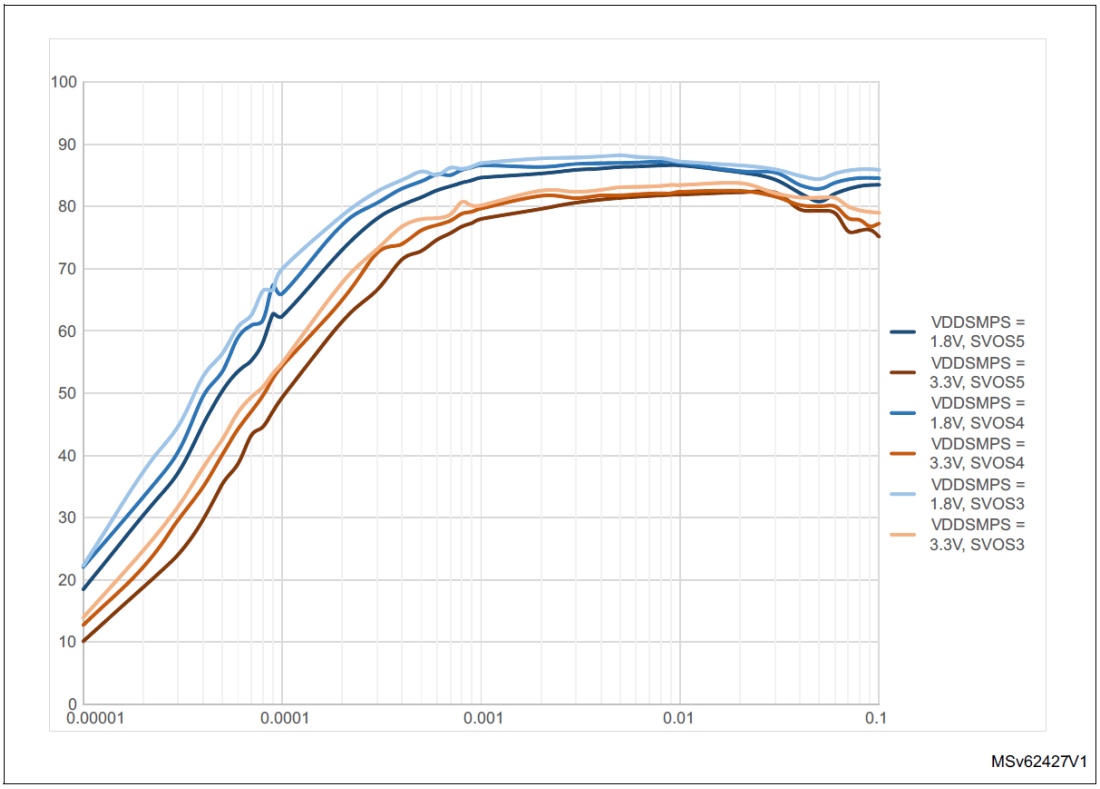


Figure 3.3-6: Typical SMPS efficiency (%) vs load current (A) in low-power mode at $T_J = T_{Jmax}$

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in Table 3.3-47: I/O static characteristics.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see Table 3.3-27: Peripheral current consumption in Run mode), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
V_{DDx} is the MCU supply voltage
f_{SW} is the I/O switching frequency
C_L is the total capacitance seen by the I/O pin: C = CINT+ CEXT

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The I/O compensation cell is enabled.
- $f_{rcc\_c\_ck}$ is the CPU clock. $f_{PCLK} = f_{rcc\_c\_ck}/4$, and $f_{HCLK} = f_{rcc\_c\_ck}/2$.

  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - $f_{rcc\_c\_ck}$ = 480 MHz (Scale 0), $f_{rcc\_c\_ck}$ = 400 MHz (Scale 1), $f_{rcc\_c\_ck}$ = 300 MHz (Scale 2), $f_{rcc\_c\_ck}$ = 200 MHz (Scale 3)
- The ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Bus	Peripheral	VOS0	VOS1	VOS2	VOS3	Unit
AHB3	MDMA	4.6	3.8	3.4	3.2	µA/MHz
	DMA2D	2.9	2.4	2.1	1.9	
	JPGDEC	4.1	3.7	3.4	3.1	
	FLASH	17.0	15.0	14.0	12.0	
	FMC registers	0.9	1.1	0.9	0.8	
	FMC kernel	7.0	6.1	5.6	5.0	
	QUADSPI registers	1.5	1.5	1.4	1.3	
	QSPI kernel	1.0	0.9	0.8	0.7	
	SDMMC1 registers	8.2	7.2	6.7	6.0	
	SDMMC1 kernel	1.3	1.2	0.9	0.9	
	DTCM1	7.9	6.8	6.0	5.3	
	DTCM2	8.3	7.2	6.4	5.7	
	ITCM	7.0	6.3	5.6	5.1	
	D1SRAM1	13.0	11.0	9.9	8.7	
	AHB3 bridge	35.0	32.0	29.0	26.0	
	Total AHB3	**120**	**106**	**96**	**86**	
AHB1	DMA1	54.0	48.0	41.0	37.0	
	DMA2	55.0	49.0	42.0	37.0	
	ADC12 registers	4.5	4.1	3.7	3.3	
	ADC12 kernel	1.0	0.7	0.4	0.6	
	ART accelerator	4.1	3.7	3.2	2.9	
	ETH1MAC	17.0	15.0	14.0	12.0	
	ETH1TX	0.1	0.1	0.1	0.1	
	ETH1RX	0.1	0.1	0.1	0.1	
	USB1 OTG registers	23.0	21.0	19.0	17.0	
	USB1 OTG kernel	8.2	0.5	8.3	8.2	
	USB1 ULPI	0.1	0.1	0.1	0.1	
	USB2 OTG registers	21.0	19.0	17.0	15.0	
	USB2 OTG kernel	8.5	0.4	8.6	8.3	
	USB2 ULPI	23.0	19.0	20.0	19.0	
	AHB1 bridge	0.1	0.1	0.1	0.1	
	Total AHB1	**220**	**181**	**178**	**161**	

Table 3.3-27: Peripheral current consumption in Run mode

Bus	Peripheral	VOS0	VOS1	VOS2	VOS3	Unit
AHB2	DCMI	2.1	1.9	1.8	1.6	µA/MHz
	CRYPT	0.1	0.1	0.1	0.1	
	HASH	0.1	0.1	0.1	0.1	
	RNG registers	1.7	2.0	1.3	1.2	
	RNG kernel	11.0	0.1	9.7	9.4	
	SDMMC2 registers	47.0	41.0	37.0	34.0	
	SDMMC2 kernel	1.7	1.2	1.1	1.0	
	D2SRAM1	5.7	4.9	4.4	3.9	
	D2SRAM2	5.2	4.5	4.0	3.5	
	D2SRAM3	4.1	3.6	3.2	2.8	
	AHB2 bridge	0.1	0.1	0.1	0.1	
	Total AHB2	**79**	**60**	**63**	**58**	
AHB4	GPIOA	1.5	1.3	1.3	1.1	
	GPIOB	1.2	1.0	1.0	0.9	
	GPIOC	0.8	0.7	0.7	0.6	
	GPIOD	1.1	1.0	1.0	0.9	
	GPIOE	0.7	0.7	0.7	0.6	
	GPIOF	0.8	0.8	0.7	0.6	
	GPIOG	0.9	0.8	0.8	0.7	
	GPIOH	1.1	1.0	1.0	0.9	
	GPIOI	0.9	0.9	0.8	0.7	
	GPIOJ	0.8	0.8	0.7	0.7	
	GPIOK	0.7	0.8	0.7	0.6	
	CRC	0.4	0.5	0.4	0.3	
	BDMA	6.6	5.9	5.3	4.8	
	ADC3 registers	1.7	1.5	1.2	1.2	
	ADC3 kernel	0.4	0.3	0.5	0.2	
	BKPRAM	2.3	1.9	1.7	1.5	
	AHB4 bridge	0.1	0.1	0.1	0.1	
	Total AHB4	**22**	**20**	**19**	**16**	
APB3	WWDG1	0.7	0.5	0.5	0.2	µA/MHz
	LCD-TFT	81.0	36.0	33.0	30.0	
	APB3 bridge	0.3	0.2	0.1	0.1	
	Total APB3	**87**	**41**	**38**	**34**	

Table 3.3-27: Peripheral current consumption in Run mode (continued)

Bus	Peripheral	VOS0	VOS1	VOS2	VOS3	Unit
APB1	TIM2	7.7	3.6	3.3	3.0	µA/MHz
	TIM3	6.7	3.2	3.0	2.7	
	TIM4	6.3	3.1	2.8	2.5	
	TIM5	7.4	3.5	3.2	2.8	
	TIM6	1.4	0.7	0.8	0.6	
	TIM7	1.4	0.7	0.7	0.6	
	TIM12	3.2	1.5	1.5	1.3	
	TIM13	2.3	1.1	1.1	0.9	
	TIM14	2.1	1.1	1.1	0.9	
	LPTIM1 registers	0.7	0.5	0.8	0.7	
	LPTIM1 kernel	2.4	2.3	1.9	1.7	
	WWDG2	0.6	0.5	0.5	0.4	
	SPI2 registers	2.0	1.8	1.7	1.4	
	SPI2 kernel	0.8	0.6	0.5	0.6	
	SPI3 registers	1.8	1.6	1.6	1.3	
	SPI3 kernel	0.7	0.9	0.7	0.7	
	SPDIFRX1 registers	0.5	0.7	0.7	0.6	
	SPDIFRX1 kernel	3.5	2.8	2.4	2.2	
	USART2 registers	1.9	1.7	1.4	1.3	
	USART2 kernel	4.3	3.9	3.6	3.2	
	USART3 registers	1.9	1.7	1.4	1.3	
	USART3 kernel	4.4	3.9	3.5	3.2	
	UART4 registers	1.7	1.5	1.4	1.4	
	UART4 kernel	3.9	3.4	3.1	2.8	
	UART5 registers	1.6	1.4	1.4	1.3	
	UART5 kernel	3.8	3.4	3.0	2.7	
	I2C1 registers	1.1	0.8	0.9	0.8	
	I2C1 kernel	2.5	2.3	2.0	1.9	
	I2C2 registers	1.0	0.8	0.9	0.8	
	I2C2 kernel	2.3	2.2	1.9	1.7	
	I2C3 registers	0.8	1.0	0.8	0.8	
	I2C3 kernel	2.4	1.9	1.8	1.6	
	HDMI-CEC registers	0.7	0.5	0.6	0.5	
	HDMI-CEC kernel	0.1	0.1	3.2	0.1	
	DAC12	3.6	1.3	1.2	1.0	
	USART7 registers	1.8	1.8	1.6	1.4	
	USART7 kernel	4.0	3.3	3.0	2.8	

Table 3.3-27: Peripheral current consumption in Run mode (continued)

Bus	Peripheral	VOS0	VOS1	VOS2	VOS3	Unit
APB1 (continued)	USART8 registers	2.0	1.6	1.6	1.4	µA/MHz
	USART8 kernel	3.9	3.4	3.1	2.8	
	CRS	6.4	5.5	5.0	4.5	
	SWPMI registers	2.7	2.4	2.3	1.9	
	SWPMI kernel	0.1	0.1	0.1	0.1	
	OPAMP	0.2	0.3	0.3	0.2	
	MDIO	3.3	2.9	2.6	2.3	
	FDCAN registers	19.0	17.0	15.0	13.0	
	FDCAN kernel	9.1	7.9	6.9	6.4	
	APB1 bridge	0.1	0.1	0.1	0.1	
	Total APB1	**142**	**108**	**102**	**88**	
APB2	TIM1	11.0	5.0	4.5	4.0	
	TIM8	10.0	4.7	4.3	3.8	
	USART1 registers	3.6	2.5	2.7	2.9	
	USART1 kernel	0.1	0.1	0.1	0.1	
	USART6 registers	4.5	3.0	3.1	3.4	
	USART6 kernel	0.1	0.1	0.1	0.1	
	SPI1 registers	2.0	1.7	1.6	1.4	
	SPI1 kernel	0.9	0.8	0.7	0.6	
	SPI4 registers	2.1	1.7	1.6	1.5	
	SPI4 kernel	0.6	0.5	0.5	0.3	
	TIM15	5.5	2.5	2.3	2.1	
	TIM16	4.1	2.0	1.8	1.7	
	TIM17	4.1	1.9	1.8	1.6	
	SPI5 registers	2.0	1.8	1.6	1.3	
	SPI5 kernel	0.5	0.4	0.4	0.5	
	SAI1 registers	1.3	1.1	1.1	1.0	
	SAI1 kernel	1.4	1.1	1.0	0.8	
	SAI2 registers	1.5	1.3	1.2	1.0	
	SAI2 kernel	1.1	1.0	0.9	0.9	
	SAI3 registers	1.6	1.3	1.1	1.0	
	SAI3 kernel	1.1	1.2	1.1	0.9	
	SAI1 kernel	1.4	1.1	1.0	0.8	

Table 3.3-27: Peripheral current consumption in Run mode (continued)

Bus	Peripheral	VOS0	VOS1	VOS2	VOS3	Unit
APB2 (continued)	DFSDM1 registers	6.5	5.8	5.2	4.7	µA/MHz
	DFSDM1 kernel	0.3	0.2	0.2	0.4	
	HRTIM	84.0	39.0	35.0	32.0	
	APB2 bridge	0.2	0.1	0.1	0.2	
	Total APB2	**150**	**81**	**74**	**68**	
APB4	SYSCFG	0.9	1.0	0.7	0.8	
	LPUART1 registers	1.1	1.3	1.0	0.8	
	LPUART1 kernel	2.9	2.2	2.2	2.1	
	SPI6 registers	1.8	1.6	1.4	1.3	
	SPI6 kernel	0.4	0.4	0.5	0.3	
	I2C4 registers	0.9	0.7	0.7	0.4	
	I2C4 kernel	2.2	2.1	1.9	1.8	
	LPTIM2 registers	0.8	0.6	0.7	0.5	
	LPTIM2 kernel	2.3	2.1	1.8	1.4	
	LPTIM3 registers	0.7	0.7	0.7	0.4	
	LPTIM3 kernel	2.1	1.7	1.6	1.5	
	LPTIM4 registers	0.8	0.4	0.6	0.4	
	LPTIM4 kernel	2.2	2.0	1.7	1.5	
	LPTIM5 registers	0.5	0.4	0.6	0.4	
	LPTIM5 kernel	2.0	1.8	1.5	1.2	
	COMP12	0.6	0.4	0.5	0.2	
	VREF	0.4	0.2	0.2	0.1	
	RTC	1.1	0.9	1.0	0.6	
	SAI4 registers	1.7	1.4	1.3	1.0	
	SAI4 kernel	2.0	2.0	1.8	1.6	
	APB4 bridge	0.1	0.1	0.1	0.1	
	Total APB4	**28**	**24.4**	**22.4**	**18.9**	

Table 3.3-27: Peripheral current consumption in Run mode (continued)

3.3.8 Wakeup time from low-power modes

The wakeup times given in Table 3.3-28 are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PC1) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Symbol	Parameter	Conditions	Typ(2)	Max(2)	Unit
$t_{WUSLEEP}$(3)	Wakeup from Sleep	-	9	10	CPU clock cycles
t_{WUSTOP}(3)	Wakeup from Stop	VOS3, HSI, Flash memory in normal mode	4.4	5.6	µs
		VOS3, HSI, Flash memory in low-power mode	12	15	
		VOS4, HSI, Flash memory in normal mode	15	20	
		VOS4, HSI, Flash memory in low-power mode	23	28	
		VOS5, HSI, Flash memory in normal mode	39	71	
		VOS5, HSI, Flash memory in low-power mode	39	47	
		VOS3, CSI, Flash memory in normal mode	30	37	
		VOS3, CSI, Flash memory in low power mode	36	50	
		VOS4, CSI, Flash memory in normal mode	38	48	
		VOS4, CSI, Flash memory in low-power mode	47	61	
		VOS5, CSI, Flash memory in normal mode	68	75	
		VOS5, CSI, Flash memory in low-power mode	68	77	
t_{WUSTOP_KERON}(3)	Wakeup from Stop, clock kept running	VOS3, HSI, Flash memory in normal mode	2.6	3.4	
		VOS3, CSI, Flash memory in normal mode	26	36	
$t_{WUSTDBY}$(3)	Wakeup from Standby mode	-	390	500	

1. The wakeup timings is valid for both CPUs.
2. Guaranteed by characterization results.
3. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

Table 3.3-28: Low-power mode wakeup timings(1)

3.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

The external clock signal has to respect the Table 3.3-47: I/O static characteristics. However, the recommended clock input waveform is shown in Figure 3.3-7.

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	4	25	50	MHz
V_{SW} ($V_{HSEH}-V_{HSEL}$)	OSC_IN amplitude	$0.7V_{DD}$	-	V_{DD}	V
V_{DC}	OSC_IN input voltage	V_{SS}	-	$0.3V_{SS}$	
$t_{W(HSE)}$	OSC_IN high or low time	7	-	-	ns

1. Guaranteed by design.

Table 3.3-29: High-speed external user clock characteristics(1)

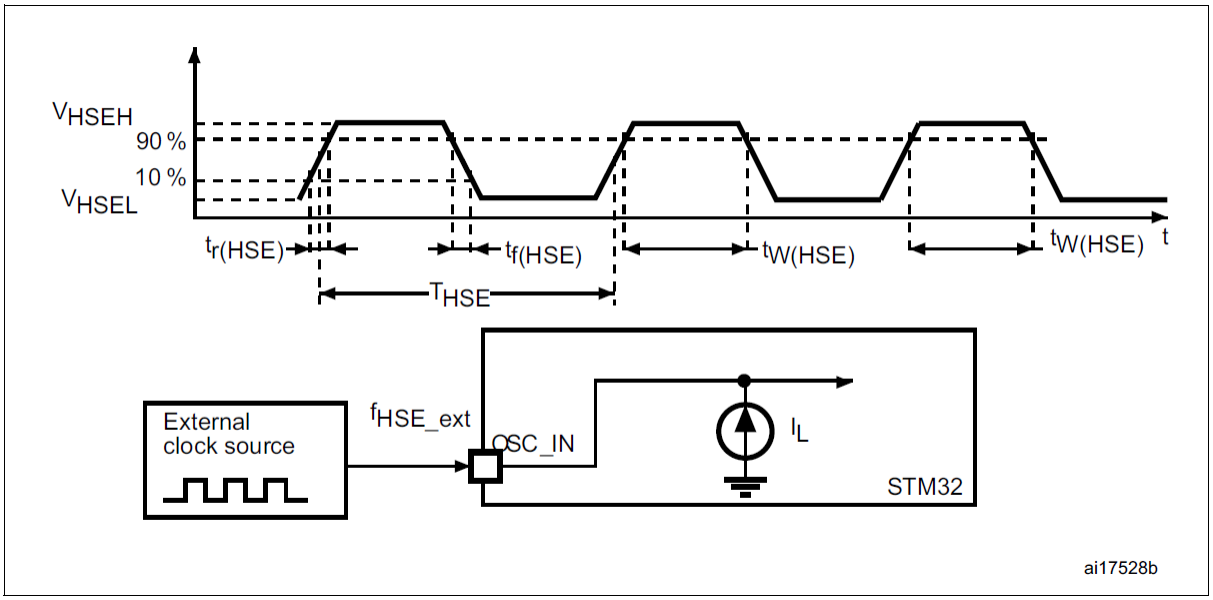


Figure 3.3-7: High-speed external clock source AC timing diagram

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the Table 3.3-47: I/O static characteristics. However, the recommended clock input waveform is shown in Figure 3.3-8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Table 3.3-30: Low-speed external user clock characteristics(1)

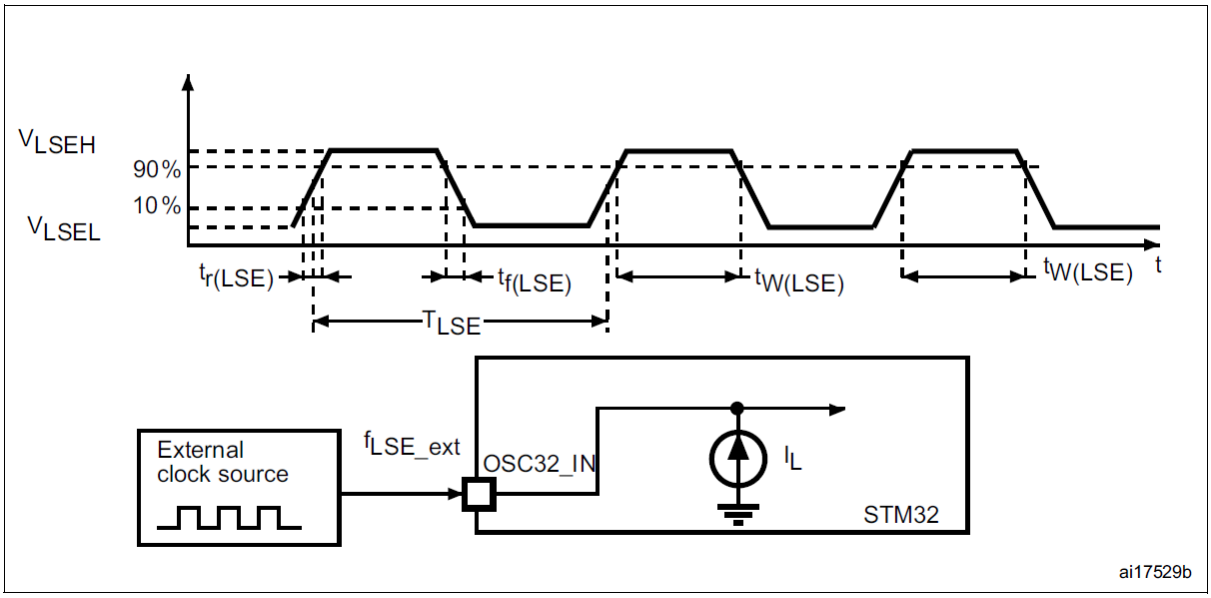


Figure 3.3-8: Low-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

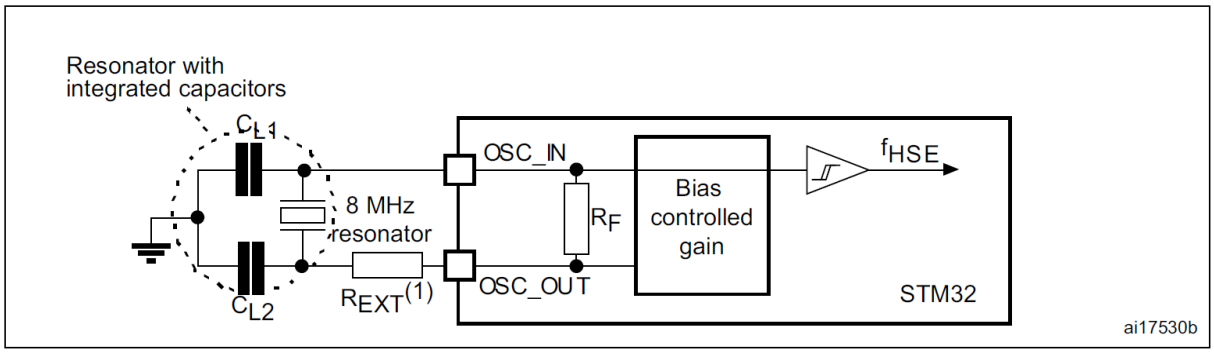
The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 3.3-31. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Operatingconditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	4	-	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	4	mA
		V_{DD}=3 V, Rm=30 Ω C_L=10pF@4MHz	-	0.35	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 8 MHz	-	0.40	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 16 MHz	-	0.45	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 32 MHz	-	0.65	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 48 MHz	-	0.95	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
t_{SU}(4)	Start-up time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the tSU(HSE) startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Table 3.3-31: 4-48 MHz HSE oscillator characteristics(1)

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typical), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see Figure 3.3-9). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. The PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.



1. REXT value depends on the crystal characteristics.

Figure 3.3-9: Typical application with an 8 MHz crystal

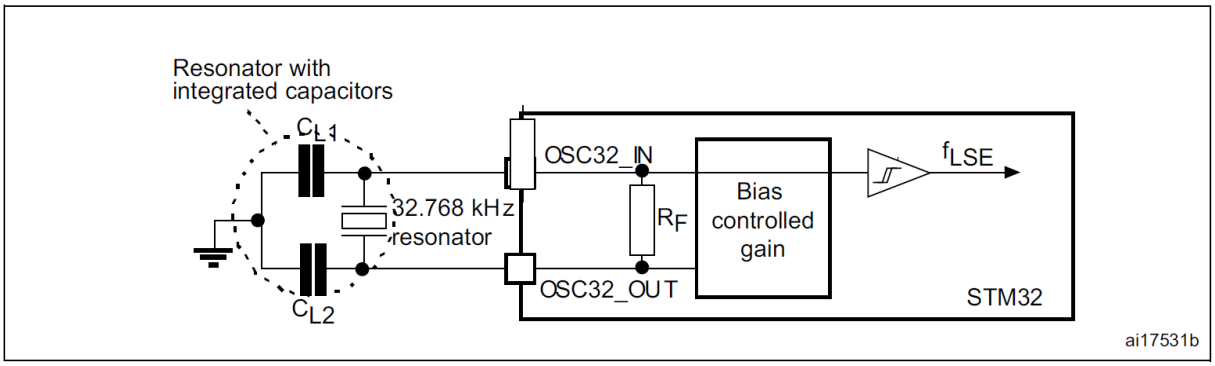
Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 KHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 3.3-32. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	KHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 00, Low drive capability	-	290	-	nA
		LSEDRV[1:0] = 01, Medium Low drive capability	-	390	-	
		LSEDRV[1:0] = 10, Medium high drive capability	-	550	-	
		LSEDRV[1:0] = 11, High drive capability	-	900	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, Medium Low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU}(3)	Startup time	VDD is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers.
3. tSU is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768k Hz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Table 3.3-32: Low-speed external user clock characteristics(1)



1. An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

Figure 3.3-10: Typical application with a 32.768 KHz crystal

3.3.10 Internet clock source characteristics

The parameters given in Table 3.3-33 to Table 3.3-36 are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in Table 3.3-1: General operating conditions.

48 MHz high-speed internal RC oscillator (HSI48)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency	V_{DD}=3.3 V, TJ=30 °C	47.5(1)	48	48.5(1)	MHz
TRIM(2)	USER trimming step	-	-	0.175	-	%
USER TRIM COVERAGE(3)	USER TRIMMING Coverage	± 32 steps	±4.79	±5.60	-	%
DuCy(HSI48)(2)	Duty Cycle	-	45	-	55	%
ACCHSI48_REL(3)(4)	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	T_J=-40 to 125 °C	–4.5	-	3.5	%
		T_J=-40 to 140 °C	–4.5	-	4	
Δ_{VDD}(HSI48)(3)	HSI48 oscillator frequency drift with V_{DD}(5)	V_{DD}=3 to 3.6 V	-	0.025	0.05	%
		V_{DD}=1.62 V to 3.6 V	-	0.05	0.1	
$t_{su(HSI48)}$(2)	HSI48 oscillator start-up time	-	-	2.1	4.0	µs
$I_{DD(HSI48)}$ (2)	HSI48 oscillator power consumption	-	-	350	400	µA
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(6)	-	-	± 0.15	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(6)	-	-	± 0.25	-	ns

1. Guaranteed by test in production.
2. Guaranteed by design.
3. Guaranteed by characterization.
4. ΔfHSI = ACCHSI48_REL + ΔVDD.
5. These values are obtained by using the formula: (Freq(3.6V) - Freq(3.0V)) / Freq(3.0V) or (Freq(3.6V) - Freq(1.62V)) / Freq(1.62V).
6. Jitter measurements are performed without clock source activated in parallel.

Table 3.3-33: HSI48 oscillator characteristics

64 MHz high-speed internal RC oscillator (HSI)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	V_{DD}=3.3 V, T_J=30 °C	63.7(2)	64	64.3(2)	MHz
TRIM	HSI user trimming step	Trimming is not a multiple of 32	-	0.24	0.32	%
		Trimming is 128, 256 and 384	−5.2	−1.8	-	
		Trimming is 64, 192,320 and 448	−1.4	−0.8	-	
		Other trimming are a multiple of 32 (not including multiple of 64 and 128)	−0.6	−0.25	-	
DuCy(HSI)	Duty Cycle	-	45	-	55	%
$\Delta_{VDD\,(HSI)}$	HSI oscillator frequency drift over V_{DD} (reference is 3.3 V)	V_{DD}=1.62 to 3.6 V	−0.12	-	0.03	%
$\Delta_{TEMP\,(HSI)}$	HSI oscillator frequency drift over temperature (reference is 64 MHz)	T_J=-20 to 105 °C	−1(3)	-	1(3)	%
		T_J=−40 to $T_J$max °C	−2(3)	-	1(3)	
t_{su}(HSI)	HSI oscillator start-up time	-	-	1.4	2	µs
t_{stab}(HSI)	HSI oscillator stabilization time	at 1% of target frequency	-	4	8	µs
I_{DD}(HSI)	HSI oscillator power consumption	-	-	300	400	µA

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by test in production.
3. Guaranteed by characterization.

Table 3.3-34: HSI oscillator characteristics(1)

4 MHz low-power internal RC oscillator (CSI)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CSI}	CSI frequency	V_{DD}=3.3 V, T_J=30 °C	3.96(2)	4	4.04(2)	MHz
TRIM	Trimming step	-	-	0.35	-	%
DuCy(CSI)	Duty Cycle	-	45	-	55	%
Δ_{TEMP} (CSI)	CSI oscillator frequency drift over temperature	T_J = 0 to 85 °C	-	−3.7(3)	4.5(3)	%
		T_J = −40 to 140 °C	-	−11(3)	7.5(3)	
D_{VDD} (CSI)	CSI oscillator frequency drift over V_{DD}	V_{DD} = 1.62 to 3.6 V	-	−0.06	0.06	%
$t_{su(CSI)}$	CSI oscillator startup time	-	-	1	2	µs
$t_{stab(CSI)}$	CSI oscillator stabilization time (to reach ±3% of f_{CSI})	-	-	-	4	cycle
$I_{DD(CSI)}$	CSI oscillator power consumption	-	-	23	30	µA

1. Guaranteed by design.
2. Guaranteed by test in production.
3. Guaranteed by characterization.

Table 3.3-35: CSI oscillator characteristics(1)

Low-speed internal (LSI) RC oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD} = 3.3 V, T_J = 25 °C	31.4(1)	32	32.6(1)	KHz
		T_J = –40 to 110 °C, V_{DD} = 1.62 to 3.6 V	29.76(2)	-	33.6(2)	
		T_J = –40 to 125 °C, V_{DD} = 1.62 to 3.6 V	29.4	-	33.6	
		T_J = –40 to 140 °C, V_{DD} = 1.62 to 3.6 V	29.4	-	33.6	
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	80	130	µs
$t_{stab(LSI)}$(3)	LSI oscillator stabilization time (5% of final value)	-	-	120	170	
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	-	130	280	nA

1. Guaranteed by test in production.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Table 3.3-36: LSI oscillator characteristics

3.3.11 PLL characteristics

The parameters given in Table 3.3-37 are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in Table 3.3-1: General operating conditions.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		2	-	16	MHz
	PLL input clock duty cycle	-		10	-	90	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	VOS0		1.5	-	480(2)	MHz
		VOS1		1.5	-	400(2)	
		VOS2		1.5	-	300(2)	
		VOS3		1.5	-	200(2)	
f_{VCO_OUT}	PLL VCO output	-		192	-	960	
t_{LOCK}	PLL lock time	Normal mode		-	50(3)	150(3)	µs
		Sigma-delta mode (CKIN ≥ 8 MHz)		-	58(3)	166(3)	
Jitter	Cycle-to-cycle jitter(4)	-	VCO = 192 MHz	-	134	-	±ps
			VCO = 200 MHz	-	134	-	
			VCO = 400 MHz	-	76	-	
			VCO = 800 MHz	-	39	-	
	Long term jitter	Normal mode	VCO = 800 MHz	-	±0.7	-	%
		Sigma-delta mode (CKIN = 16 MHz)	VCO = 800 MHz	-	±0.8	-	
$I_{DD(PLL)}$(3)	PLL power consumption on V_{DD}	VCO freq = 836 MHz	V_{DDA}	-	590	1500	µA
			V_{CORE}	-	720	-	
		VCO freq = 192 MHz	V_{DDA}	-	180	600	
			V_{CORE}	-	280	-	

1. Guaranteed by design unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation (480 MHz for VOS0, 400 MHz for VOS1, 300 MHz for VOS2, 200 MHz for VOS3).
3. Guaranteed by characterization results.
4. Integer mode only.

Table 3.3-37: PLL characteristics (wide VCO frequency range)(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		1	-	2	MHz
	PLL input clock duty cycle	-		10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R	VOS1		1.17	-	210	MHz
		VOS2		1.17	-	210	
		VOS3		1.17	-	200	
f_{VCO_OUT}	PLL VCO output	-		150	-	420	
t_{LOCK}	PLL lock time	Normal mode		-	60(2)	100(2)	µs
		Sigma-delta mode		forbidden			
Jitter	Cycle-to-cycle jitter(3)	-	VCO = 150 MHz	-	145	-	±ps
			VCO = 300 MHz	-	91	-	
			VCO = 400 MHz	-	64	-	
			VCO = 420 MHz	-	63	-	
	Period jitter	f_{PLL_OUT} = 50 MHz	VCO = 150 MHz	-	55	-	±-ps
			VCO = 400 MHz	-	30	-	
	Long term jitter	Normal mode	VCO = 400 MHz	-	±0.3	-	%
I(PLL)(2)	PLL power consumption on V_{DD}	VCO freq = 420MHz	VDD	-	440	1150	µA
			VCORE	-	530	-	
		VCO freq = 150MHz	VDD	-	180	500	
			VCORE	-	200	-	

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by characterization results.
3. Integer mode only.

Table 3.3-38: PLL characteristics (medium VCO frequency range)(1)

3.3.12 Memory characteristics

Flash memory

The characteristics are given at T_J = –40 to 125 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode	-	6.5	-	mA
		Write / Erase 16-bit mode	-	11.5	-	
		Write / Erase 32-bit mode	-	20	-	
		Write / Erase 64-bit mode	-	35	-	

Table 3.3-39: Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word (266 bits) programming time	Program/erase parallelism x 8	-	290	580(2)	µs
		Program/erase parallelism x 16	-	180	360	
		Program/erase parallelism x 32	-	130	260	
		Program/erase parallelism x 64	-	100	200	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism x 8	-	2	4	s
		Program/erase parallelism x 16	-	1.8	3.6	
		Program/erase parallelism x 32	-			
t_{ME}	Mass erase time	Program/erase parallelism x 8	-	13	26	
		Program/erase parallelism x 16	-	8	16	
		Program/erase parallelism x 32	-	6	12	
		Program/erase parallelism x 64	-	5	10	
V_{prog}	Programming voltage	Program parallelism x 8	1.62	-	3.6	V
		Program parallelism x 16				
		Program parallelism x 32				
		Program parallelism x 64	1.8	-	3.6	

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 10K erase operations.

Table 3.3-40: Flash memory programming (single bank configuration nDBANK=1)

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_J = –40 to +125 °C (6 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle at T_A = 85 °C	30	Years
		10 kcycles at T_A = 55 °C	20	

1. Guaranteed by characterization results.

Table 3.3-41: Flash memory endurance and data retention

3.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB:** A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in Table 3.3-42. They are based on the EMS levels and classes defined in application note AN1709.

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, UFBGA240, $f_{rcc\_c\_ck}$ = 400 MHz, conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance		5A

Table 3.3-42: EMS characteristics

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/400 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, UFBGA240 package, conforming to IEC61967-2	0.1 to 30 MHz	11	dBµV
			30 to 130 MHz	6	
			130 MHz to 1 GHz	12	
			1 GHz to 2 GHz	7	
			EMI Level	2.5	-

Table 3.3-43: EMI characteristics

3.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	All	1C	1000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All	C1	250	

1. Guaranteed by characterization results.

Table 3.3-44: ESD absolute maximum ratings

Static Latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

Symbol	Parameter	Conditions	Class
LU	Static latchup class	T_A = +25 °C conforming to JESD78	II level A

Table 3.3-45: Electrical sensitivities

3.3.15 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	PA7, PC5, PG1, PB14, PJ7, PA11, PA12, PA13, PA14, PA15, PJ12, PB4	5	0	mA
	PA2, PH2, PH3, PE8, PA6, PA7, PC4, PE7, PE10, PE11	0	NA	
	PA0, PA_C, PA1, PA1_C, PC2, PC2_C, PC3, PC3_C, PA4, PA5, PH4, PH5, BOOT0	0	0	
	All other I/Os	5	NA	

1. Guaranteed by characterization.

Table 3.3-46: I/O current injection susceptibility(1)

3.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 3.3-47: I/O static characteristics are derived from tests performed under the conditions summarized in Table 3.3-1: General operating conditions. All I/Os are CMOS and TTL compliant (except for BOOT0).

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	0.3 V_{DD}(1)	V
	I/O input low level voltage except BOOT0		-	-	0.4V_{DD}−0.1(2)	
	BOOT0 I/O input low level voltage		-	-	0.19V_{DD}+0.1(2)	
V_{IH}	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.7V_{DD}(1)	-	-	V
	I/O input high level voltage except BOOT0(3)		0.47V_{DD}+0.25(2)	-	-	
	BOOT0 I/O input high level voltage(3)		0.17V_{DD}+0.6(2)	-	-	
V_{HYS} (2)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V< V_{DDIOx} <3.6 V	-	250	-	mV
	BOOT0 I/O input hysteresis		-	200	-	
I_{leak} (4)	FT_xx Input leakage current(2)	0< V_{IN} ≤ Max(V_{DDXXX})(9)	-	-	+/-250	nA
		Max(V_{DDXXX}) < V_{IN} ≤ 5.5 V (5)(6)(9)	-	-	1500	
	FT_u IO	0< V_{IN} ≤ Max(V_{DDXXX})(9)	-	-	+/- 350	
		Max(V_{DDXXX}) < V_{IN} ≤ 5.5 V (5)(6)(9)	-	-	5000(7)	
	TT_xx Input leakage current	0< V_{IN} ≤ Max(V_{DDXXX}) (9)	-	-	+/-250	
	VPP (BOOT0 alternate function)	0< V_{IN} ≤ V_{DDIOX}	-	-	15	
		V_{DDIOX} < V_{IN} ≤ 9 V			35	
R_{PU}	Weak pull-up equivalent resistor(8)	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(8)	V_{IN}=V_{DD}(9)	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Compliant with CMOS requirements.
2. Guaranteed by design.
3. V_{DDIOx} represents V_{DDIO1}, V_{DDIO2} or V_{DDIO3}. V_{DDIOx}= V_{DD}.
4. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: $I_{Total\_Ileak\_max}$ = 10 μA + [number of I/Os where V_{IN} is applied on the pad] x $I_{lkg(Max)}$.
5. All FT_xx IO except FT_lu, FT_u and PC3.
6. V_{IN} must be less than Max(VDDXXX) + 3.6 V.
7. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, $V_{DD33USB}$) +0.3 V, the internal pull-up and pull-down resistors must be disabled.
8. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).
9. Max(VDDXXX) is the maximum value of all the I/O supplies.

Table 3.3-47: I/O static characteristics

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in Figure 3.3-11.

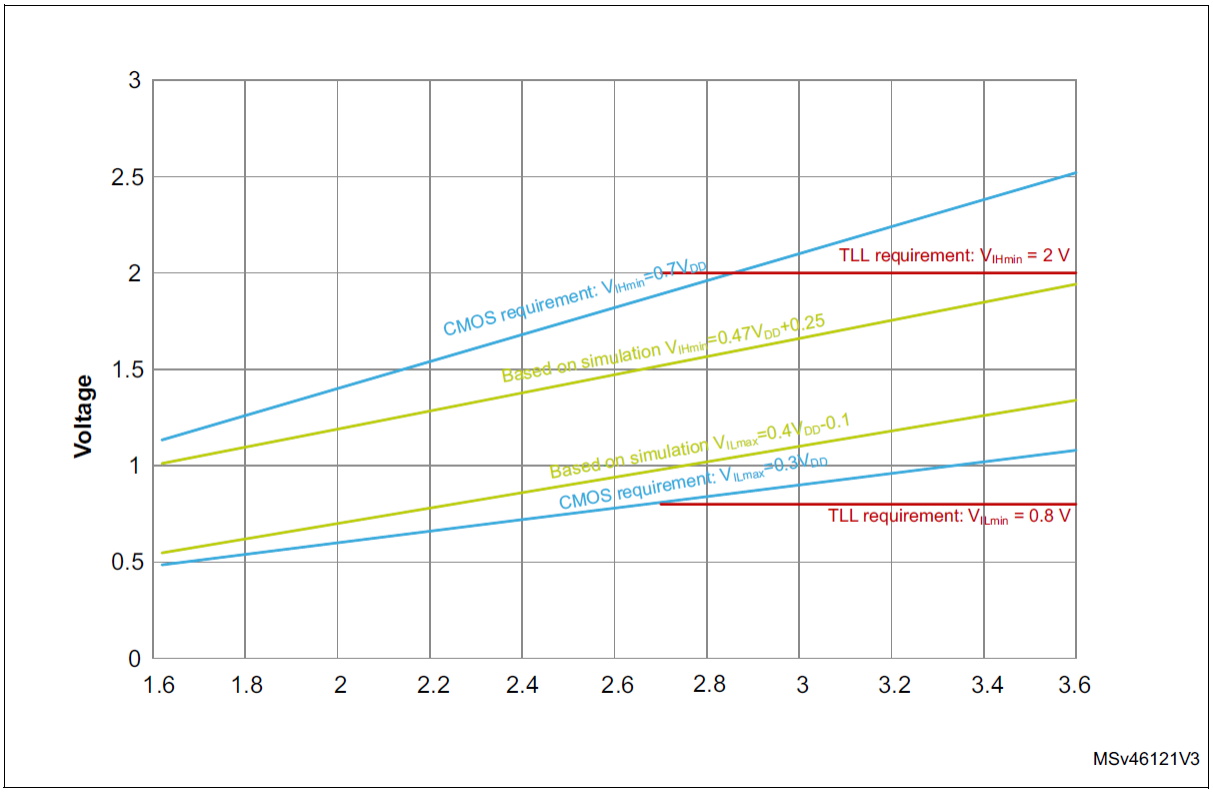


Figure 3.3-11: V_{IL}/V_{IH} for all I/Os except BOOT0

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in Section 3.2. In particular:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see Table 3.2-2).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see Table 3.2-2).

Output voltage levels

Unless otherwise specified, the parameters given in Table 3.3-48: Output voltage characteristics for all I/Os except PC13, PC14, PC15 and PI8[1] and Table 3.3-49: Output voltage characteristics for PC13, PC14, PC15 and PI8[1] are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in Table 3.3-1: General operating conditions. All I/Os are CMOS and TTL compliant.

Symbol	Parameter	Conditions[3]	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port[2] I_{IO}=8 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port[2] I_{IO}=-8 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	
V_{OL}[3]	Output low level voltage	TTL port[2] I_{IO}=8 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}[3]	Output high level voltage	TTL port[2] I_{IO}=-8 mA 2.7 V≤ V_{DD} ≤3.6 V	2.4	-	
V_{OL}[3]	Output low level voltage	I_{IO}=20 mA 2.7 V≤ V_{DD} ≤3.6 V	-	1.3	
V_{OH}[3]	Output high level voltage	I_{IO}=-20 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−1.3	-	
V_{OL}[3]	Output low level voltage	I_{IO}=4 mA 1.62 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}[3]	Output high level voltage	I_{IO}=-4 mA 1.62 V≤V_{DD}<3.6 V	V_{DD}−-0.4	-	
V_{OLFM+}[3]	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO}= 20 mA 2.3 V≤ V_{DD}≤3.6 V	-	0.4	
		I_{IO}= 10 mA 1.62 V≤ V_{DD} ≤3.6 V	-	0.4	

1. The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 3.2-1: Voltage characteristics[1], and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Table 3.3-48: Output voltage characteristics for all I/Os except PC13, PC14, PC15 and PI8[1]

Symbol	Parameter	Conditions[3]	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port[2] I_{IO}=3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port[2] I_{IO}=-3 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	
V_{OL}[3]	Output low level voltage	TTL port[2] I_{IO}=3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}[2]	Output high level voltage	TTL port[2] I_{IO}=-3 mA 2.7 V≤ V_{DD} ≤3.6 V	2.4	-	
V_{OL}[2]	Output low level voltage	I_{IO}=1.5 mA 1.62 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}[2]	Output high level voltage	I_{IO}=-1.5 mA 1.62 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	

1. The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 3.2-1: Voltage characteristics[1], and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Table 3.3-49: Output voltage characteristics for PC13, PC14, PC15 and PI8[1]

Output buffer timing characteristics (HSLV option disabled)

The HSLV bit of SYSCFG_CCCSR register can be used to optimize the I/O speed when the product voltage is below 2.7 V.

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(3)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	12	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	12	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	16	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	4	
	t_r/ t_f(4)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	16.6	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	33.3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	13.3	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	25	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
01	F_{max}(3)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	60	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	80	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	110	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
	t_r/ t_f(4)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	5.2	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	4.2	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	7.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	2.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	5.2	
10	F_{max}(3)	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	85	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	35	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	110	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	40	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	166	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	100	
	t_r/ t_f(4)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	3.8	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	6.9	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	2.8	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(5)	-	5.2	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(5)	-	1.8	

			C=10 pF, 1.62 V≤V_{DD}≤2.7 V[v]	-	3.3	
11	F_{max}[3]	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V[v]	-	100	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V[5]	-	50	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V[v]	-	133	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V[5]	-	66	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V[5]	-	220	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V[5]	-	85	
	t_r/ t_f[4]	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V[5]	-	3.3	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V[5]	-	6.6	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V[5]	-	2.4	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V[5]	-	4.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V[5]	-	1.5	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V[5]	-	2.7	

1. Guaranteed by design.
2. The frequency of the GPIOs that can be supplied in VBAT mode (PC13, PC14, PC15 and PI8) is limited to 2 MHz
3. The maximum frequency is defined with the following conditions:
   (t_r+t_f) ≤ 2/3 T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
4. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
5. Compensation system enabled.

Table 3.3-50: Output timing characteristics (HSLV OFF)[1][2]

Output buffer timing characteristics (HSLV option enabled)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
	t_r/ t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	11	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	9	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	6.6	
01	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	50	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	58	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	66	
	t_r/ t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	6.6	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	4.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
10	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	55	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	80	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	133	
	t_r/ t_f(3)	Output high to low level fall time and output low to high level rise time	C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.8	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	4	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	2.4	
11	F_{max}(2)	Maximum frequency	C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	60	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	90	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	175	
	t_r/ t_f(3)	Output high to low level fall time and output low to high level rise time	C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.3	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	3.6	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	1.9	

1. Guaranteed by design.
2. The maximum frequency is defined with the following conditions:
   (t_r+t_f) ≤ 2/3 T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

Table 3.3-51: Output timing characteristics (HSLV ON)(1)

3.3.17 NRST pin characteristics

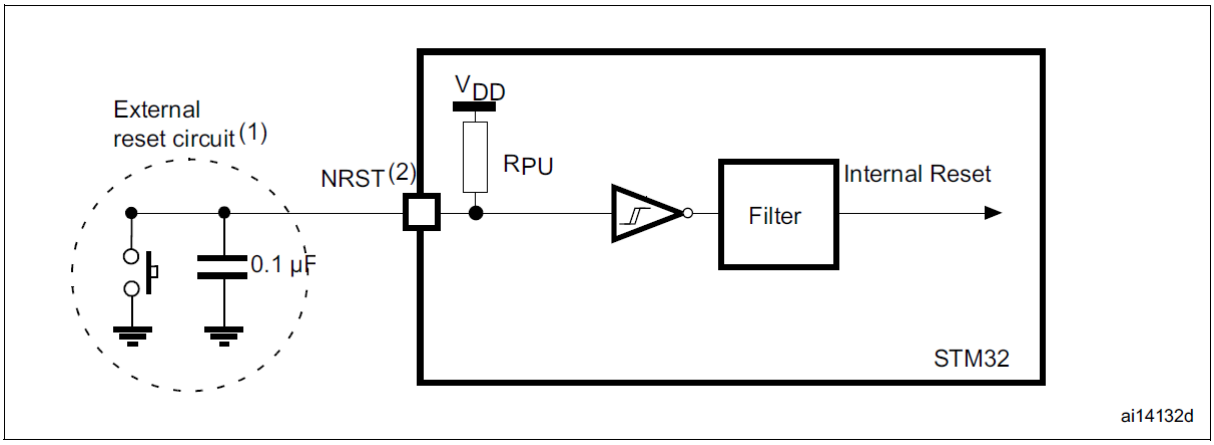
The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see Table 3.3-47: I/O static characteristics).

Unless otherwise specified, the parameters given in Table 3.3-52 are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in Table 3.3-1: General operating conditions.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(2)	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	1.71 V < V_{DD} < 3.6 V	-	-	50	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	1.71 V < V_{DD} < 3.6 V	300	-	-	
		1.62 V < V_{DD} < 3.6 V	1000	-	-	

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Table 3.3-52: NRST pin characteristics



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 3.3-47. Otherwise the reset is not taken into account by the device.

Figure 3.3-12: Recommended NRST pin protection

3.3.18 FMC characteristics

Unless otherwise specified, the parameters given in Table 3.3-53 to Table 3.3-66 for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in Table 3.3-1: General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS1.

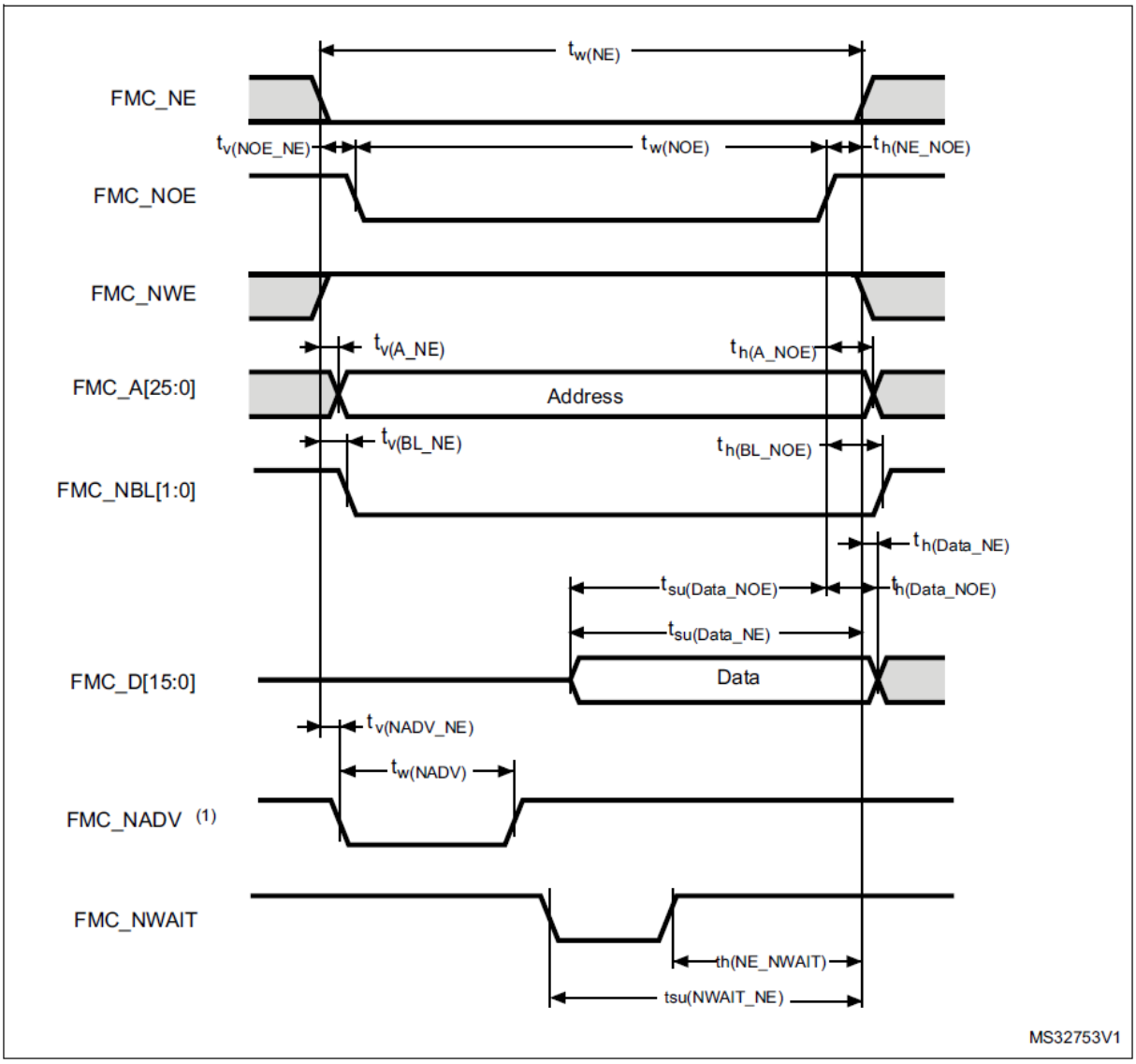
Refer to Section 3.3.16: I/O port characteristics for more details on the input/output alternate function characteristics.

Asynchronous waveforms and timings

Figure 3.3-13 through Figure 3.3-15 represent asynchronous waveforms and Table 3.3-53 through Table 3.3-60 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

In all timing tables, the T_{KERCK} is the $f_{mc\_ker\_ck}$ clock period.



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Figure 3.3-13: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc\_ker\_ck}-1$	$3T_{fmc\_ker\_ck}+1$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{fmc\_ker\_ck}-1$	$2T_{fmc\_ker\_ck}+1$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	11	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	11	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc\_ker\_ck}+1$	

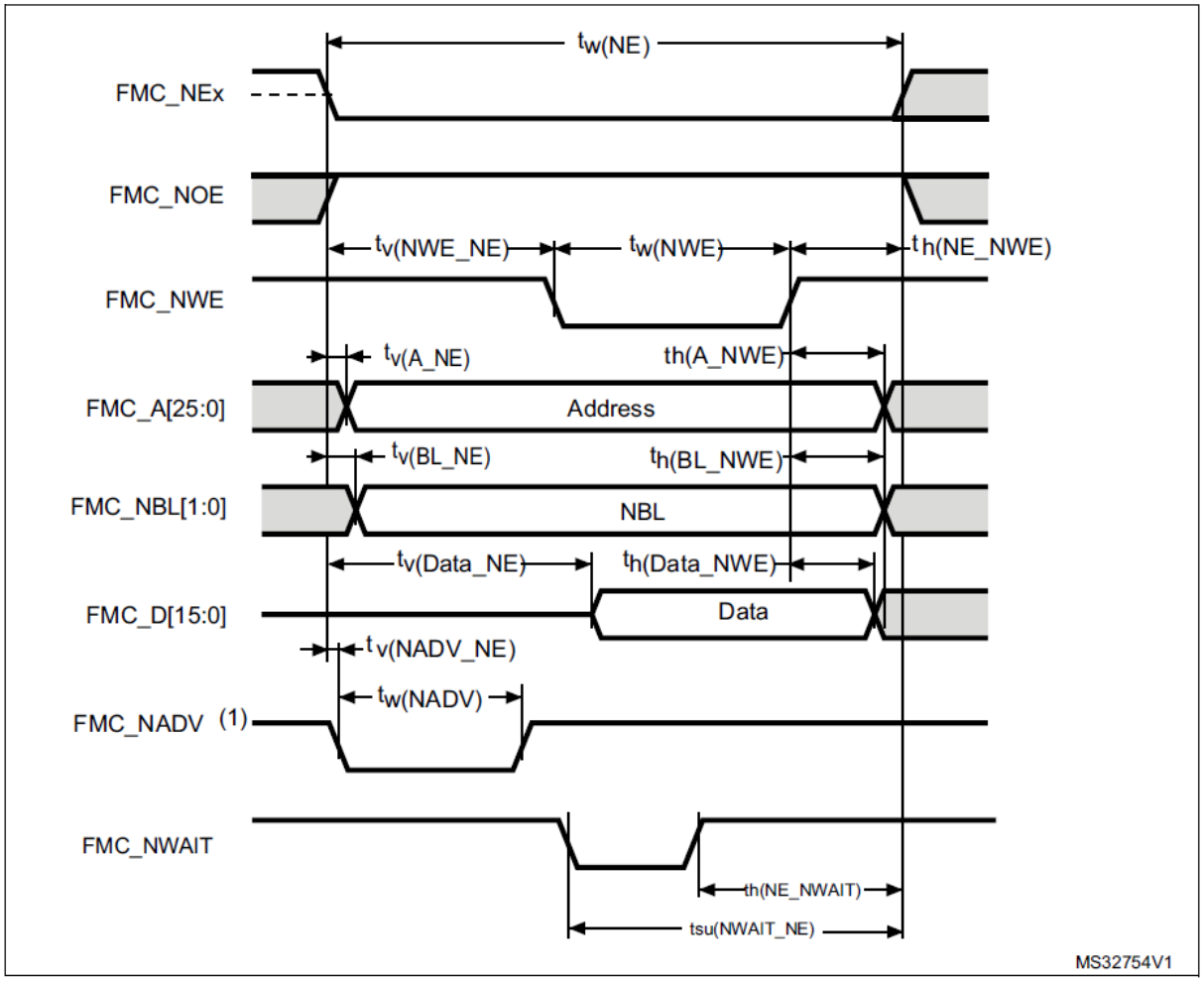
1. Guaranteed by characterization results.

Table 3.3-53: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{fmc\_ker\_ck}+1$	$7T_{fmc\_ker\_ck}+1$	ns
$t_{w(NOE)}$	FMC_NOE low time	$5T_{fmc\_ker\_ck}-1$	$5T_{fmc\_ker\_ck}+1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc\_ker\_ck}-0.5$	-	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$4T_{fmc\_ker\_ck}+11$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$3T_{fmc\_ker\_ck}+11.5$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Table 3.3-54: Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)(2)



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Figure 3.3-14: Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc\_ker\_ck}$ –1	$3T_{fmc\_ker\_ck}$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc\_ker\_ck}$	$T_{fmc\_ker\_ck}$+1	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc\_ker\_ck}$ –0.5	$T_{fmc\_ker\_ck}$+0.5	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc\_ker\_ck}$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc\_ker\_ck}$ –0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc\_ker\_ck}$ –0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{fmc\_ker\_ck}$+ 2.5	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc\_ker\_ck}$+0.5	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc\_ker\_ck}$+ 1	

1. Guaranteed by characterization results.

Table 3.3-55: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc\_ker\_ck}$ –1	$8T_{fmc\_ker\_ck}$+1	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{fmc\_ker\_ck}$ –1.5	$6T_{fmc\_ker\_ck}$+0.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc\_ker\_ck}$+13	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc\_ker\_ck}$+13	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Table 3.3-56: Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)(2)

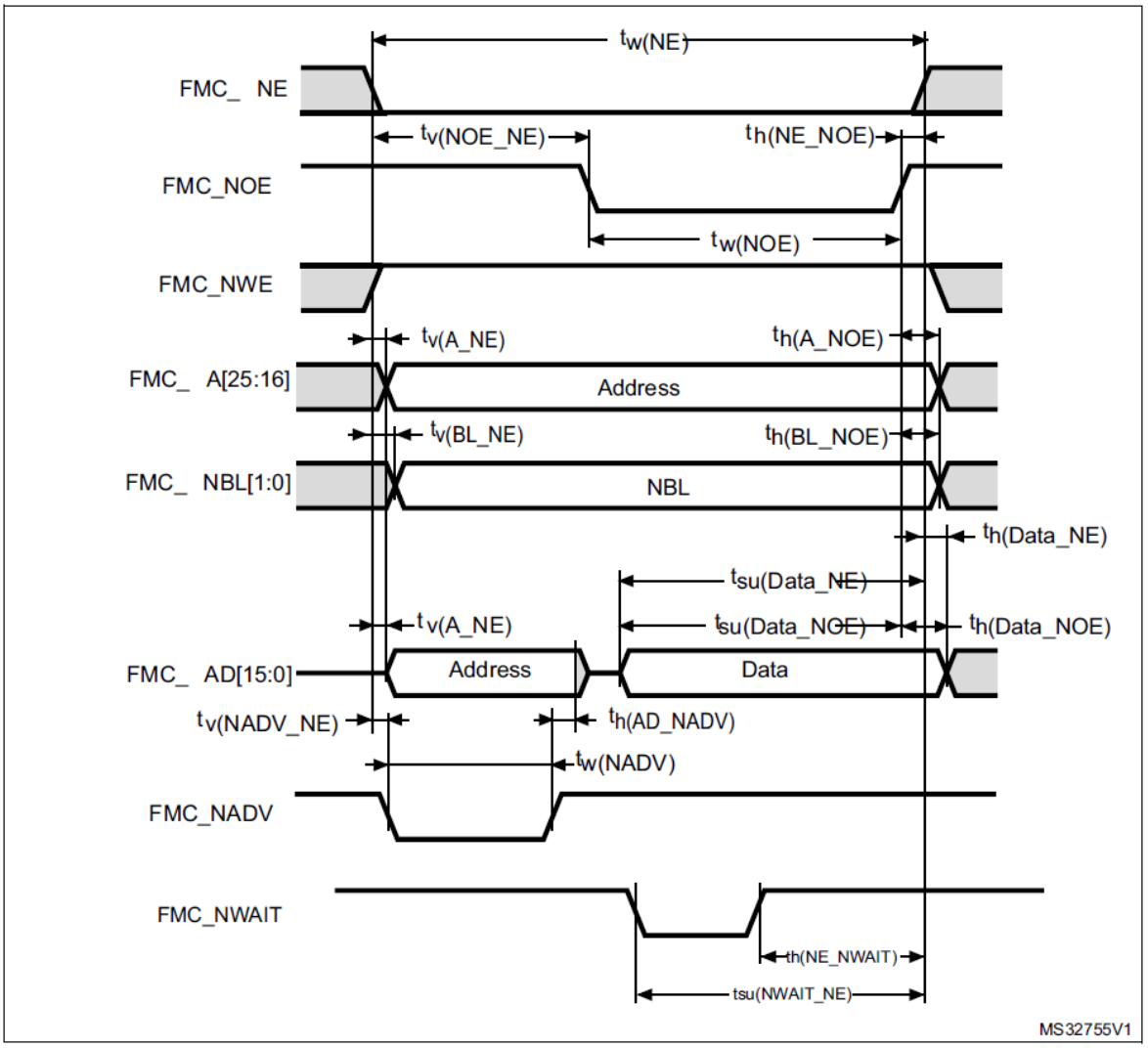


Figure 3.3-15: Asynchronous multiplexed PSRAM/NOR read waveforms

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc\_ker\_ck}$ –1	$4T_{fmc\_ker\_ck}$ +1	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{fmc\_ker\_ck}$	$2T_{fmc\_ker\_ck}$ +0.5	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{fmc\_ker\_ck}$ –1	$T_{fmc\_ker\_ck}$ +1	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc\_ker\_ck}$ –0.5	$T_{fmc\_ker\_ck}$ +1	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high)	$T_{fmc\_ker\_ck}$ +0.5	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	$T_{fmc\_ker\_ck}$ –0.5	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	11	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	11	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Guaranteed by characterization results.

Table 3.3-57: Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc\_ker\_ck}$ –1	$8T_{fmc\_ker\_ck}$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{fmc\_ker\_ck}$ –1.5	$5T_{fmc\_ker\_ck}$ +0.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$4T_{fmc\_ker\_ck}$ +11	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$3T_{fmc\_ker\_ck}$ +11.5	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Table 3.3-58: Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc\_ker\_ck} - 1$	$4T_{fmc\_ker\_ck}$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc\_ker\_ck} - 1$	$T_{fmc\_ker\_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{fmc\_ker\_ck} - 0.5$	$2T_{fmc\_ker\_ck} + 0.5$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc\_ker\_ck}$	$T_{fmc\_ker\_ck} + 1$	
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high)	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	$T_{fmc\_ker\_ck} + 2$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc\_ker\_ck} + 0.5$	-	

1. Guaranteed by characterization results.

Table 3.3-59: Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc\_ker\_ck} - 1$	$9T_{fmc\_ker\_ck}$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{fmc\_ker\_ck} - 0.5$	$7T_{fmc\_ker\_ck} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc\_ker\_ck} + 11$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc\_ker\_ck} + 11.5$	-	

1. Guaranteed by characterization results.

2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Table 3.3-60: Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Synchronous waveforms and timings

Figure 3.3-16 through Figure 3.3-19 represent synchronous waveforms and Table 3.3-61 through Table 3.3-64 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all the timing tables, the $T_{fmc\_ker\_ck}$ is the $f_{mc\_ker\_ck}$ clock period, with the following FMC_CLK maximum values:

- For 2.7 V<V_{DD}<3.6 V, FMC_CLK = 125 MHz at 20 pF
- For 1.8 V<V_{DD}<1.9 V, FMC_CLK = 100 MHz at 20 pF
- For 1.62 V<V_{DD}<1.8 V, FMC_CLK = 100 MHz at 15 pF

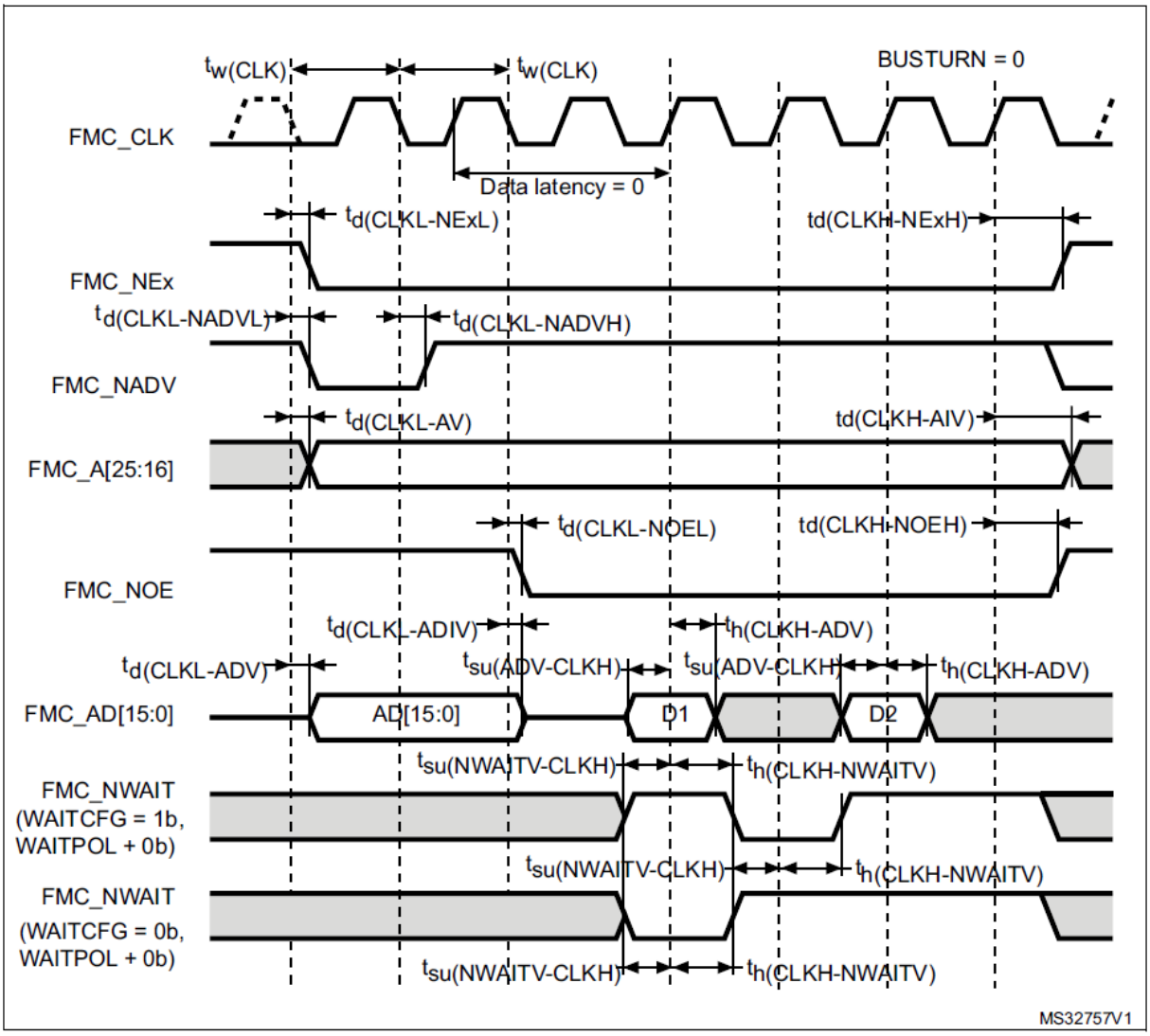


Figure 3.3-16: Synchronous multiplexed NOR/PSRAM read timings

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck}$ –1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck}$+0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc\_ker\_ck}$ –0.5	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	2	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

Table 3.3-61: Synchronous multiplexed NOR/PSRAM read timings(1)

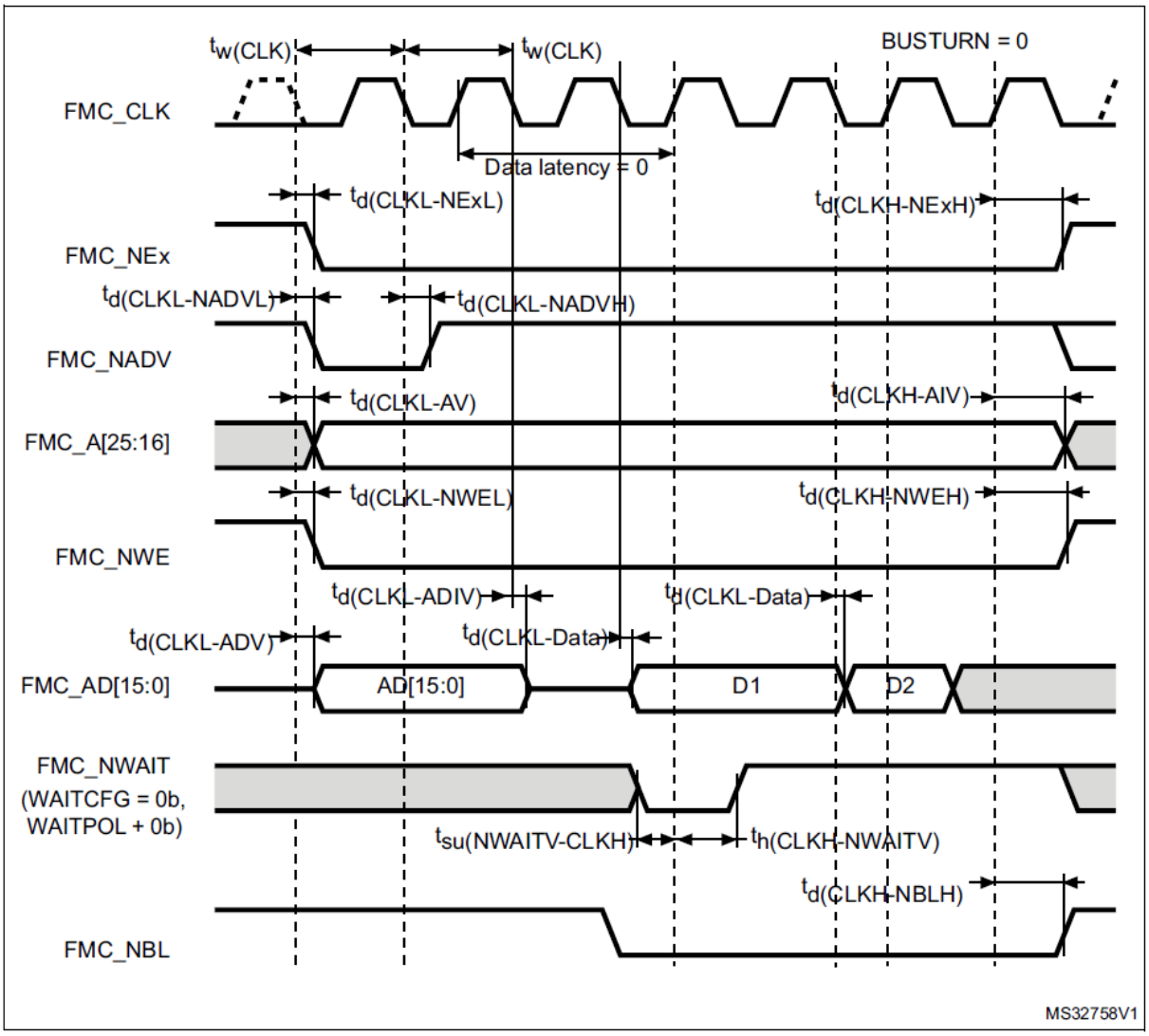


Figure 3.3-17: Synchronous multiplexed PSRAM write timings

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period, V_{DD} = 2.7 to 3.6 V	$2T_{fmc\_ker\_ck}$ –1 1	-	Ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x =0..2)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0…2)	$T_{fmc\_ker\_ck}$ +0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x =16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x =16…25)	$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc\_ker\_ck}$ +0.5	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to to FMC_AD[15:0] valid	-	2.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	2.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc\_ker\_ck}$ +0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

Table 3.3-62: Synchronous multiplexed PSRAM write timings(1)

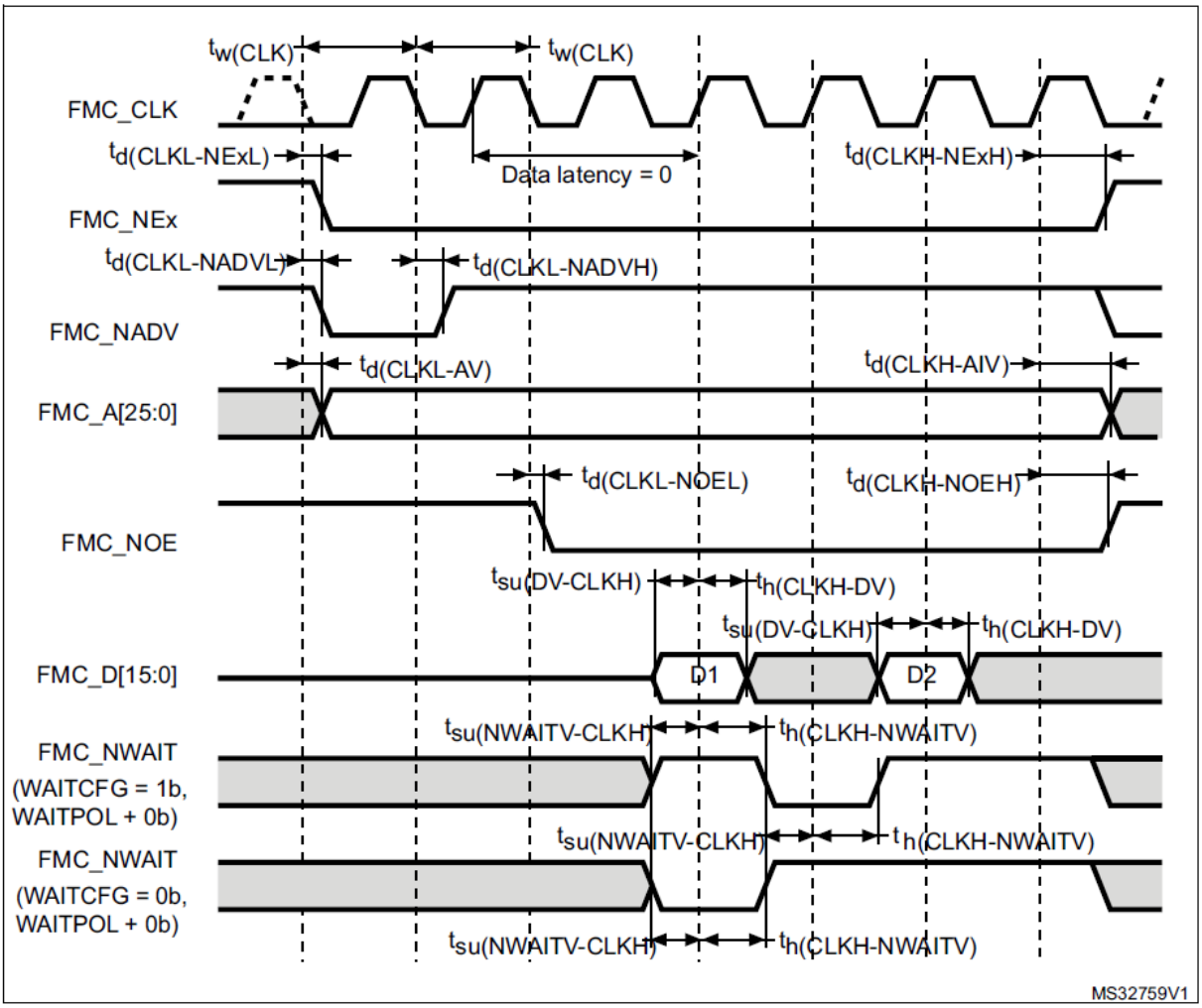


Figure 3.3-18: Synchronous non-multiplexed NOR/PSRAM read timings

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck}$ –1	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$2T_{fmc\_ker\_ck}$+0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$2T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$2T_{fmc\_ker\_ck}$-0.5	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	2	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	1	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

Table 3.3-63: Synchronous non-multiplexed NOR/PSRAM read timings(1)

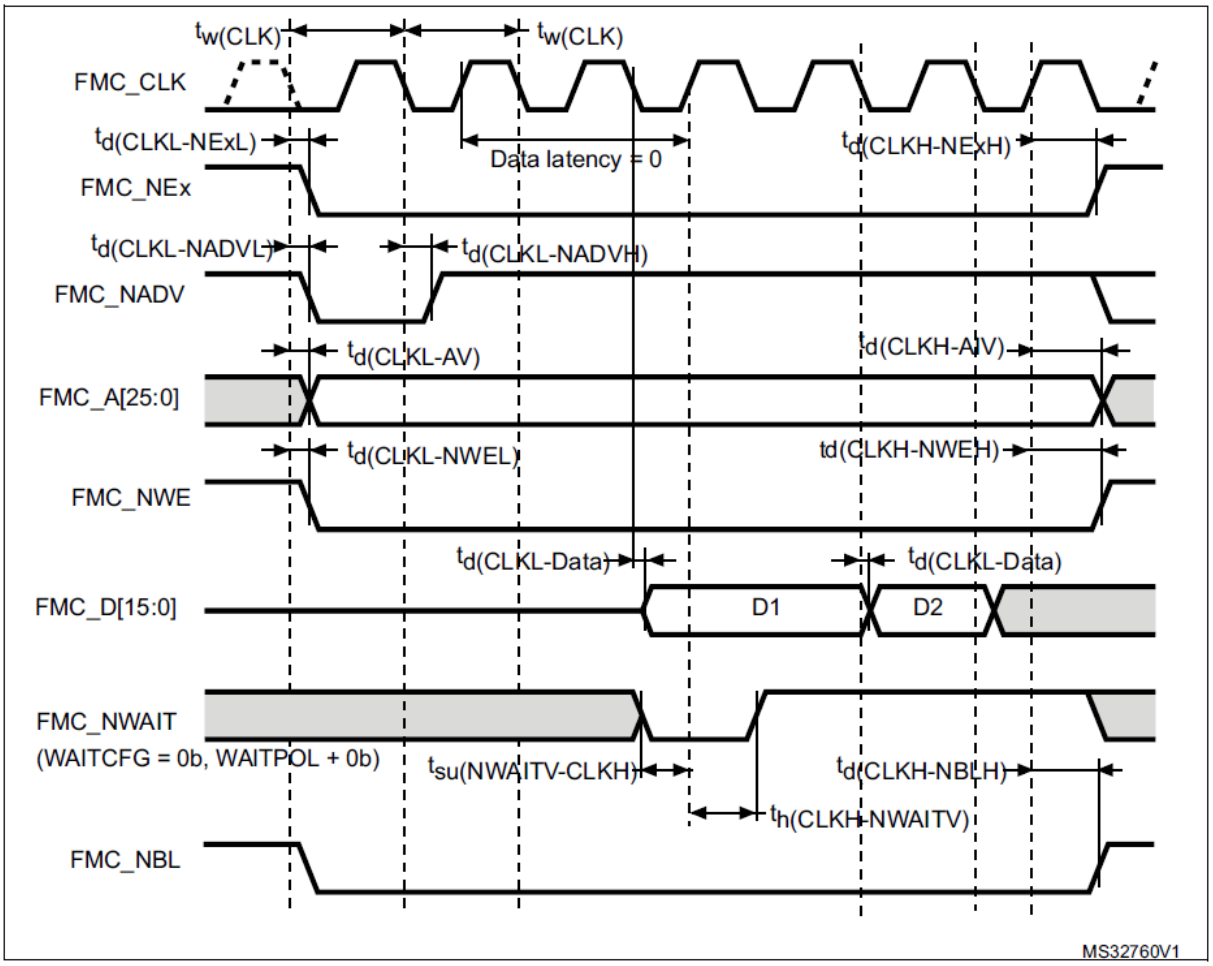


Figure 3.3-19: Synchronous non-multiplexed PSRAM write timings

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck}$ –1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck}$**+0.5**	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	**0**	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc\_ker\_ck}$+1	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc\_ker\_ck}$+1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

Table 3.3-64: Synchronous non-multiplexed PSRAM write timings(1)

NAND controller waveforms and timings

Figure 3.3-20 through Figure 3.3-23 represent synchronous waveforms, and Table 3.3-65 and Table 3.3-66 provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

- Capacitive load CL = 30 pF

In all timing tables, the $T_{fmc\_ker\_ck}$ is the $f_{mc\_ker\_ck}$ clock period.

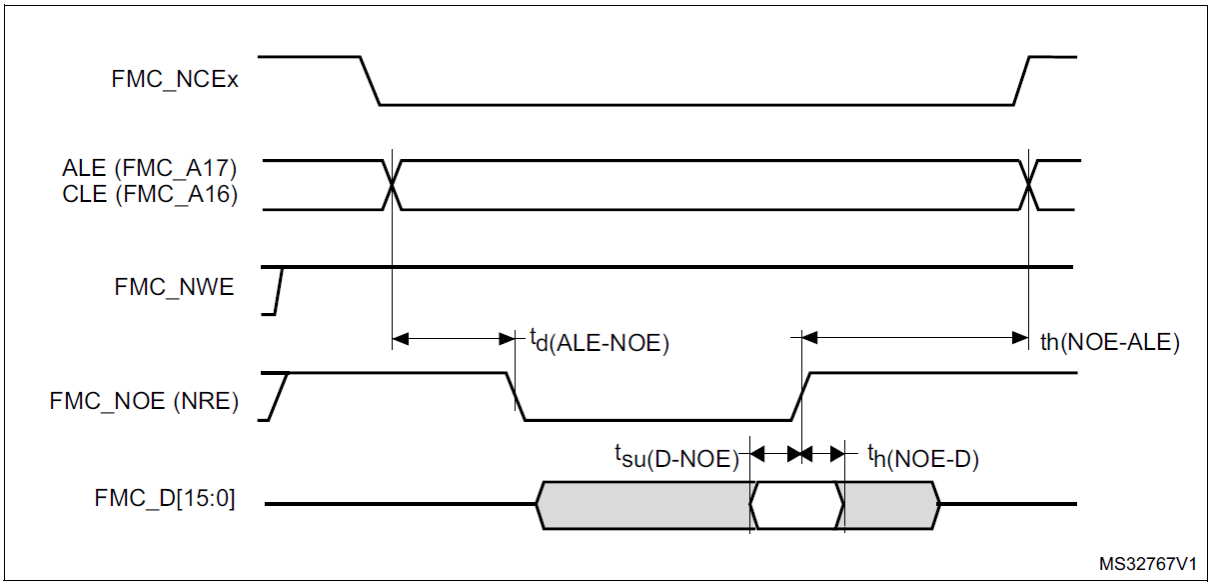


Figure 3.3-20: NAND controller waveforms for read access

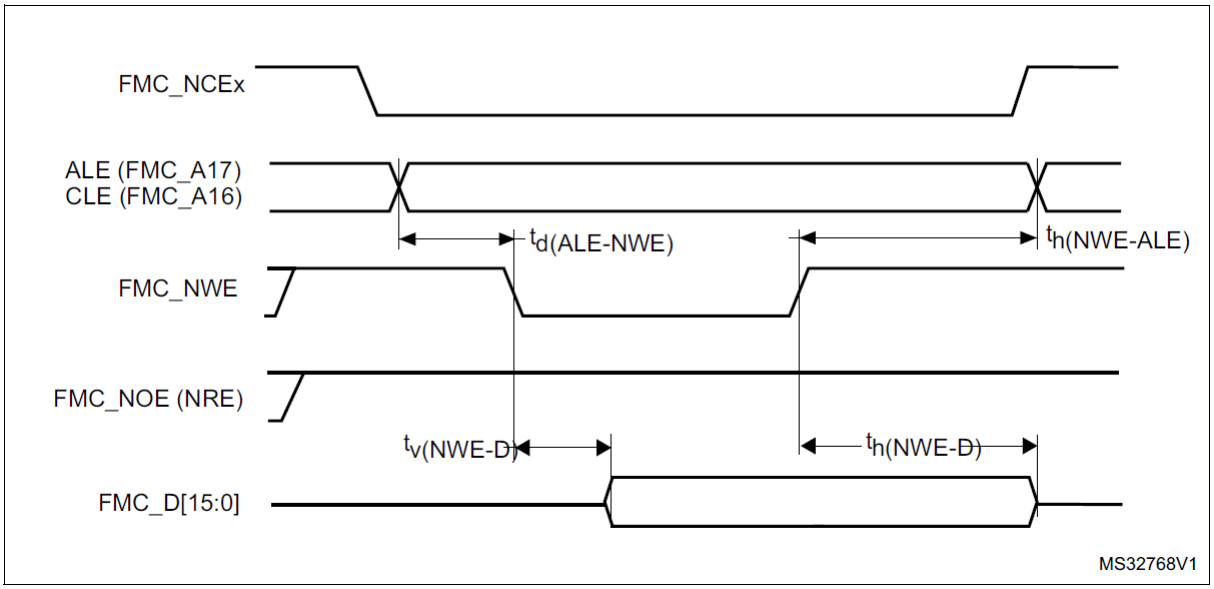


Figure 3.3-21: NAND controller waveforms for write access

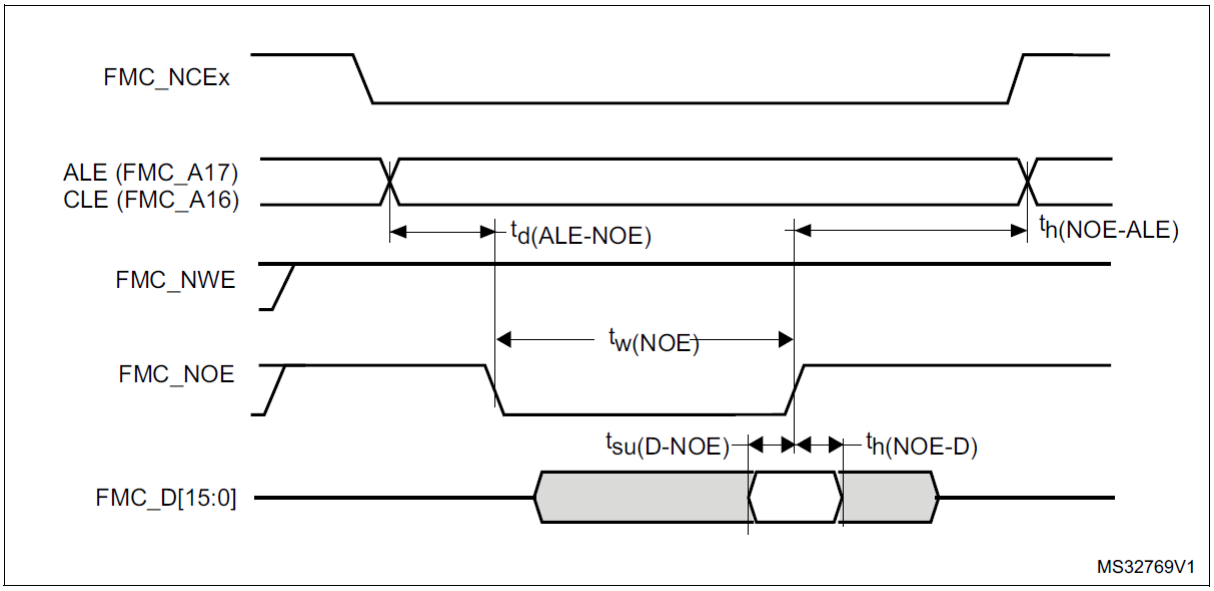


Figure 3.3-22: NAND controller waveforms for common memory read access

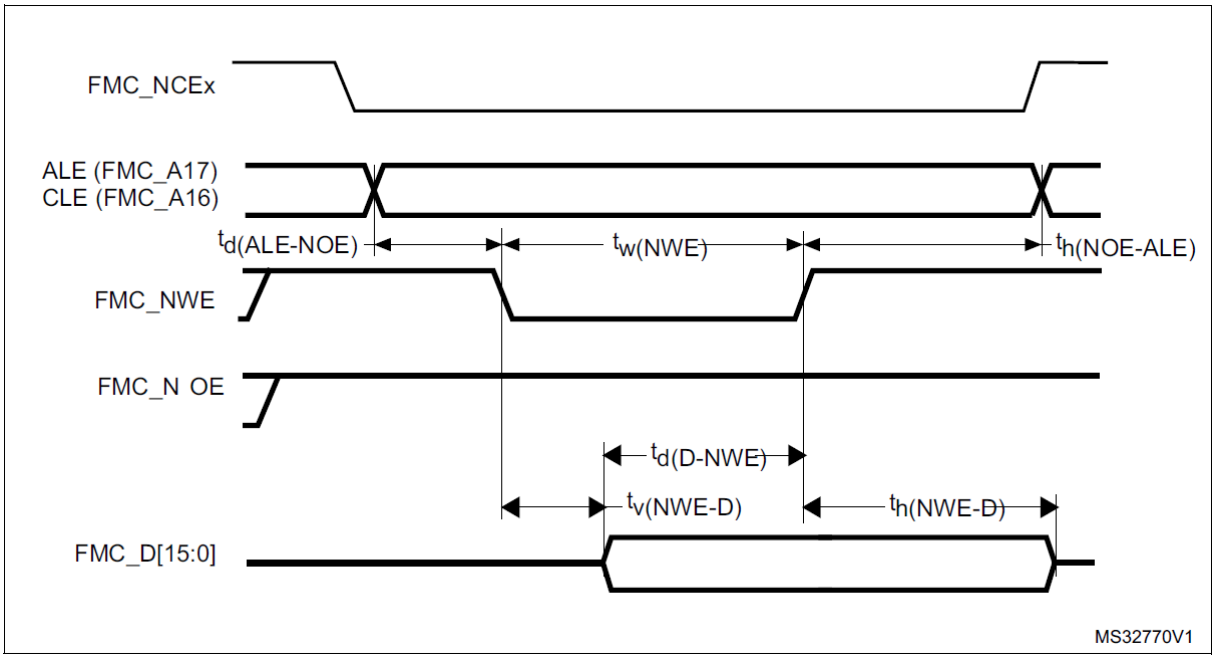


Figure 3.3-23: NAND controller waveforms for common memory write access

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{fmc\_ker\_ck} - 0.5$	$4T_{fmc\_ker\_ck}+0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	8	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{fmc\_ker\_ck}$ +1	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$4T_{fmc\_ker\_ck}$ –2	-	

1. Guaranteed by characterization results.

Table 3.3-65: Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc\_ker\_ck} - 0.5$	$4T_{fmc\_ker\_ck}$ +0.5	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{fmc\_ker\_ck} - 0.5$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{fmc\_ker\_ck} - 1$	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{fmc\_ker\_ck}$ +0.5	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{fmc\_ker\_ck} - 1$	-	

1. Guaranteed by characterization results.

Table 3.3-66: Switching characteristics for NAND Flash write cycles(1)

SDRAM waveforms and timings

In all timing tables, the TKERCK is the fmc_ker_ck clock period, with the following FMC_SDCLK maximum values:

- For 2.7 V<V_{DD}<3.6 V: FMC_CLK =110 MHz at 20 pF
- For 1.8 V<V_{DD}<1.9 V: FMC_CLK =100 MHz at 20 pF
- For 1.62 V<V_{DD}<1.8 V, FMC_CLK =100 MHz at 15 pF

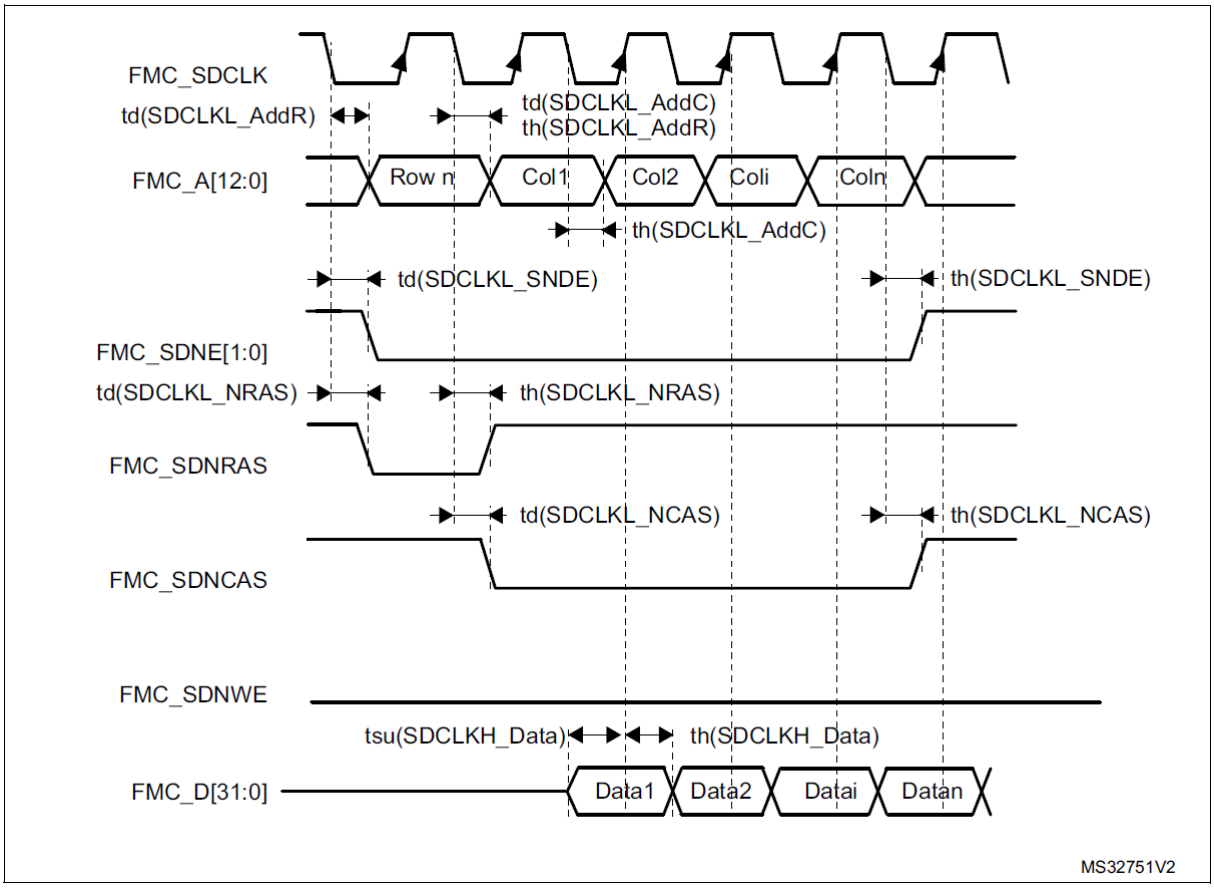


Figure 3.3-24: SDRAM read access waveforms (CL = 1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck}$ +0.5	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	1	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL-\ SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Table 3.3-67: SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck}+0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	1.5	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	2.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Table 3.3-68: LPSDR SDRAM read timings(1)

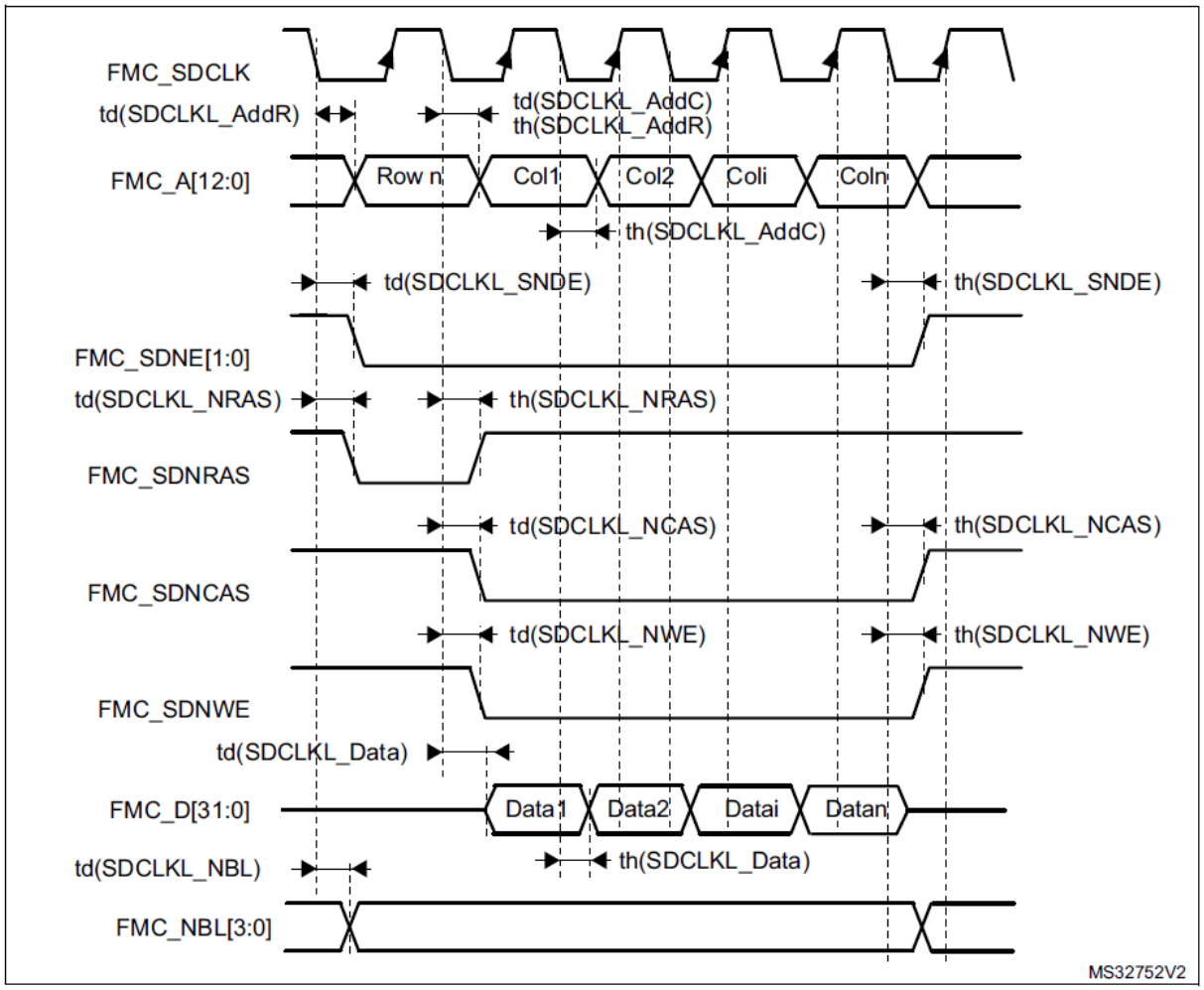


Figure 3.3-25: SDRAM write access waveforms

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck}+0.5$	ns
$t_{d(SDCLKL\ \_Data)}$	Data output valid time	-	1	
$t_{h(SDCLKL\ \_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL\_SDNWE)}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL\_SDNWE)}$	SDNWE hold time	0.5	-	
$t_{d(SDCLKL\_\ SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL\text{-}\_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0.5	-	

1. Guaranteed by characterization results.

Table 3.3-69: SDRAM Write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck}+0.5$	ns
$t_{d(SDCLKL\ \_Data)}$	Data output valid time	-	2.5	
$t_{h(SDCLKL\ \_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL\text{-}SDNWE)}$	SDNWE valid time	-	2.5	
$t_{h(SDCLKL\text{-}SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL\text{-}\ SDNE)}$	Chip select valid time	-	3	
$t_{h(SDCLKL\text{-}\ SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\text{-}SDNRAS)}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL\text{-}SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\text{-}SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{d(SDCLKL\text{-}SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Table 3.3-70: LPSDR SDRAM Write timings(1)

3.3.19 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in Table 3.3-71 and Table 3.3-72 for QUADSPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in Table 3.3-1: General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS1

Refer to Section 3.3.16: I/O port characteristics for more details on the input/output alternate function characteristics.

The following table summarizes the parameters measured in SDR mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{ck1}1/T_{CK}$	QUADSPI clock frequency	2.7<V_{DD}<3.6 V CL = 20 pF	-	-	133	MHz
		1.62<V_{DD}<3.6 V CL = 15 pF	-	-	100	
$t_{w(CKH)}$	QUADSPI clock high and low time Even division	PRESCALER[7:0] = n = 0,1,3,5...	$T_{CK}/2$–0.5	-	$T_{CK}/2$	ns
$t_{w(CKL)}$			$T_{CK}/2$	-	$T_{CK}/2$+0.5	
$t_{w(CKH)}$	QUADSPI clock high and low time Odd division	PRESCALER[7:0] = n = 2,4,6,8...	(n/2)*T_{CK}/(n+1)-0.5	-	(n/2)*T_{CK}/ (n+1)	
$t_{w(CKL)}$			(n/2+1)*T_{CK}/(n+1)	-	(n/2+1)*T_{CK}/ (n+1)+0.5	
$t_{s(IN)}$	Data input setup time	-	1	-	-	
$t_{h(IN)}$	Data input hold time		3.5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	1	2	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

1. Guaranteed by characterization results.

Table 3.3-71: QUADSPI characteristics in SDR mode(1)

The following table summarizes the parameters measured in DDR mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{ck1}1/T_{CK}$	QUADSPI clock frequency	2.7<V_{DD}<3.6 V CL = 20 pF	-	-	100	MHz
		1.62<V_{DD}<3.6 V CL = 15 pF	-	-	100	
$t_{w(CKH)}$	QUADSPI clock high and low time Even division	PRESCALER[7:0] = n = 0,1,3,5...	T_{CK}/2–0.5	-	T_{CK}/2	ns
$t_{w(CKL)}$			T_{CK}/2	-	T_{CK}/2+0.5	
$t_{w(CKH)}$	QUADSPI clock high and low time Odd division	PRESCALER[7:0] = n = 2,4,6,8...	(n/2)*T_{CK}/(n+1)-0.5	-	(n/2)*T_{CK}/(n+1)	
$t_{w(CKL)}$			(n/2+1)*T_{CK}/(n+1)	-	(n/2+1)*T_{CK} /(n+1)+0.5	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	-	1.5	-	-	
$t_{hr(IN)}$,$t_{hf(IN)}$	Data input hold time	-	3.5	-	-	
$t_{vr(OUT)}$,$t_{vf(OUT)}$	Data output valid time	DHHC=0	-	5	6	
		DHHC=1 PRESCALER[7:0] = 1,2…	-	T_{CK}/4+1	T_{CK}/4+2	
$t_{hr(OUT)}$,$t_{hf(OUT)}$	Data output hold time	DHHC=0	3	-	-	
		DHHC=1 PRESCALER[7:0]=1,2…	T_{CK}/4	-	-	

1. Guaranteed by characterization results.

Table 3.3-72: QUADSPI characteristics in DDR mode(1)

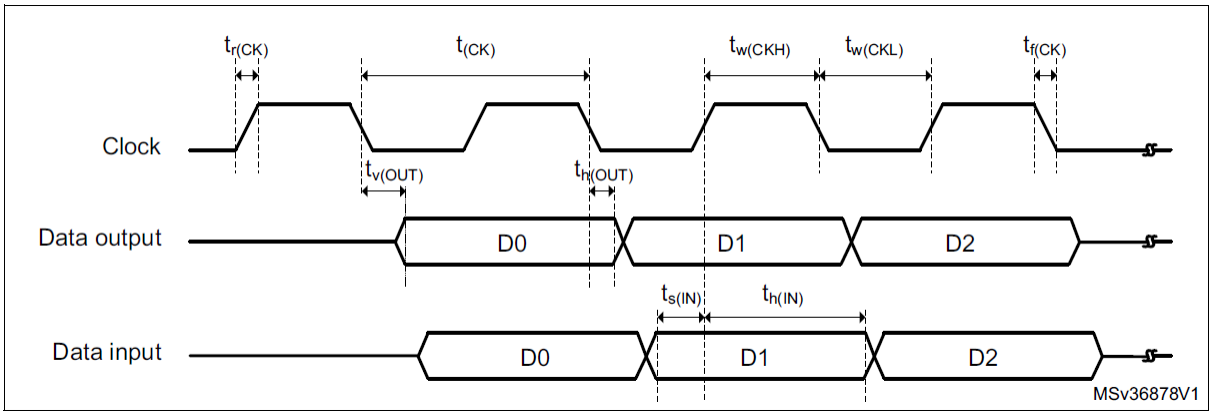


Figure 3.3-26: Quad-SPI timing diagram - SDR mode

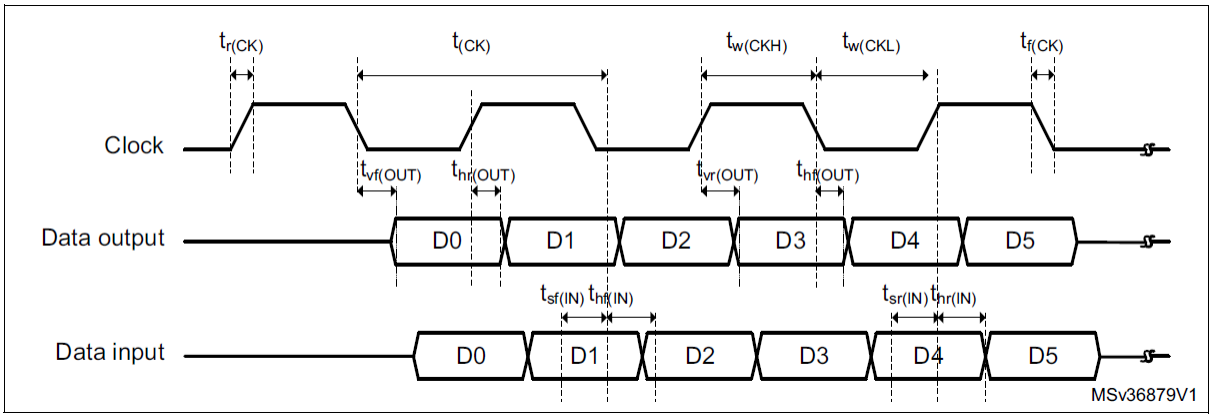


Figure 3.3-27: Quad-SPI timing diagram - DDR mode

3.3.20 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in Table 3.3-73 for Delay Block are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and VDD supply voltage summarized in Table 3.3-1: General operating conditions, with the following configuration:

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	1400	2200	2400	ps
t_{Δ}	Unit Delay	-	35	40	45	-

Table 3.3-73: Delay Block characteristics

3.3.21 16-bit ADC characteristics

Unless otherwise specified, the parameters given in Table 3.3-74 are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in Table 3.3-1.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-		1.62	-	3.6	V
V_{REF+}	Positive reference voltage	-		1.62	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-			V_{SSA}		V
f_{ADC}	ADC clock frequency	1.62 V ≤ VDDA ≤ 3.6 V	BOOST = 11	0.12	-	50	MHz
			BOOST = 10	0.12	-	25	
			BOOST = 01	0.12	-	12.5	
			BOOST = 00	-	-	6.25	

Table 3.3-74: ADC characteristics(1)(2)

Symbol	Parameter	Conditions				Min	Typ	Max	Unit
f_s[3]	Sampling rate for Direct channels	Resolution = 16 bits, V_{DDA} >2.5 V	T_J = 90 °C	f_{ADC}=36 MHz	SMP = 1.5	-	-	3.60	MSps
		Resolution = 16 bits		f_{ADC}=37 MHz	SMP = 2.5	-	-	3.35	
		Resolution = 14 bits	T_J = 125 °C	f_{ADC} = 50 MHz	SMP = 2.5	-	-	5.00	
		Resolution = 12 bits		f_{ADC} = 50 MHz	SMP = 2.5	-	-	5.50	
		Resolution = 10 bits		f_{ADC} = 50 MHz	SMP = 1.5	-	-	7.10	
		Resolution = 8 bits		f_{ADC} = 50 MHz	SMP = 1.5	-	-	8.30	
		Resolution = 14 bits	T_J = 140 °C	f_{ADC} = 49 MHz	SMP = 2.5	-	-	4.90	
		Resolution = 12 bits		f_{ADC} = 50 MHz	SMP = 2.5	-	-	5.50	
		Resolution = 10 bits		f_{ADC} = 50 MHz	SMP = 1.5	-	-	6.70	
		Resolution = 8 bits		f_{ADC} = 50 MHz	SMP = 1.5	-	-	8.30	
	Sampling rate for Fast channels	Resolution = 16 bits, V_{DDA} >2.5 V	T_J = 90 °C	f_{ADC}=32 MHz	SMP = 2.5	-	-	2.90	
		Resolution = 16 bits		f_{ADC}=31 MHz	SMP = 2.5	-	-	2.80	
		Resolution = 14 bits	T_J = 125 °C	f_{ADC} = 33 MHz	SMP = 2.5	-	-	3.30	
		Resolution = 12 bits		f_{ADC} = 39 MHz	SMP = 2.5	-	-	4.30	
		Resolution = 10 bits		f_{ADC} = 48 MHz	SMP = 2.5	-	-	6.00	
		Resolution = 8 bits		f_{ADC} = 50 MHz	SMP = 2.5	-	-	7.10	
		Resolution = 12 bits	T_J = 140 °C	f_{ADC} = 37 MHz	SMP = 2.5	-	-	4.10	
		Resolution = 10 bits		f_{ADC} = 46 MHz	SMP = 2.5	-	-	5.70	
		Resolution = 8 bits		f_{ADC} = 50 MHz	SMP = 2.5	-	-	7.10	
	Sampling rate for Slow channels	Resolution = 16 bits	T_J = 90 °C	f_{ADC} = 10 MHz	SMP = 1.5	-	-	1.00	
		resolution = 14 bits	T_J = 125 °C			-	-		
		resolution = 12 bits				-	-		
		resolution = 10 bits				-	-		
		resolution = 8 bits				-	-		
		resolution = 12 bits	T_J = 140 °C			-	-		
		resolution = 10 bits				-	-		
		resolution = 8 bits				-	-		
t_{TRIG}	External trigger period	Resolution = 16 bits				-	-	10	$1/f_{ADC}$
V_{AIN}[4]	Conversionvoltage range	-				0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	-				$V_{REF}/2$ – 10%	$V_{REF}/2$	$V_{REF}/2$ + 10%	V

Table 3.3-74: ADC characteristics[1][2] (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
R_{AIN} (5)	External input impedance	Resolution = 16 bits, T_J = 140 °C	-	-	-	-	50	Ω
		Resolution = 16 bits, T_J = 125 °C	-	-	-	-	170	
		Resolution = 14 bits, T_J = 140 °C	-	-	-	-	200	
		Resolution = 14 bits, T_J = 125 °C	-	-	-	-	435	
		Resolution = 12 bits, T_J = 140 °C	-	-	-	-	700	
		Resolution = 12 bits, T_J =125 °C	-	-	-	-	1150	
		Resolution = 10 bits, T_J = 140 °C	-	-	-	-	3700	
		Resolution = 10 bits, T_J = 125 °C	-	-	-	-	5650	
		Resolution = 8 bits, T_J = 140 °C	-	-	-	-	18000	
		Resolution = 8 bits, T_J = 125 °C	-	-	-	-	26500	
C_{ADC}	Internal sample and hold capacitor	-			-	4	-	pF
$t_{ADCVREG\_STUP}$	ADC LDO startup time	-			-	5	10	us
t_{STAB}	ADC Power-up time	LDO already started			1	-	-	conversioncycle
t_{CAL}	Offset and linearity calibration time	-			165010	-	-	$1/f_{ADC}$
t_{OFF_CAL}	Offset calibration time	-			1280	-	-	$1/f_{ADC}$
t_{LATR}	Triggerconversion latency regular and injected channels without conversion abort	CKMODE = 00			1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01			-	-	2.5	
		CKMODE = 10			-	-	2.5	
		CKMODE = 11			-	-	2.25	
$t_{LATRINJ}$	Triggerconversion latency regular injected channels aborting a regular conversion	CKMODE = 00			2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01			-	-	3.5	
		CKMODE = 10			-	-	3.5	
		CKMODE = 11			-	-	3.25	
t_S	Sampling time	-			1.5	-	810.5	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	Resolution = N bits			ts + 0.5 + N/2	-	-	$1/f_{ADC}$

Table 3.3-74: ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$I_{DDA–D}$ (ADC)	ADC consumption on V_{DDA}, BOOST=11, Differential mode	Resolution = 16 bits, f_{ADC}=25 MHz	-	-	-	1440	-	µA
		Resolution = 14 bits, f_{ADC}=30 MHz	-	-	-	1350	-	
		Resolution = 12 bits, f_{ADC}=40 MHz	-	-	-	990	-	
	ADC consumption on V_{DDA} BOOST=10, Differential mode f_{ADC}=25 MHz	Resolution = 16 bits	-	-	-	1080	-	
		Resolution = 14 bits	-	-	-	810	-	
		Resolution = 12 bits	-	-	-	585	-	
	ADC consumption on V_{DDA} BOOST=01, Differential mode f_{ADC}=12.5 MHz	Resolution = 16 bits	-	-	-	630	-	
		Resolution = 14 bits	-	-	-	432	-	
		Resolution = 12 bits	-	-	-	315	-	
	ADC consumption on V_{DDA} BOOST=00, Differential mode f_{ADC}=6.25 MHz	Resolution = 16 bits	-	-	-	360	-	
		Resolution = 14 bits	-	-	-	270	-	
		Resolution = 12 bits	-	-	-	225	-	
$I_{DDA–SE}$ (ADC)	ADC consumption on V_{DDA} BOOST=11, Single-endedmode	Resolution = 16 bits, f_{ADC}=25 MHz	-	-	-	720	-	
		Resolution = 14 bits, f_{ADC}=30 MHz	-	-	-	675	-	
		Resolution = 12 bits, f_{ADC}=40 MHz	-	-	-	495	-	
	ADC consumption on V_{DDA} BOOST=10, Singl-ended mode f_{ADC}=25 MHz	Resolution = 16 bits	-	-	-	540	-	
		Resolution = 14 bits	-	-	-	405	-	
		Resolution = 12 bits	-	-	-	292.5	-	
	ADC consumption on V_{DDA} BOOST=01, Single-endedmode f_{ADC}=12.5 MHz	Resolution = 16 bits	-	-	-	315	-	
		Resolution = 14 bits	-	-	-	216	-	
		Resolution = 12 bits	-	-	-	157.5	-	
	ADC consumption on V_{DDA} BOOST=00, Single-endedmode f_{ADC}=6.25 MHz	Resolution = 16 bits	-	-	-	180	-	
		Resolution = 14 bits	-	-	-	135	-	
		Resolution = 12 bits	-	-	-	112.5	-	
I_{DD} (ADC)	ADC consumption on V_{DD}	f_{ADC}=50 MHz	-	-	-	400	-	
		f_{ADC}=25 MHz	-	-	-	220	-	
		f_{ADC}=12.5 MHz	-	-	-	180	-	
		f_{ADC}=6.25 MHz	-	-	-	120	-	
		f_{ADC}=3.125 MHz	-	-	-	80	-	

1. Guaranteed by design.
2. The voltage booster on ADC switches must be used for VDDA < 2.4 V (embedded I/O switches).
3. These values are valid for UFBGA176+25 and one ADC. The values for other packages and multiple ADCs may be different.
4. Depending on the package, V_{REF+} can be internally connected to V_{DDA} and V_{REF-} to V_{SSA}.
5. The tolerance is 10 LSBs for 16-bit resolution, 4 LSBs for 14-bit resolution, and 2 LSBs for 12-bit, 10-bit and 8-bit resolutions.

Table 3.3-74: ADC characteristics(1)(2) (continued)

Resolution	RAIN (Ω)	Minimum sampling time (s)		
		Directchannels(3)	Fast channels(4)	Slow channels(5)
16 bits	47	7.37E-08	1.14E-07	1.72E-07
14 bits	47	6.29E-08	9.74E-08	1.55E-07
	68	6.84E-08	1.02E-07	1.58E-07
	100	7.80E-08	1.12E-07	1.62E-07
	150	9.86E-08	1.32E-07	1.80E-07
	220	1.32E-07	1.61E-07	2.01E-07
12 bits	47	5.32E-08	8.00E-08	1.29E-07
	68	5.74E-08	8.50E-08	1.32E-07
	100	6.58E-08	9.31E-08	1.40E-07
	150	8.37E-08	1.10E-07	1.51E-07
	220	1.11E-07	1.34E-07	1.73E-07
	330	1.56E-07	1.78E-07	2.14E-07
	470	2.16E-07	2.39E-07	2.68E-07
	680	3.01E-07	3.29E-07	3.54E-07
10 bits	47	4.34E-08	6.51E-08	1.08E-07
	68	4.68E-08	6.89E-08	1.11E-07
	100	5.35E-08	7.55E-08	1.16E-07
	150	6.68E-08	8.77E-08	1.26E-07
	220	8.80E-08	1.08E-07	1.40E-07
	330	1.24E-07	1.43E-07	1.71E-07
	470	1.69E-07	1.89E-07	2.13E-07
	680	2.38E-07	2.60E-07	2.80E-07
	1000	3.45E-07	3.66E-07	3.84E-07
	1500	5.15E-07	5.35E-07	5.48E-07
	2200	7.42E-07	7.75E-07	7.78E-07
	3300	1.10E-06	1.14E-06	1.14E-06

Table 3.3-75: Minimum sampling time vs R_{AIN}(1)(2)

Resolution	RAIN (Ω)	Minimum sampling time (s)		
		Directchannels(3)	Fast channels(4)	Slow channels(5)
8 bits	47	3.32E-08	5.10E-08	8.61E-08
	68	3.59E-08	5.35E-08	8.83E-08
	100	4.10E-08	5.83E-08	9.22E-08
	150	5.06E-08	6.76E-08	9.95E-08
	220	6.61E-08	8.22E-08	1.11E-07
	330	9.17E-08	1.08E-07	1.32E-07
	470	1.24E-07	1.40E-07	1.63E-07
	680	1.74E-07	1.91E-07	2.12E-07
	1000	2.53E-07	2.70E-07	2.85E-07
	1500	3.73E-07	3.93E-07	4.05E-07
	2200	5.39E-07	5.67E-07	5.75E-07
	3300	8.02E-07	8.36E-07	8.38E-07
	4700	1.13E-06	1.18E-06	1.18E-06
	6800	1.62E-06	1.69E-06	1.68E-06
	10000	2.36E-06	2.47E-06	2.45E-06
	15000	3.50E-06	3.69E-06	3.65E-06

1. Guaranteed by design.
2. Data valid at up to 140 °C, with a 47 pF PCB capacitor, and V_{DDA}=1.6 V.
3. Direct channels are connected to analog I/Os (PA0_C, PA1_C, PC2_C and PC3_C) to optimize ADC performance.
4. Fast channels correspond to PF3, PF5, PF7, PF9, PA6, PC4, PB1, PF11 and PF13.
5. Slow channels correspond to all ADC inputs except for the Direct and Fast channels.

Table 3.3-75: Minimum sampling time vs RAIN(1)(2) (continued)

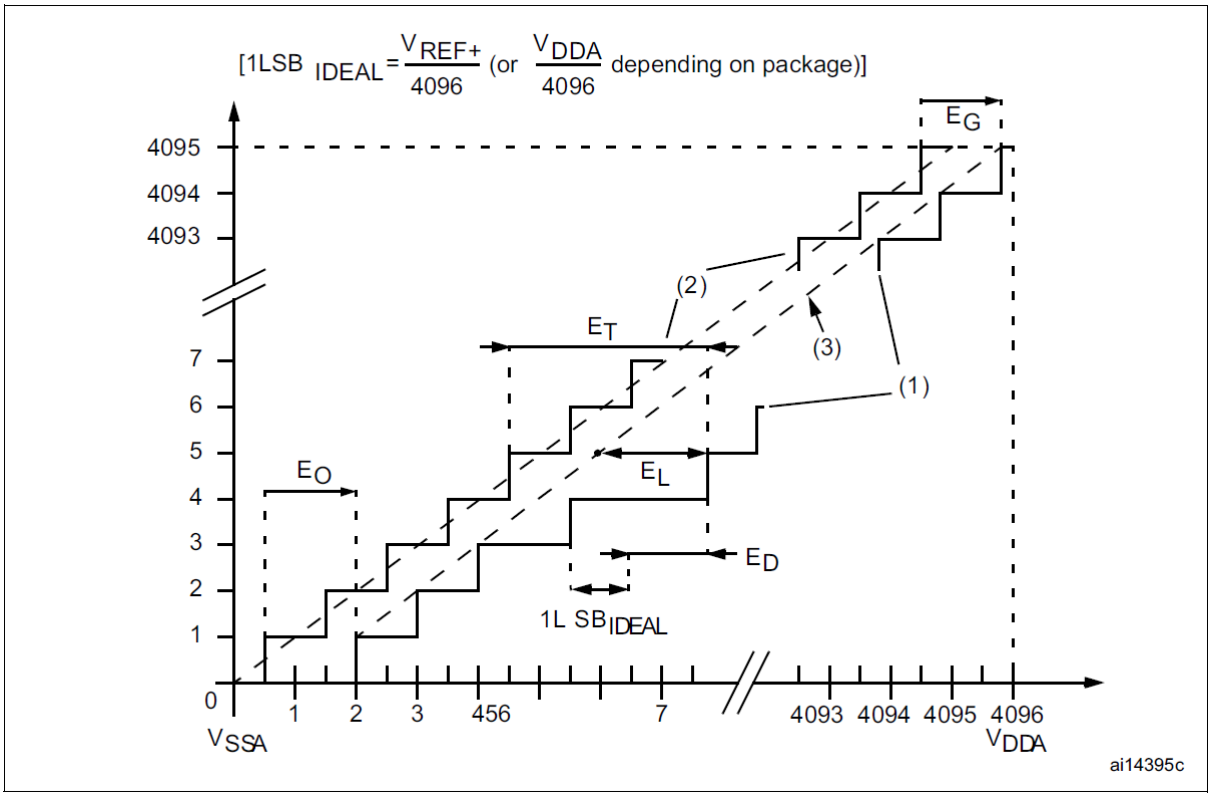
Symbol	Parameter	Conditions(3)		Min	Typ	Max	Unit
ET	Total unadjusted error	Direct channel	Single ended	-	+10/–20	-	LSB
			Differential	-	±15	-	
		Fast channel	Single ended	-	+10/–20	-	
			Differential	-	±15	-	
		Slow channel	Single ended	-	±10	-	
			Differential		±10	-	
EO	Offset error	-		-	±10	-	
EG	Gain error	-		-	±15	-	
ED	Differential linearity error	Single ended		-	+3/–1	-	
		Differential		-	+4.5/–1	-	
EL	Integral linearity error	Directchannel	Single ended	-	±11	-	
			Differential	-	±7	-	
		Fast channel	Single ended	-	±13	-	
			Differential	-	±7	-	
		Slowchannel	Single ended	-	±10	-	
			Differential	-	±6	-	
ENOB	Effective number of bits	Single ended		-	12.2	-	Bits
		Differential		-	13.2	-	
SINAD	Signal-to-noise and distortion ratio	Single ended		-	75.2	-	dB
		Differential		-	81.2	-	
SNR	Signal-to-noise ratio	Single ended		-	77.0	-	
		Differential		-	81.0	-	
THD	Total harmonic distortion	Single ended		-	87	-	
		Differential		-	90	-	

1. Data guaranteed by characterization for BGA packages. The values for LQFP packages might differ.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC clock frequency = 25 MHz, ADC resolution = 16 bits, V_{DDA}=V_{REF+}=3.3 V and BOOST=11.

Table 3.3-76: ADC accuracy(1)(2)

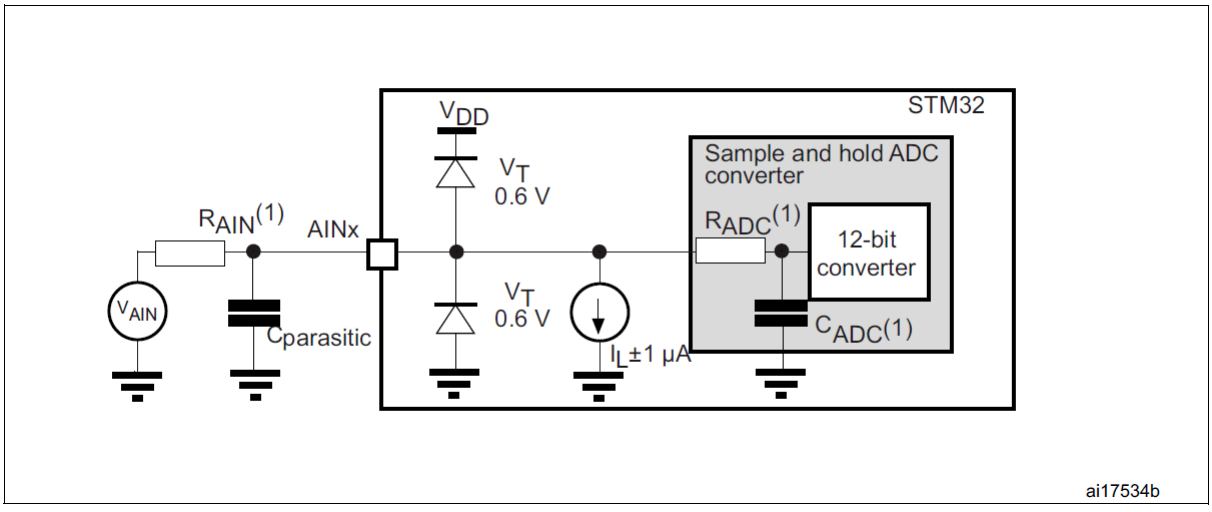
Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 3.3.15 does not affect the ADC accuracy.



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. ET = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 3.3-28: ADC accuracy characteristics (12-bitresolution)

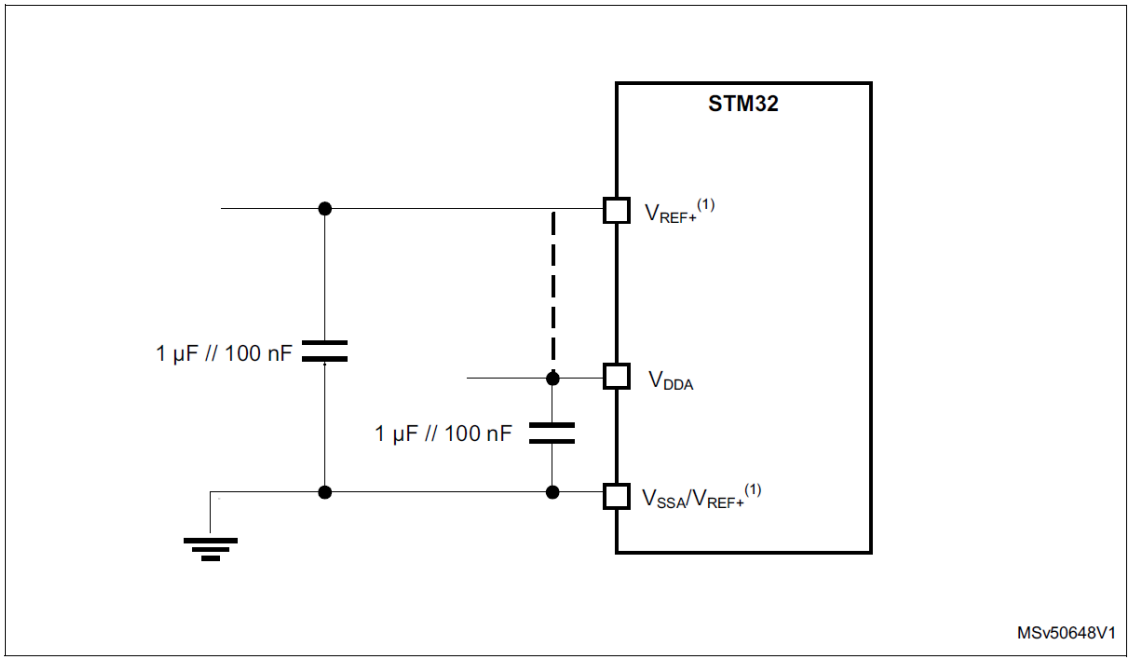


1. Refer to Table 3.3-74 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

Figure 3.3-29: Typical connection diagram using the ADC

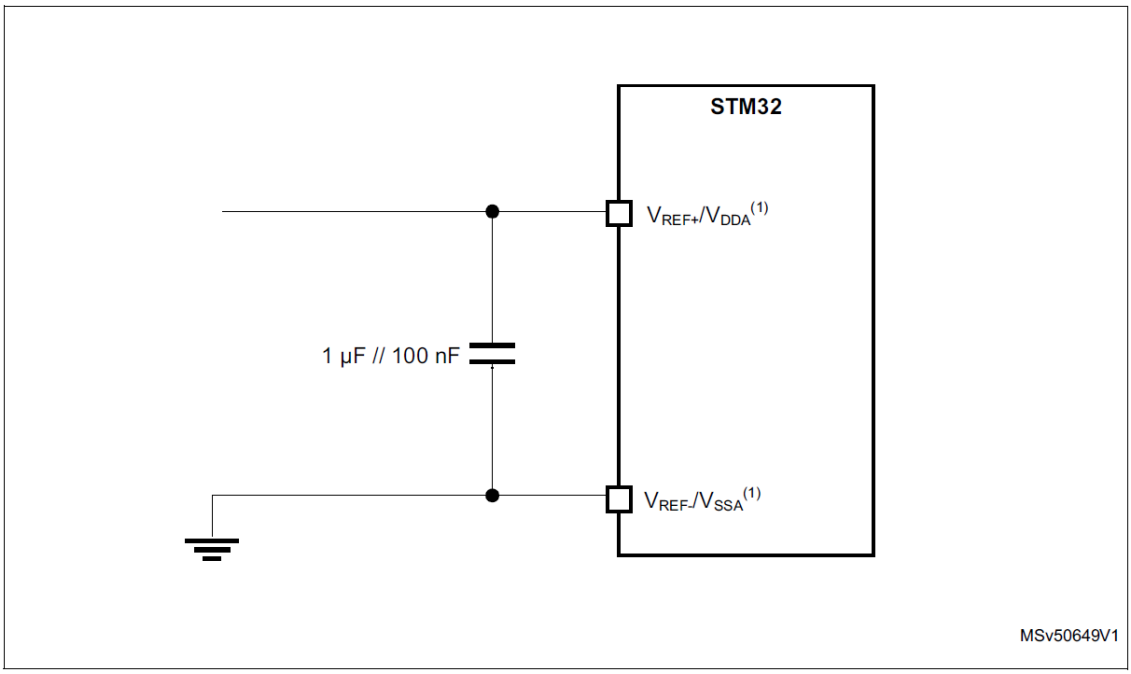
General PCB design guidelines

Power supply decoupling should be performed as shown in Figure 3.3-30 or Figure 3.3-31, depending on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.



1. V_{REF+} input is available on all package whereas the V_{REF-} s available only on UFBGA176+25 and TFBGA240+25. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA}.

Figure 3.3-30: Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} input is available on all package whereas the V_{REF-} s available only on UFBGA176+25 and TFBGA240+25. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA}.

Figure 3.3-31: Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

3.3.22 DAC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.8	3.3	3.6	V
V_{REF+}	Positive reference voltage	-		1.80	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-		-	V_{SSA}	-	
R_L	Resistive Load	DAC output buffer ON	connectedto V_{SSA}	5	-	-	kΩ
			connectedto V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		10.3	13	16	
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	V_{DD} = 2.7 V	-	-	1.6	kΩ
			V_{DD} = 2.0 V	-	-	2.6	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	V_{DD} = 2.7 V	-	-	17.8	kΩ
			V_{DD} = 2.0 V	-	-	18.7	
C_L	Capacitive Load	DAC output buffer OFF		-	-	50	pF
C_{SH}		Sample and Hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{DDA} −0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5LSB, ±1LSB, ±2LSB, ±4LSB, ±8LSB)	Normal mode, DAC output buffer ON, $C_L \le$ 50 pF, $R_L \ge 5$ kΩ	±0.5 LSB	-	2.05	-	µs
			±1 LSB	-	1.97	-	
			±2 LSB	-	1.67	-	
			±4 LSB	-	1.66	-	
			±8 LSB	-	1.65	-	
		Normal mode, DAC output buffer OFF, ±1LSB C_L=10 pF		-	1.7	2	
t_{WAKEUP}(3)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until the final value of ±1LSB is reached	Normal mode, DAC output buffer ON, $C_L \le$ 50 pF, R_L = 5 kΩ		-	5	7.5	µs
		Normal mode, DAC output buffer OFF, $C_L \le$ 10 pF			2	5	
PSRR	DC V_{DDA} supply rejection ratio	Normal mode, DAC output buffer ON, $C_L \le$ 50 pF, R_L = 5 kΩ		-	−80	−28	dB
t_{SAMP}	Sampling time in Sample and Hold mode C_L=100 nF (code transition between the lowest input code and the highest input code when DAC_OUT reaches the ±1LSB final value)	MODE<2:0>_V12=100/101 (BUFFER ON)		-	0.7	2.6	ms
		MODE<2:0>_V12=110 (BUFFER OFF)		-	11.5	18.7	
		MODE<2:0>_V12=111 (INTERNAL BUFFER OFF)		-	0.3	0.6	µs

C_{Iint}	Internal sample and hold capacitor	-		1.8	2.2	2.6	pF
t_{TRIM}	Middle code offset trim time	Minimum time to verify the each code		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	850	-	µV
		V_{REF+} = 1.8 V		-	425	-	
$I_{DDA(DAC)}$	DAC quiescent consumption from V_{DDA}	DAC output buffer ON	No load, middlecode (0x800)	-	360	-	µA
			No load, worst code (0xF1C)	-	490	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	20	-	
		Sample and Hold mode, C_{SH}=100 nF		-	360*T_{ON}/(T_{ON}+T_{OFF})(4)	-	
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middlecode (0x800)	-	170	-	
			No load, worst code (0xF1C)	-	170	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	160	-	
		Sample and Hold mode, Buffer ON, C_{SH}=100 nF (worst code)		-	170*T_{ON}/(T_{ON}+T_{OFF}) (4)	-	
		Sample and Hold mode, Buffer OFF, C_{SH}=100 nF (worst code)		-	160*T_{ON}/(T_{ON}+T_{OFF}) (4)	-	

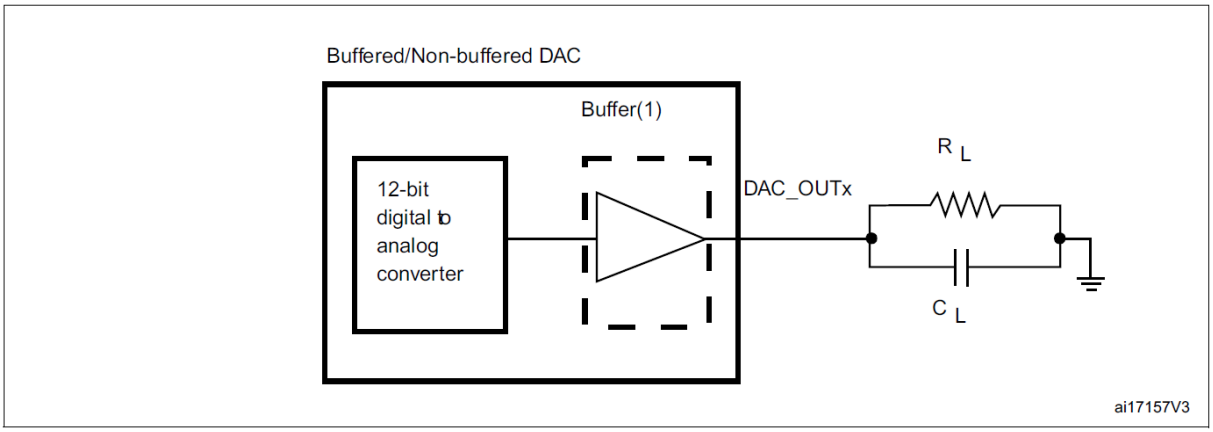
1. Guaranteed by design unless otherwise specified.
2. TBD stands for “to be defined”.
3. In buffered mode, the output can overshoot above the final value for low input code (starting from the minimum value).
4. T_{ON} is the refresh phase duration, while T_{OFF} is the hold phase duration. Refer to the product reference manual for more details.

Table 3.3-77: DAC characteristics(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity(2)	DAC output buffer ON		−2	-	2	LSB
		DAC output buffer OFF		−2	-	2	
-	Monotonicity	10 bits		-	-	-	-
INL	Integral non linearity(3)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ		−4	-	4	LSB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		−4	-	4	
Offset	Offset error at code 0x800 (3)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ	V_{REF+} = 3.6 V	-	-	±15	LSB
			V_{REF+} = 1.8 V	-	-	±30	
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±5	LSB
OffsetCal	Offset error at code 0x800 after factory calibration	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ	V_{REF+} = 3.6 V	-	-	±6	LSB
			V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ		-	-	±1	%
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±1	
SNR	Signal-to-noise ratio(6)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ , 1 KHz, BW = 500 KHz		-	67.8	-	dB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L, 1 KHz, BW = 500 KHz		-	67.8	-	
THD	Total harmonic distortion(6)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ , 1KHz		-	−78.6	-	dB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L, 1 KHz		-	−78.6	-	
SINAD	Signal-to-noise and distortion ratio(6)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ , 1KHz		-	67.5	-	dB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L, 1 KHz		-	67.5	-	
ENOB	Effective number of bits	DAC output buffer ON, CL ≤ 50 pF, RL ≥ 5 kΩ , 1 KHz		-	10.9	-	bits
		DAC output buffer OFF, CL ≤ 50 pF, no RL, 1 KHz		-	10.9	-	

1. Guaranteed by characterization.
2. Difference between two consecutive codes minus 1 LSB.
3. Difference between the value measured at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and (VREF+ - 0.2 V) when the buffer is ON.
6. Signal is −0.5dBFS with $F_{sampling}$=1 MHz.

Table 3.3-78: DAC accuracy(1)



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Figure 3.3-32: 12-bit buffered /non-buffered DAC

3.3.23 Voltage reference buffer characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	VSCALE = 000	2.8	3.3	3.6	V
			VSCALE = 001	2.4	-	3.6	
			VSCALE = 010	2.1	-	3.6	
			VSCALE = 011	1.8	-	3.6	
		Degraded mode	VSCALE = 000	1.62	-	2.80	
			VSCALE = 001	1.62	-	2.40	
			VSCALE = 010	1.62	-	2.10	
			VSCALE = 011	1.62	-	1.80	
V_{REFBUF_OUT}	Voltage Reference Buffer Output, at 30 °C, I_{load}= 100 µA	Normal mode	VSCALE = 000	2.498	2.5	2.5035	
			VSCALE = 001	2.046	2.049	2.052	
			VSCALE = 010	1.801	1.804	1.806	
			VSCALE = 011	1.4995	1.5015	1.504	
		Degraded mode(2)	VSCALE = 000	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 001	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 010	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 011	V_{DDA}– 150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
C_L	Load capacitor	-	-	0.5	1	1.50	uF
esr	Equivalent Serial Resistor of C_L	-	-	-	-	2	Ω

I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	-	ppm/V
			I_{load} = 4 mA	-	100	-	
I_{load_reg}	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal Mode	-	50	-	ppm/mA
T_{coeff}	Temperature coefficient	−40 °C < T_J < +125 °C		-	-	T_{coeff} V_{REFINT} + 100	ppm/ °C
PSRR	Power supply rejection	DC	-	-	60	-	dB
		100KHz	-	-	40	-	
t_{START}	Start-up time	C_L=0.5 µF	-	-	300	-	µs
		C_L=1 µF	-	-	500	-	
		C_L=1.5 µF	-	-	650	-	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase(3)	-		-	8	-	mA
$I_{DDA(VREFBUF)}$	VREFBUF consumption from V_{DDA}	I_{LOAD} = 0 µA	-	-	15	25	µA
		I_{LOAD} = 500 µA	-	-	16	30	
		I_{LOAD} = 4 mA	-	-	32	50	

1. Guaranteed by design.
2. In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage (V_{DDA}−drop voltage).
3. To properly control VREFBUF IINRUSH current during the startup phase and the change of scaling, V_{DDA} voltage should be in the range of 1.8 V-3.6 V, 2.1 V-3.6 V, 2.4 V-3.6 V and 2.8 V-3.6 V for VSCALE = 011, 010, 001 and 000, respectively.

Table 3.3-79: VREFBUF characteristics(1)

3.3.24 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T^{(1)}{}_L$	V_{SENSE} linearity with temperature	-	-	3	°C
Avg_Slope(2)	Average slope	-	2	-	mV/°C
V_{30}(3)	Voltage at 30°C ± 5 °C	-	0.62	-	V
t_{start_run}	Startup time in Run mode (buffer startup)	-	-	25.2	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	
I_{sens}(1)	Sensor consumption	-	0.18	0.31	µA
$I_{sensbuf}$(1)	Sensor buffer consumption	-	3.8	6.5	

1. Guaranteed by design.
2. Guaranteed by characterization.
3. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.

Table 3.3-80: Temperature sensor characteristics

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 30 °C, V_{DDA}=3.3 V	0x1FF1 E820 -0x1FF1 E821
TS_CAL2	Temperature sensor raw data acquired value at 110 °C, V_{DDA}=3.3 V	0x1FF1 E840 - 0x1FF1 E841

Table 3.3-81: Temperature sensor calibration values

3.3.25 Temperature and V_{BAT} monitoring

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	26	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	–10	-	+10	%
t_{S_vbat}(1)	ADC sampling time when reading V_{BAT} input	9	-	-	µs
$V_{BAThigh}$	High supply monitoring	-	3.55	-	V
V_{BATlow}	Low supply monitoring	-	1.36	-	

1. Guaranteed by design.

Table 3.3-82: V_{BAT} monitoring characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS in PWR_CR3= 0	-	5	-	KΩ
		VBRS in PWR_CR3= 1		1.5	-	

Table 3.3-83: V_{BAT} charging characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	-	117	-	°C
$TEMP_{low}$	Low temperature monitoring	-	–25	-	

Table 3.3-84: Temperature monitoring characteristics

3.3.26 Voltage booster for analog switch

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	-	1.62	2.6	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	1.62 V ≤ V_{DD} ≤ 2.7 V	-	-	125	µA
		2.7 V < V_{DD} < 3.6 V	-	-	250	

1. Guaranteed by characterization results.

Table 3.3-85: Voltage booster for analog switch characteristics(1)

3.3.27 Comparator characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	3.3	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}	Scaler input voltage	-		(2)			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	0.2	0.3	µA
		BRG_EN=1 (bridge enable)		-	0.8	1	
t_{START_SCALER}	Scaler startup time	-		-	140	250	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode		-	2	5	µs
		Medium mode		-	5	20	
		Ultra-low-power mode		-	15	80	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode		-	50	80	ns
		Medium mode		-	0.5	1.2	µs
		Ultra-low-power mode		-	2.5	7	
	Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs	High-speed mode		-	50	120	ns
		Medium mode		-	0.5	1.2	µs
		Ultra-low-power mode		-	2.5	7	
V_{offset}	Comparator offset error	Full common mode range		-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		5	10	22	
		Medium hysteresis		8	20	37	
		High hysteresis		16	30	52	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 KHz ±100 mV overdrive square signal	-	800	-	
		Medium mode	Static	-	5	7	µA
			With 50 KHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 KHz ±100 mV overdrive square signal	-	75	-	

1. Guaranteed by design, unless otherwise specified.
2. Refer to Table 3.3-8: Embedded reference voltage.
3. Guaranteed by characterization results.

Table 3.3-86: COMP characteristics(1)

3.3.28 Operational amplifier characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage Range	-	2	3.3	3.6	V
CMIR	Common Mode Input Range	-	0	-	V_{DDA}	
VI_{OFFSET}	Input offset voltage	25°C, no load on output	-	-	±1.5	mV
		All voltages and temperature, no load	-	-	±2.5	
ΔVI_{OFFSET}	Input offset voltage drift	-	-	±3.0	-	µV/°C
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage ($0.1*V_{DDA}$)	-	-	1.1	1.5	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage ($0.9*V_{DDA}$)	-	-	1.1	1.5	
I_{LOAD}	Drive current	-	-	-	500	µA
I_{LOAD_PGA}	Drive current in PGA mode	-	-	-	270	
C_{LOAD}	Capacitive load	-	-	-	50	pF
CMRR	Common mode rejection ratio	-	-	80	-	dB
PSRR	Power supply rejection ratio	$C_{LOAD} \le 50pf$ / $R_{LOAD} \ge 4$ kΩ(1) at 1 KHz, $V_{com}=V_{DDA}/2$	50	66	-	dB
GBW	Gain bandwidth for high supply range	200 mV ≤ Output dynamic range ≤ V_{DDA} - 200 mV	4	7.3	12.3	MHz
SR	Slew rate (from 10% and 90% of output voltage)	Normal mode	-	3	-	V/µs
		High-speed mode	-	30	-	
AO	Open loop gain	200 mV ≤ Output dynamic range ≤ V_{DDA} - 200 mV	59	90	129	dB
φm	Phase margin	-	-	55	-	°
GM	Gain margin	-	-	12	-	dB
V_{OHSAT}	High saturation voltage	I_{load}=max or R_{LOAD}=min, Input at V_{DDA}	V_{DDA} −100 mV	-	-	mV
V_{OLSAT}	Low saturation voltage	I_{load}=max or R_{LOAD}=min, Input at 0 V	-	-	100	
t_{WAKEUP}	Wake up time from OFF state	Normal mode: $C_{LOAD} \le 50pf$, $R_{LOAD} \ge 4$ kΩ, follower configuration	-	0.8	3.2	µs
		High speed mode: $C_{LOAD} \le 50pf$, $R_{LOAD} \ge 4$ kΩ, follower configuration	-	0.9	2.8	
PGA gain	Non inverting gain error value	PGA gain = 2	−1	-	1	%
		PGA gain = 4	−2	-	2	

		PGA gain = 8		−2.5	-	2.5	
		PGA gain = 16		−3	-	3	
	Inverting gain error value	PGA gain = 2		−1	-	1	
		PGA gain = 4		−1	-	1	
		PGA gain = 8		−2	-	2	
		PGA gain = 16		−3	-	3	
	External non-inverting gain error value	PGA gain = 2		−1	-	1	
		PGA gain = 4		−3	-	3	
		PGA gain = 8		−3.5	-	3.5	
		PGA gain = 16		−4	-	4	
$R_{network}$	R2/R1 internal resistance values in non-inverting PGA mode(2)	PGA Gain=2		-	10/10	-	kΩ/kΩ
		PGA Gain=4		-	30/10	-	
		PGA Gain=8		-	70/10	-	
		PGA Gain=16		-	150/10	-	
	R2/R1 internal resistance values in inverting PGA mode(2)	PGA Gain = -1		-	10/10	-	
		PGA Gain = -3		-	30/10	-	
		PGA Gain = -7		-	70/10	-	
		PGA Gain = -15		-	150/10	-	
Delta R	Resistance variation (R1 or R2)	-		−15	-	15	%
PGA BW	PGA bandwidth for different non inverting gain	Gain=2		-	GBW/2	-	MHz
		Gain=4		-	GBW/4	-	
		Gain=8		-	GBW/8	-	
		Gain=16		-	GBW/16	-	
	PGA bandwidth for different inverting gain	Gain = -1		-	5.00	-	MHz
		Gain = -3		-	3.00	-	
		Gain = -7		-	1.50	-	
		Gain = -15		-	0.80	-	
en	Voltage noise density	at 1 KHz	output loaded with 4 kΩ	-	140	-	nV/√Hz
		at 10 KHz		-	55	-	
$I_{DDA(OPAMP)}$	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode, follower	-	570	1000	µA
		High-speed mode		-	610	1200	

1. R_{LOAD} is the resistive load connected to VSSA or to VDDA.
2. R2 is the internal resistance between the OPAMP output and th OPAMP inverting input. R1 is the internal resistance between the OPAMP inverting input and ground. PGA gain = 1 + R2/R1.

Table 3.3-87: Operational amplifier characteristics

3.3.29 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in Table 3.3-88 for DFSDM are derived from tests performed under the ambient temperature, fPCLKx frequency and supply voltage conditions summarized in Table 3.3-1: General operating conditions.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS1

Refer to Section 3.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (DìFSDM_CKINx, DFSDM_DATINx, DFSDM_CKOUT for DFSDM).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	$1.62 < V_{DD} < 3.6$ V	-	-	133	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $1.62 < V_{DD} < 3.6$ V	-	-	20	
		SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $2.7 < V_{DD} < 3.6$ V	-	-	20	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]¹0), $1.62 < V_{DD} < 3.6$ V	-	-	20	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]¹0), $2.7 < V_{DD} < 3.6$ V	-	-	20	
f_{CKOUT}	Output clock frequency	$1.62 < V_{DD} < 3.6$ V	-	-	20	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	$1.62 < V_{DD} < 3.6$ V	45	50	55	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $1.62 < V_{DD} < 3.6$ V	$T_{CKIN}/2$-0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $1.62 < V_{DD} < 3.6$ V	1.5	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $1.62 < V_{DD} < 3.6$ V	0.5	-	-	

$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]≠0), $1.62 < V_{DD} < 3.6$ V	(CKOUTDIV+1) * $T_{DFSDMCLK}$	-	(2*CKOUTDIV) * $T_{DFSDMCLK}$	

Table 3.3-88: DFSDM measured timing 1.62-3.6 V

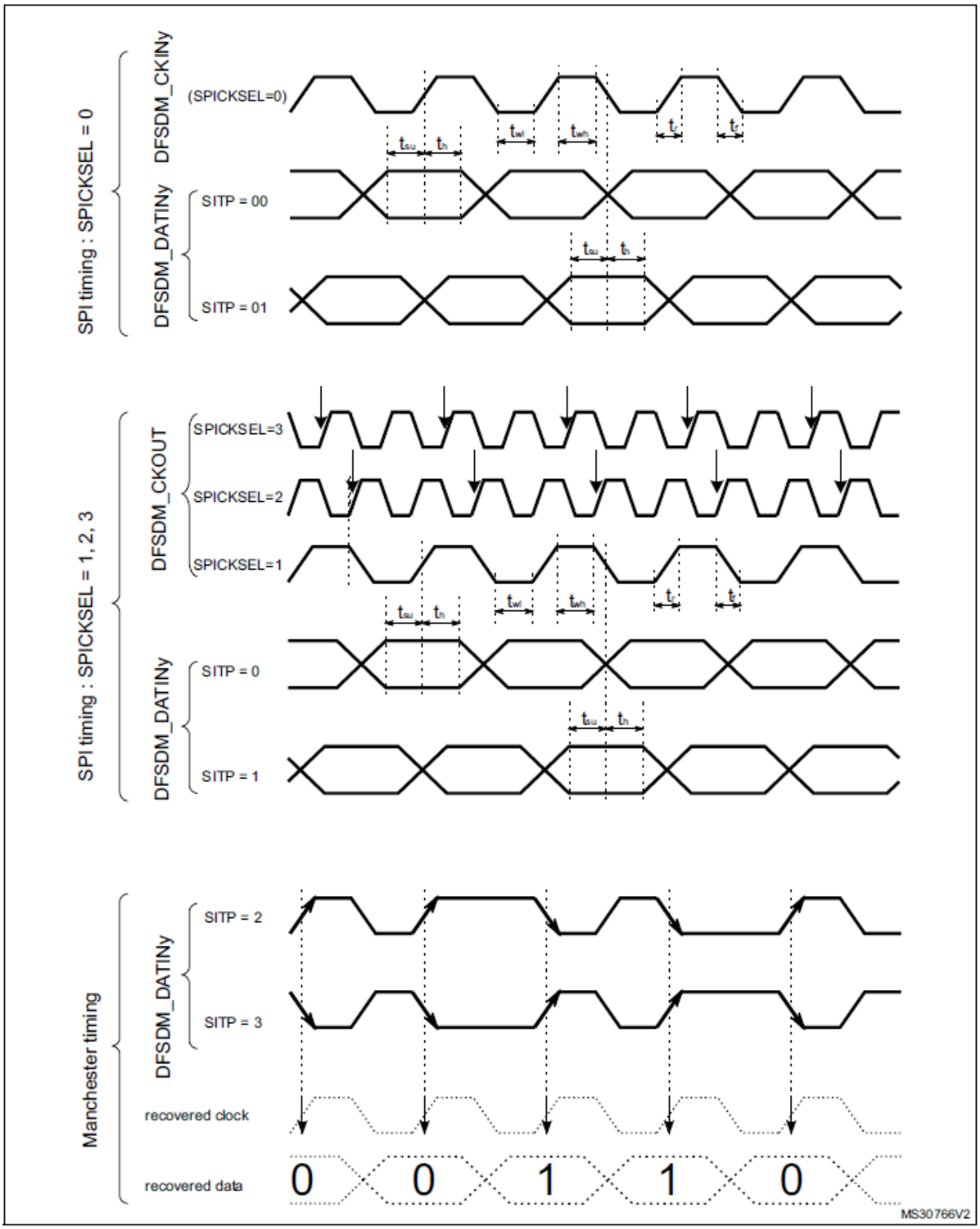


Figure 3.3-33: Channel transceiver timing diagrams

3.3.30 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in Table 3.3-89 for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in Table 3.3-1: General operating conditions, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS1

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	-
DCMI_PIXCLK	Pixel Clock input	-	80	MHz
D_{pixel}	Pixel Clock input duty cycle	30	70	%
$t_{su(}$DATA)	Data input setup time	3	-	-
t_h(DATA)	Data hold time	1	-	
tsu(HSYNC), tsu(VSYNC)	DCMI_HSYNC/ DCMI_VSYNC input setup time	2	-	ns
th(HSYNC), th(VSYNC)	DCMI_HSYNC/ DCMI_VSYNC input hold time	1	-	-

1. Guaranteed by characterization results.

Table 3.3-89: DCMI characteristics(1)

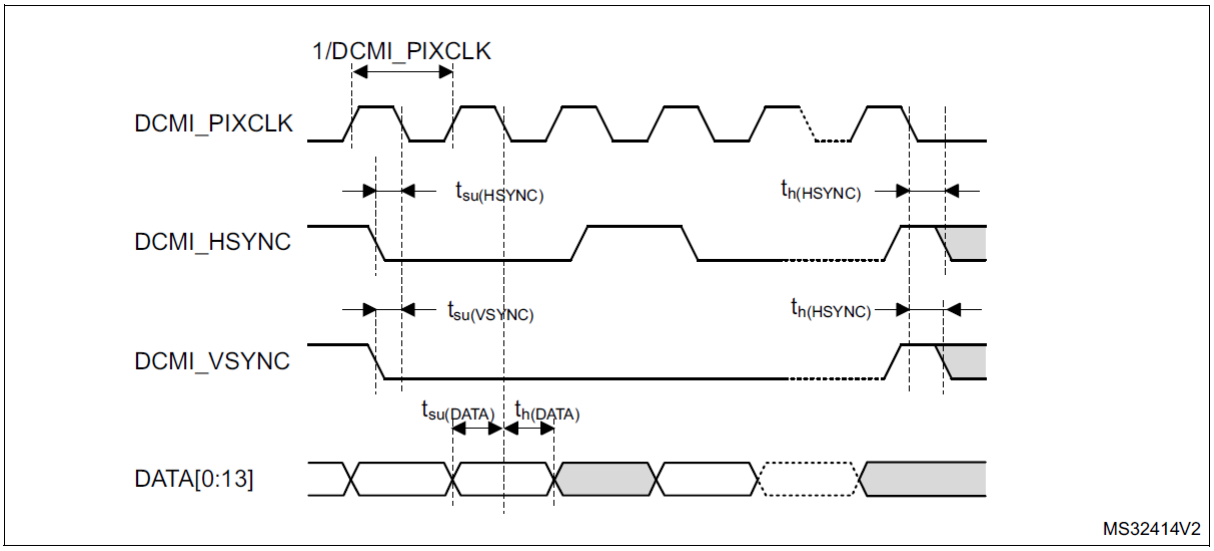


Figure 3.3-34: DCMI timing diagram

3.3.31 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in Table 3.3-90 for LCD-TFT are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in Table 3.3-1: General operating conditions, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: 0.5VDD
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS1

Symbol	Parameter		Min	Max	Unit
f_{CLK}	LTDC clock output frequency	2.7<V_{DD}<3.6 V 20pF	-	150	MHz
		2.7<V_{DD}<3.6 V		133	
		1.62<V_{DD}<3.6 V		90	
D_{CLK}	LTDC clock output duty cycle		45	55	%
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock High time, low time		$t_{w(CLK)}$//2-0.5	$t_{w(CLK)}$//2+0.5	-
$t_{v(DATA)}$	Data output valid time	2.7<V_{DD}<3.6 V	-	0.5	
$t_{h(DATA)}$		1.62<V_{DD}<3.6 V		5	
$t_{v(DATA)}$	Data output hold time		0	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time	2.7<V_{DD}<3.6 V	-	0.5	
		1.62<V_{DD}<3.6 V	-	5	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC/VSYNC/DE output hold time		0	-	

1. Guaranteed by characterization results.

Table 3.3-90: LTDC characteristics(1)

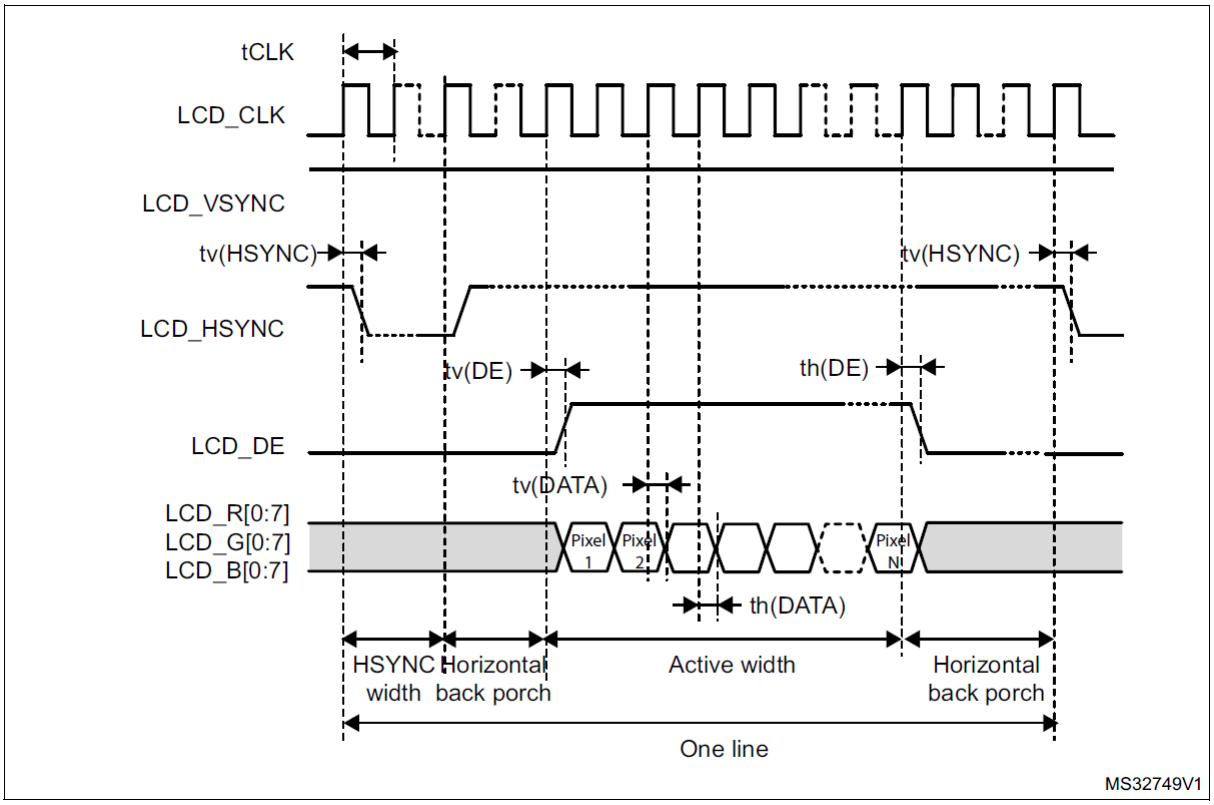


Figure 3.3-35: LCD-TFT horizontal timing diagram

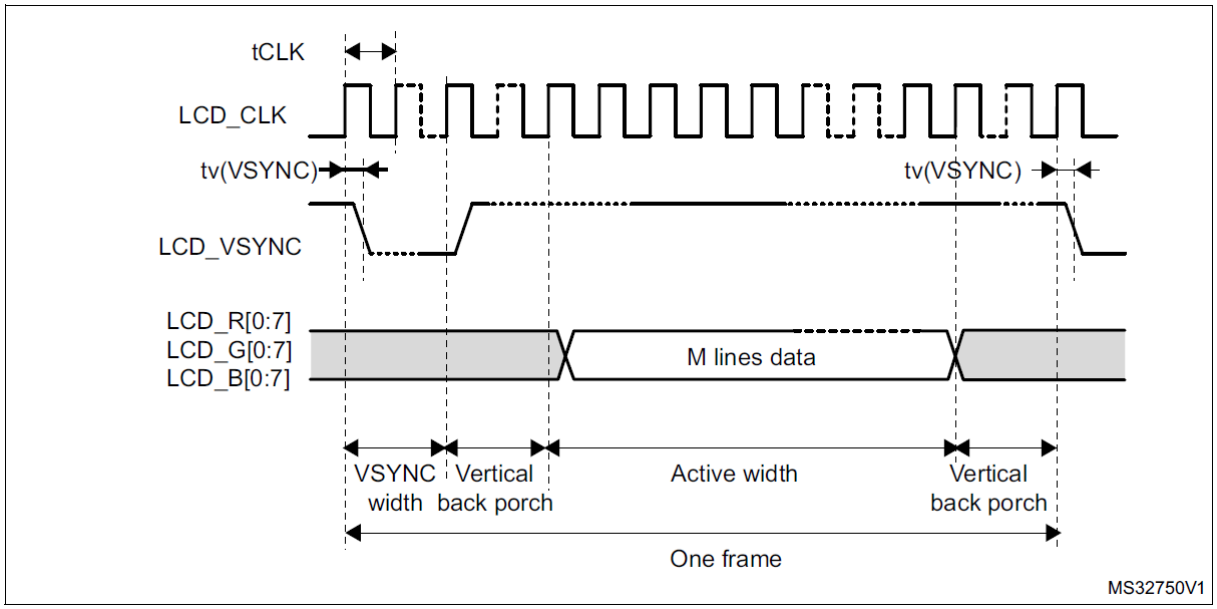


Figure 3.3-36: LCD-TFT vertical timing diagram

3.3.32 Timer characteristics

The parameters given in Table 3.3-91 are guaranteed by design.
Refer to Section 3.3.16: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Symbol	Parameter	Conditions(3)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 240 MHz	1	-	$t_{TIMxCLK}$
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 120 MHz	1	-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 240 MHz	0	$f_{TIMxCLK}/2$	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$

1. TIMx is used as a general term to refer to the TIM1 to TIM17 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 240 MHz, by setting the TIMPRE bit in the RCC_CFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = rcc_hclk1, otherwise TIMxCLK = 4x $F_{rcc\_pclkx\_d2}$.

Table 3.3-91: TIMx characteristics(1)(2)

3.3.33 Communication interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual revision 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I²C timings requirements are guaranteed by design when the I²C peripheral is properly configured and when the i2c_ker_ck frequency is greater than the minimum shown in the table below:

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog Filtre ON DNF=0	8	
			Analog Filtre OFF DNF=1	9	
		Fast-mode Plus	Analog Filtre ON DNF=0	17	
			Analog Filtre OFF DNF=1	16	-

Table 3.3-92: Minimum i2c_ker_ck frequency in all I²C modes

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but still present.
- The 20 mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load C_{Load} supported in Fm+, which is given by these formulas:

  $tr_{(SDA/SCL)}=0.8473xR_PxC_{Load}$
  $R_{P(min)}= (V_{DD}-V_{OL(max)})/I_{OL(max)}$

  Where R_P is the I^2C lines pull-up. Refer to Section 3.3.16: I/O port characteristics for the I^2C I/Os characteristics.

All I^2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by analog filter	50(2)	80(3)	ns

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered.

Table 3.3-93: I^2C analog filter characteristics(1)

USART interface characteristics

Unless otherwise specified, the parameters given in Table 3.3-94 for USART are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 3.3-1: General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- VOS level set to VOS1

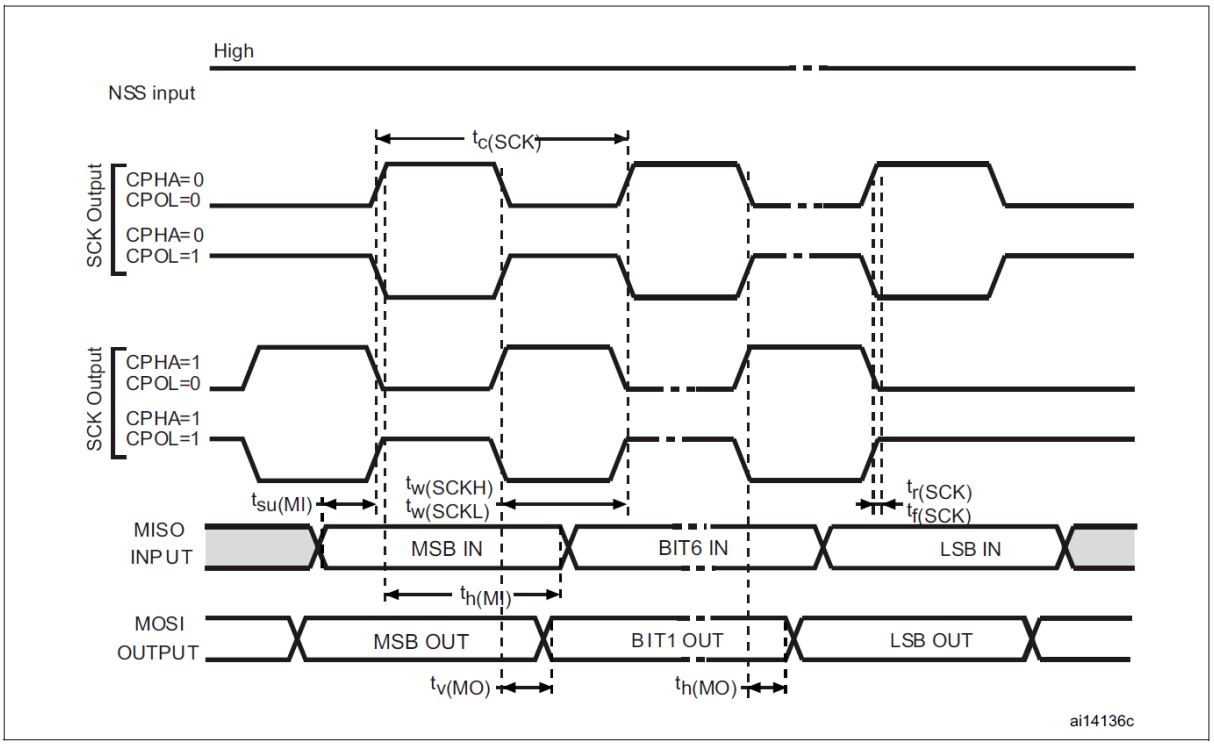
Refer to Section 3.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode	-	-	12.5	MHz
		Slave mode			25	
$t_{su(NSS)}$	NSS setup time	Slave mode	$t_{ker}+1$	-	-	-
$t_{h(NSS)}$	NSS hold time	Slave mode	2	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	CK high and low time	Master mode	$1/f_{CK}/2-2$	$1/f_{CK}/2$	$1/f_{CK}/2+2$	
$t_{su(RX)}$	Data input setup time	Master mode	$t_{ker}+6$	-	-	ns
		Slave mode	1.5	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0	-	-	
		Slave mode	1.5	-	-	

$t_{v(TX)}$	Data output valid time	Slave mode	-	12	20
		Master mode	-	0.5	1
$t_{h(TX)}$	Data output hold time	Slave mode	9	-	-
		Master mode	0	-	-

1. Guaranteed by characterization results.

Table 3.3-94: USART characteristics(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 3.3-37: USART timing diagram in Master mode

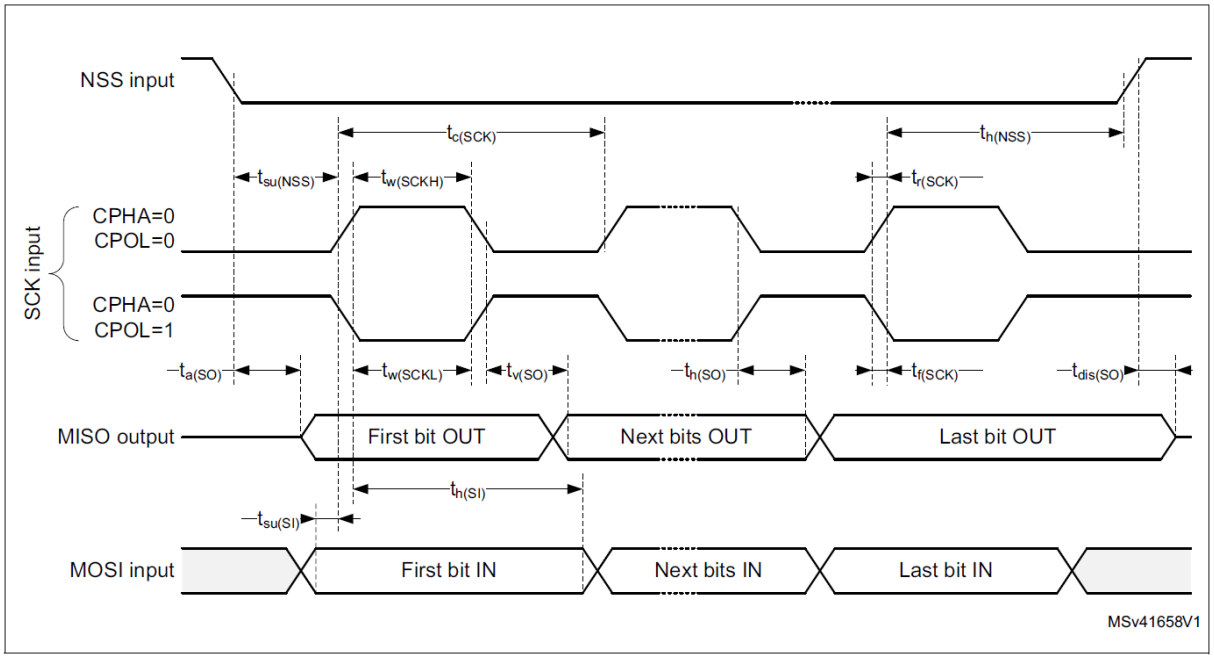


Figure 3.3-38: USART timing diagram in Slave mode

SPI interface characteristics

Unless otherwise specified, the parameters given in Table 3.3-95 for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 3.3-1: General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS1

Refer to Section 3.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode $1.62<V_{DD}<3.6$ V SPI1, 2, 3	-	-	80	MHz
		Master mode $2.7<V_{DD}<3.6$ V SPI1, 2, 3			100	
		Master mode $1.62<V_{DD}<3.6$ V SPI4, 5, 6			50	
		Slave receiver mode $1.62<V_{DD}<3.6$ V			100	

		Slave mode transmitter/full duplex 2.7<V_{DD}<3.6 V			31	
		Slave mode transmitter/full duplex 1.62 <V_{DD}<3.6 V			29	
$t_{su(NSS)}$	NSS setup time	Slave mode	2	-	-	-
$t_{h(NSS)}$	NSS hold time	Slave mode	1	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{PCLK}-2	T_{PCLK}	T_{PCLK}+2	
$t_{su(MI)}$	Data input setup time	Master mode	1	-	-	ns
$t_{su(SI)}$		Slave mode	1	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	-	
$t_{h(SI)}$		Slave mode	2	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	13	27	
$t_{dis(SO)}$	Data output disable time	Slave mode	0	1	5	
$t_{v(SO)}$	Data output valid time	Slave mode 2.7<V_{DD}<3.6 V	-	12.5	16	
		Slave mode 1.62<V_{DD}<3.6 V	-	12.5	17	
$t_{v(MO)}$		Master mode	-	1	3	
$t_{h(SO)}$	Data output hold time	Slave mode 1.62<V_{DD}<3.6 V	10	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.

Table 3.3-95: SPI characteristics(1)

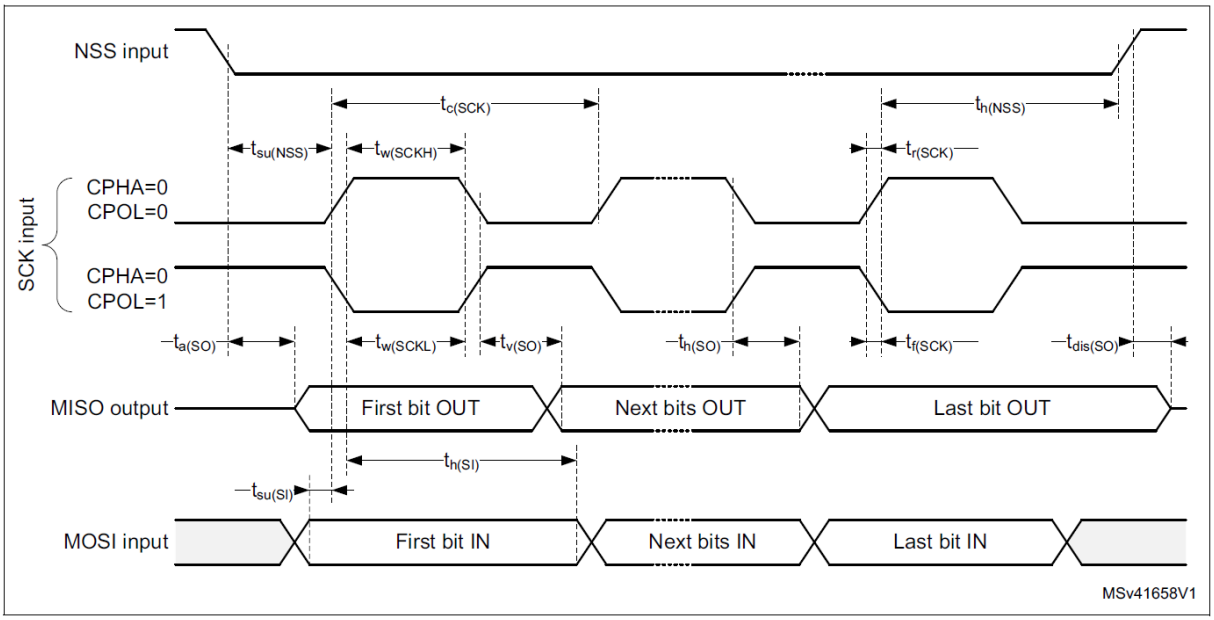
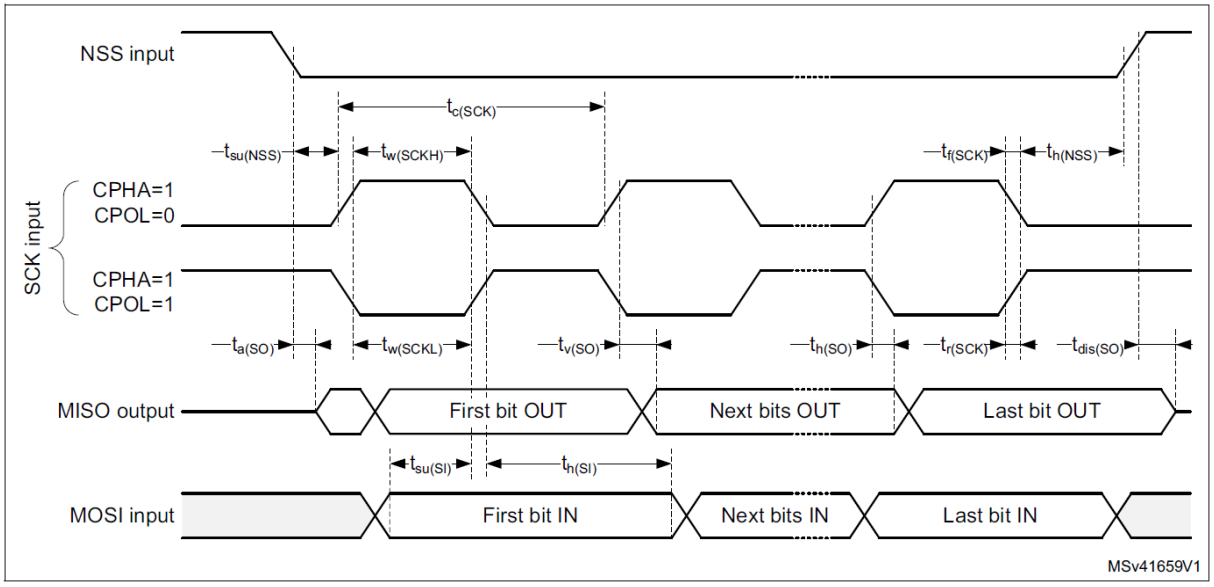
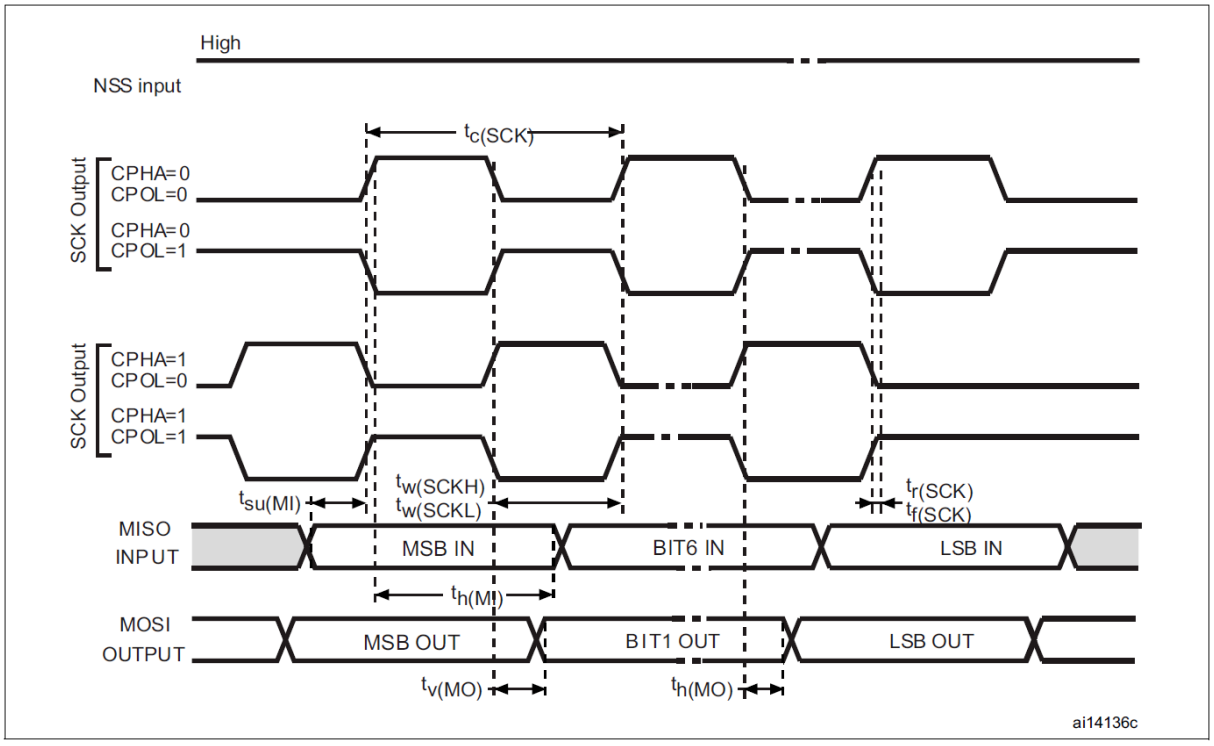


Figure 3.3-39: SPI timing diagram - slave mode and CPHA = 0



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 3.3-40: SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 3.3-41: SPI timing diagram - master mode(1)

I2S Interface characteristics

Unless otherwise specified, the parameters given in Table 3.3-96 for I^2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 3.3-1: General operating conditions, with the following configuration:

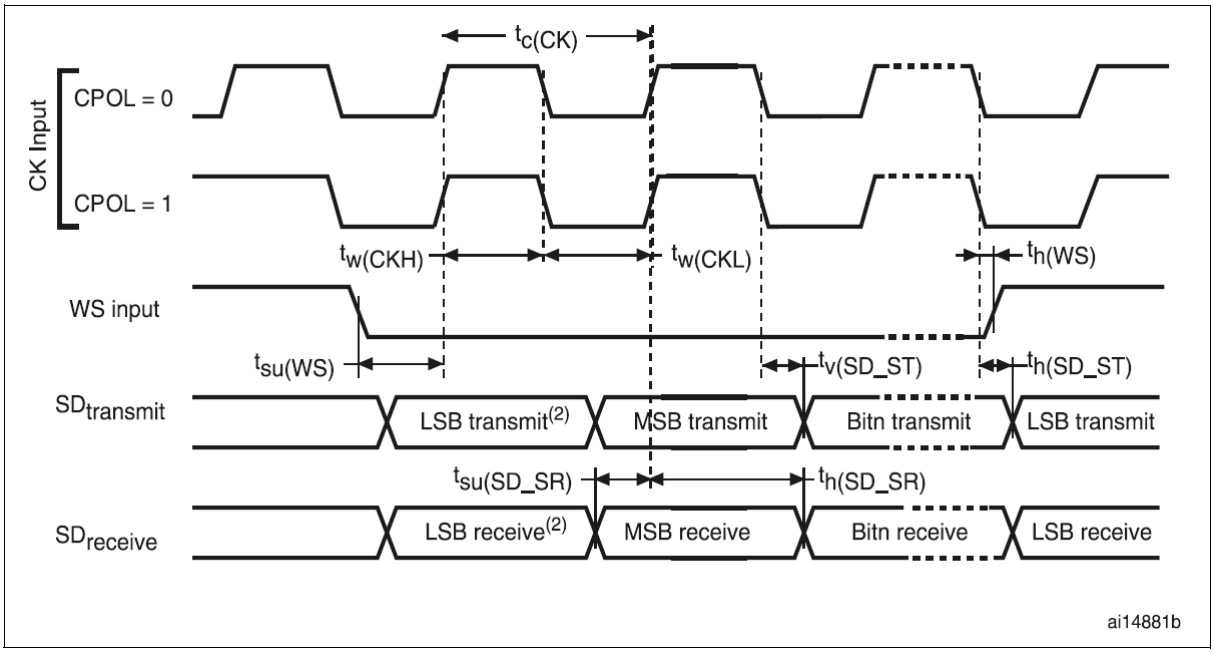
- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS1

Refer to Section 3.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (CK,SD,WS).

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I^2S main clock output	-	256x8K	$256F_S$	MHz
f_{CK}	I^2S clock frequency	Master data	-	$64F_S$	MHz
		Slave data	-	$64F_S$	
$t_{v(WS)}$	WS valid time	Master mode	-	3	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	
$t_{h(WS)}$	WS hold time	Slave mode	1	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	4	-	
$t_{h(SD\_SR)}$		Slave receiver	2	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	17	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	3	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

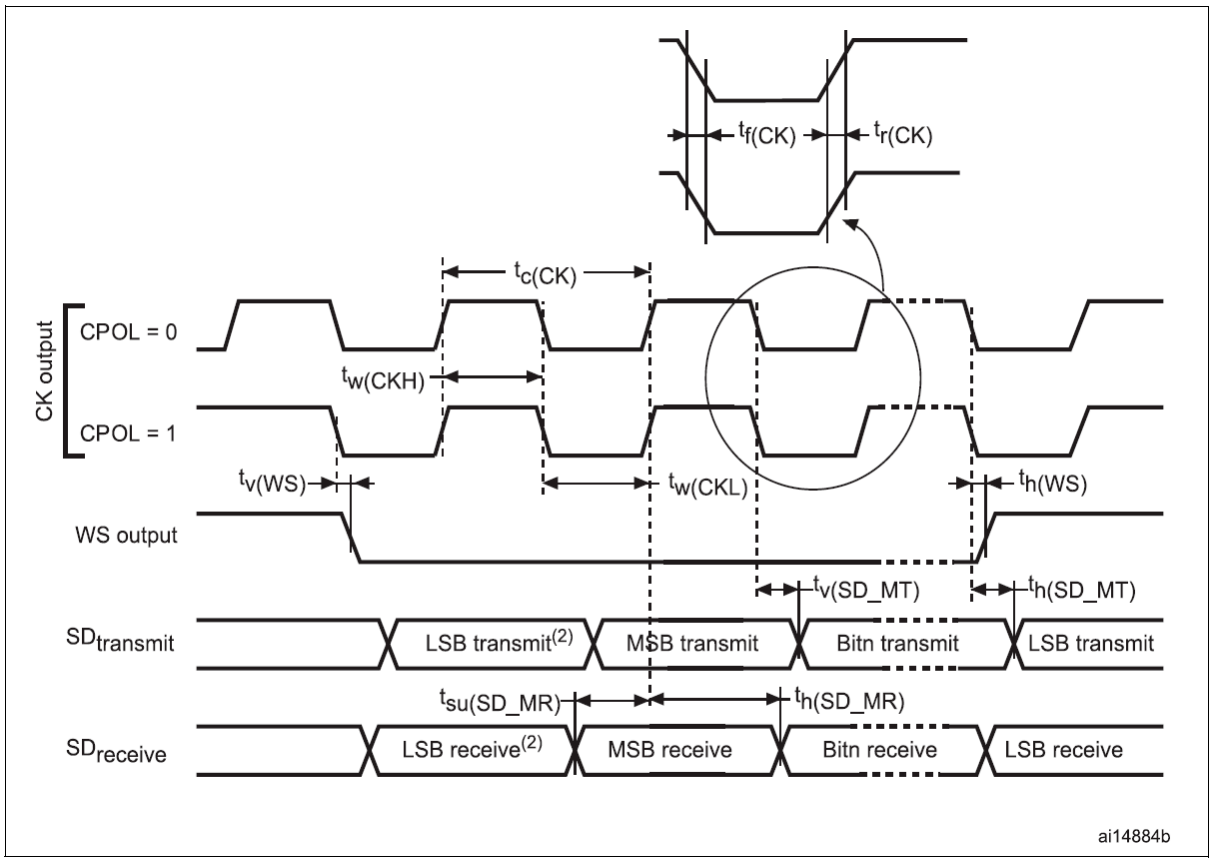
1. Guaranteed by characterization results.

Table 3.3-96: I^2S dynamic characteristics(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 3.3-42: I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 3.3-43: I²S master timing diagram (Philips protocol)(1)

SAI characteristics

Unless otherwise specified, the parameters given in Table 3.3-97 for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in Table 3.3-1: General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- IO Compensation cell activated.
- Measurement points are done at CMOS levels: 0.5VDD
- VOS level set to VOS1.

Refer to Section 3.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (SCK,SD,WS).

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI Main clock output	-	256x8K	$256xF_S$	MHz
f_{CK}	SAI clock frequency(2)	Master Data: 32 bits	-	$128xF_S$(3)	
		Slave Data: 32 bits	-	$128xF_S$(3)	
$t_{v(FS)}$	F_S valid time	Master mode $2.7 \le V_{DD} \le 3.6$	-	13	ns
		Master mode $1.62 \le V_{DD} \le 3.6$	-	20	
$t_{su(FS)}$	F_S hold time	Master mode	8	-	
$t_{h(FS)}$	F_S setup time	Slave mode	1	-	
	F_S hold time	Slave mode	1	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	0.5	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	2	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) $2.7 \le V_{DD} \le 3.6$	-	14	
		Slave transmitter (after enable edge) $1.62 \le V_{DD} \le 3.6$	-	20	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) $2.7 \le V_{DD} \le 3.6$	-	12	
		Master transmitter (after enable edge) $1.62 \le V_{DD} \le 3.6$	-	19	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	7.5	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With F_S=192 KHz.

Table 3.3-97: SAI characteristics(1)

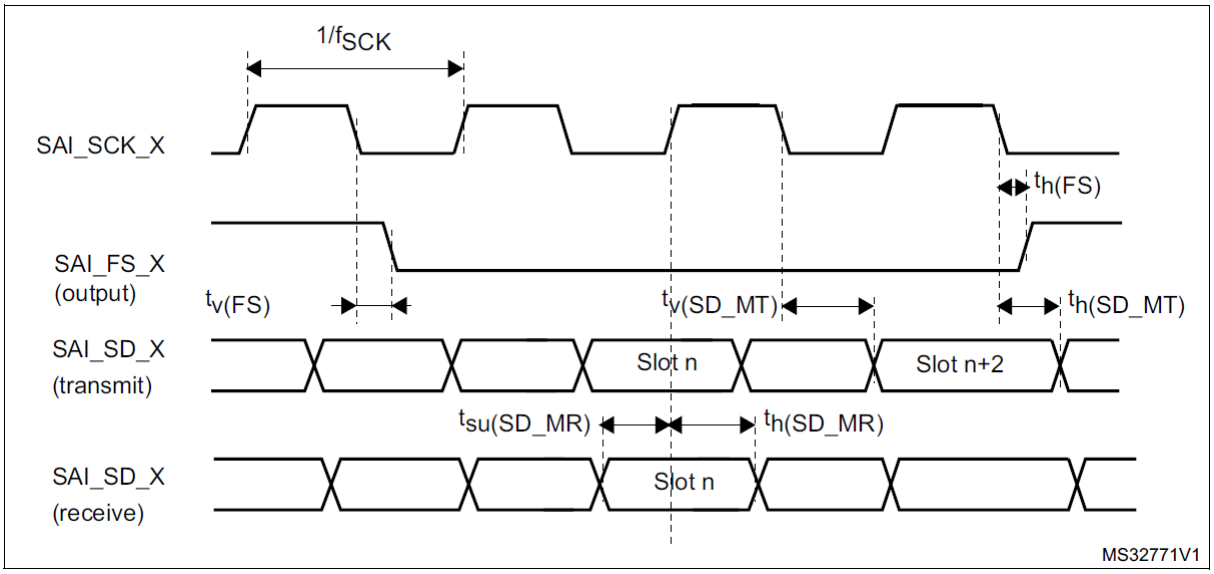


Figure 3.3-44: SAI master timing waveforms

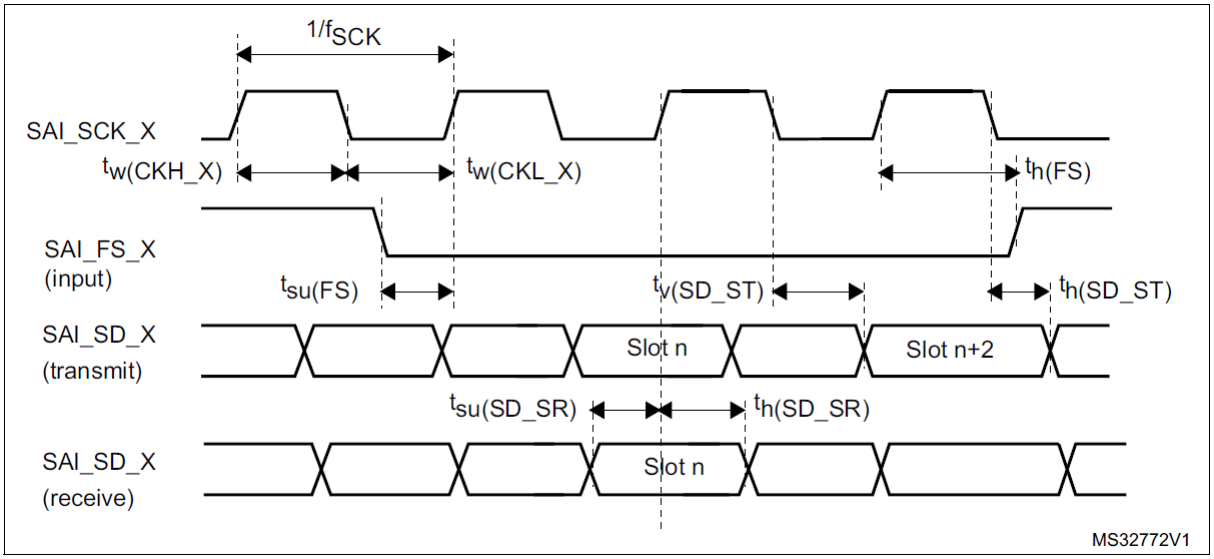


Figure 3.3-45: SAI slave timing waveforms

MDIO characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F_{MDC}	Management Data Clock	-	-	30	MHz
$t_{d(MDIO)}$	Management Data Iput/output output valid time	8	10	19	ns
$t_{su(MDIO)}$	Management Data Iput/output setup time	1	-	-	
$t_{h(MDIO)}$	Management Data Iput/output hold time	1	-	-	

Table 3.3-98: MDIO Slave timing parameters

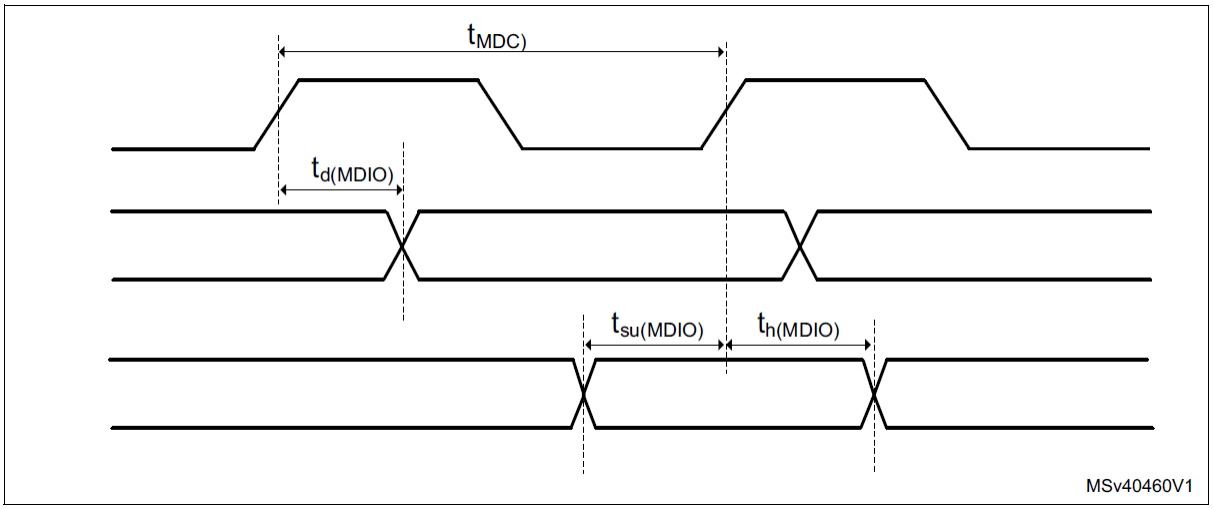


Figure 3.3-46: MDIO Slave timing diagram

SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in Table 3.3-99 and Table 3.3-100 for SDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage summarized in Table 3.3-1: General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x11
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: 0.5VDD
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS1

Refer to Section 3.3.16: I/O port characteristics for more details on the input/output characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	133	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} =52MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} =52MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(3)/DDR(3) mode						
t_{ISU}	Input setup time HS	-	1.5	-	-	ns
t_{IH}	Input hold time HS	-	1.5	-	-	
t_{IDW}(4)	Input valid window (variable window)	-	3	-	-	-
CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR/DDR(3) mode						
t_{OV}	Output valid time HS	-	-	3.5	5	ns
t_{OH}	Output hold time HS	-	2	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	-	1.5		-	ns

t_{IHD}	Input hold time SD	-	1.5		-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	-	-	0.5	2	ns
t_{OHD}	Output hold default time SD	-	0	-	-	

1. Guaranteed by characterization results.
2. Above 100 MHz, C_L = 20 pF.
3. An external voltage converter is required to support SD 1.8 V.
4. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Table 3.3-99: Dynamics characteristics: SD / MMC characteristics, V_{DD}=2.7 to 3.6 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	120	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} =52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} =52 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	-	1	-	-	ns
t_{IH}	Input hold time HS	-	2.5	-	-	
t_{IDW}(3)	Input valid window (variable window)	-	3.5	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OVD}	Output valid time HS	-	-	5	7	ns
t_{OHD}	Output hold time HS	-	3	-	-	

1. Guaranteed by characterization results.
2. C_L = 20 pF.
3. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Table 3.3-100: Dynamics characteristics: eMMC characteristics VDD=1.71V to 1.9V(1)(2)

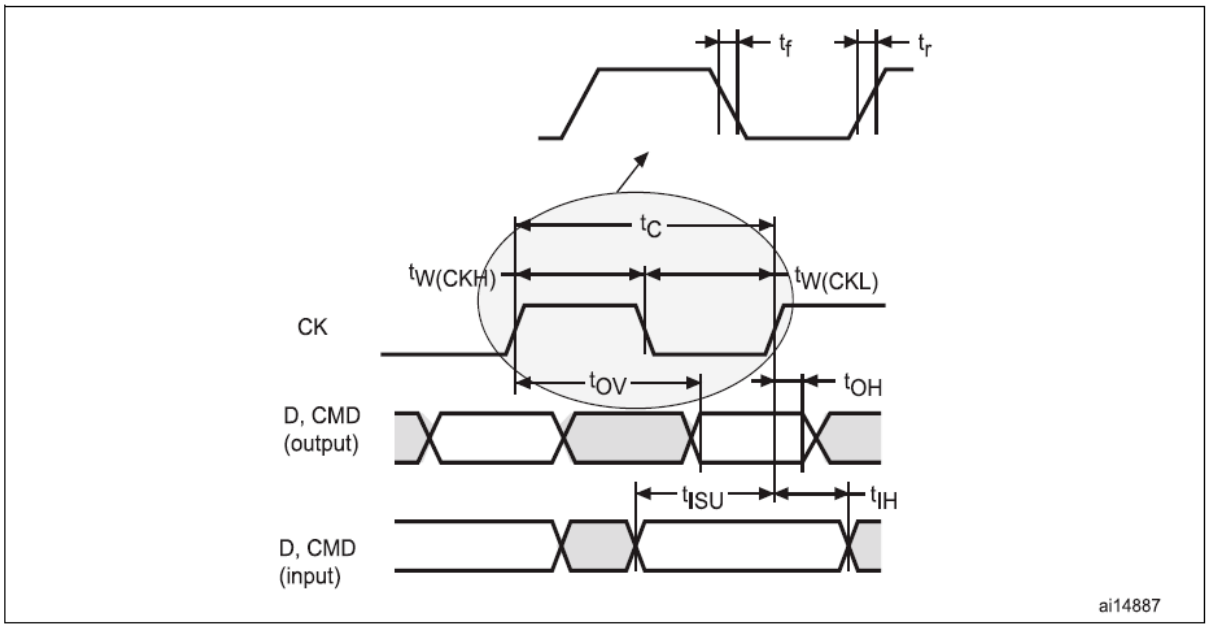


Figure 3.3-47: SDIO high-speed mode

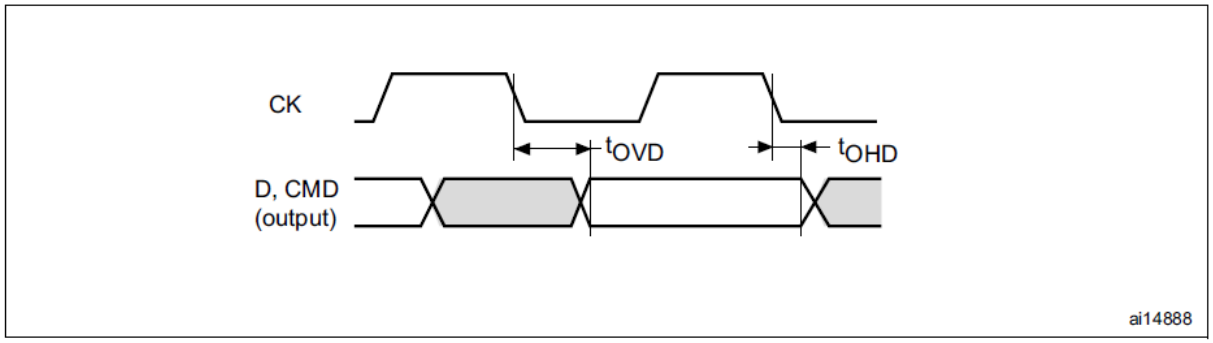


Figure 3.3-48: SD default mode

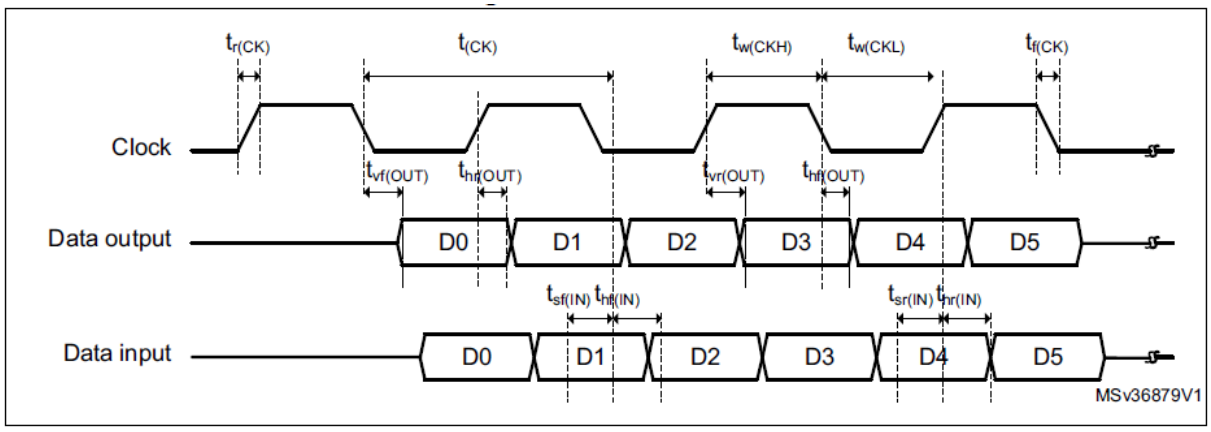


Figure 3.3-49: DDR mode

USB OTG_HS characteristics

Unless otherwise specified, the parameters given in Table 3.3-101 for ULPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage summarized in Table 3.3-1: General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- VOS level set to VOS1

Refer to Section 3.3.16: I/O port characteristics for more details on the input/output characteristics.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SC}	Control in (ULPI_DIR , ULPI_NXT) setup time	-	2.5	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	2	-	-	
t_{SD}	Data in setup time	-	2.5	-	-	
t_{HD}	Data in hold time	-	0	-	-	
t_{DC}/t_{DD}	Control/Datal output delay	$2.7<V_{DD}<3.6$ V C_L=20 pF	-	9	9.5	
		$1.71<V_{DD}<3.6$ V C_L=15 pF	-	9	14	

1. Guaranteed by characterization results.

Table 3.3-101: Dynamics characteristics: USB ULPI(1)

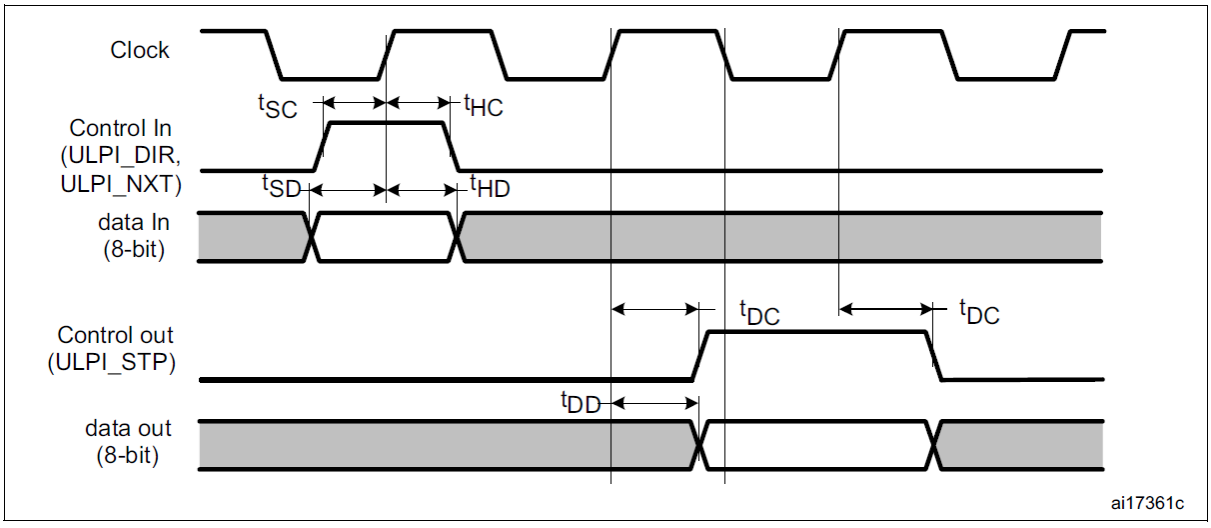


Figure 3.3-50: ULPI timing diagram

Ethernet interface characteristics

Unless otherwise specified, the parameters given in Table 3.3-102, Table 3.3-103 and Table 3.3-104 for SMI, RMII and MII are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage conditions summarized in Table 3.3-1: General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L=20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS1

Refer to Section 3.3.16: I/O port characteristics for more details on the input/output characteristics:

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.5 MHz)	400	400	403	ns
$T_{d(MDIO)}$	Write data valid time	0.5	1.5	4	
$t_{su(MDIO)}$	Read data setup time	12.5	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.

Table 3.3-102: Dynamics characteristics: Ethernet MAC signals for SMI (1)

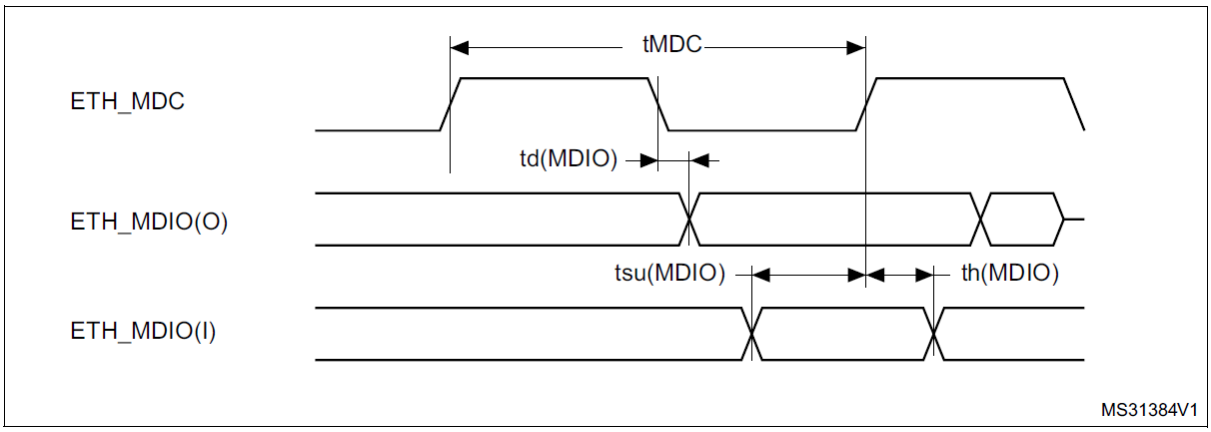


Figure 3.3-51: Ethernet SMI timing diagram

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	
$t_{su(CRS)}$	Carrier sense setup time	1.5	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	1.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	7	8	9.5	
$t_{d(TXD)}$	Transmit data valid delay time	8	9	11	

1. Guaranteed by characterization results.

Table 3.3-103: Dynamics characteristics: Ethernet MAC signals for RMII (1)

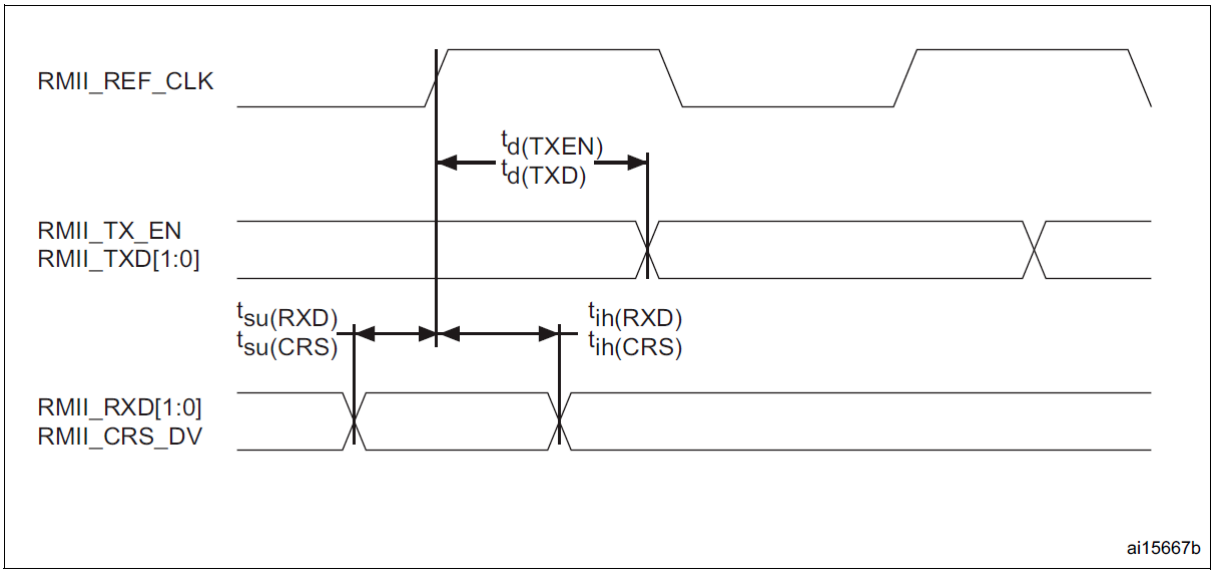


Figure 3.3-52: Ethernet RMII timing diagram

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	
$t_{su(DV)}$	Data valid setup time	1.5	-	-	
$t_{ih(DV)}$	Data valid hold time	1.5	-	-	
$t_{su(ER)}$	Error setup time	1.5	-	-	
$t_{ih(ER)}$	Error hold time	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	9	10	11	
$t_{d(TXD)}$	Transmit data valid delay time	8.5	9.5	12.5	

1. Guaranteed by characterization results.

Table 3.3-104: Dynamics characteristics: Ethernet MAC signals for MII (1)

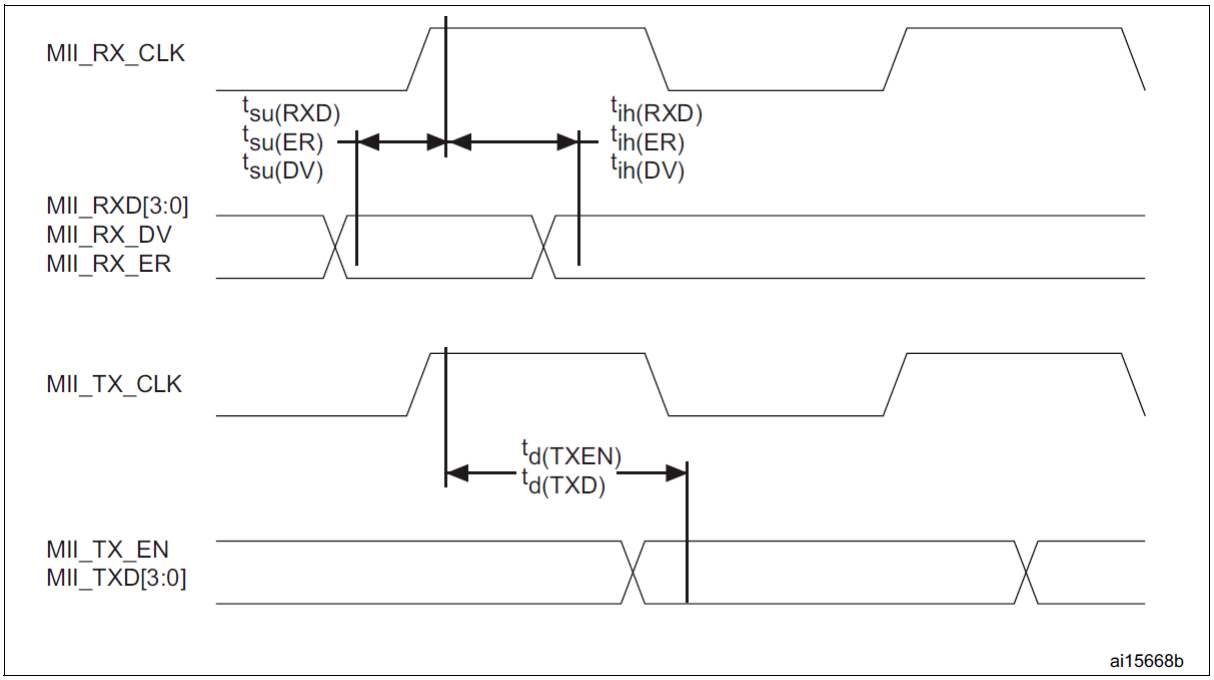


Figure 3.3-53: Ethernet MII timing diagram

JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in Table 3.3-105 and Table 3.3-106 for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage summarized in Table 3.3-1: General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x10
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS1

Refer to Section 3.3.16: I/O port characteristics for more details on the input/output characteristics:

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	T_{CK} clock frequency	2.7V <V_{DD}< 3.6 V	-	-	37	MHz
$1/t_{c(TCK)}$		1.62 <V_{DD}< 3.6 V	-	-	27.5	
$ti_{su(TMS)}$	TMS input setup time	-	2.5	-	-	
$ti_{h(TMS)}$	TMS input hold time	-	1	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	1.5	-	-	-
$ti_{h(TDI)}$	TDI input hold time	-	1	-	-	-
$t_{ov(TDO)}$	TDO output valid time	2.7V <V_{DD}< 3.6 V	-	8	13.5	-
		1.62 <V_{DD}< 3.6 V	-	8	18	-
$t_{oh(TDO)}$	TDO output hold time	-	7	-	-	-

Table 3.3-105: Dynamics JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	SWCLK clock frequency	2.7V <V_{DD}< 3.6 V	-	-	71	MHz
$1/t_{c(SWCLK)}$		1.62 <V_{DD}< 3.6 V	-	-	52.5	
$ti_{su(SWDIO)}$	SWDIO input setup time	-	2.5	-	-	-
$ti_{h(SWDIO)}$	SWDIO input hold time	-	1	-	-	-
$t_{ov(SWDIO)}$	SWDIO output valid time	2.7V <V_{DD}< 3.6 V	-	8.5	14	-
		1.62 <V_{DD}< 3.6 V	-	8.5	19	-
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8	-	-	-

Table 3.3-106: Dynamics SWD characteristics:

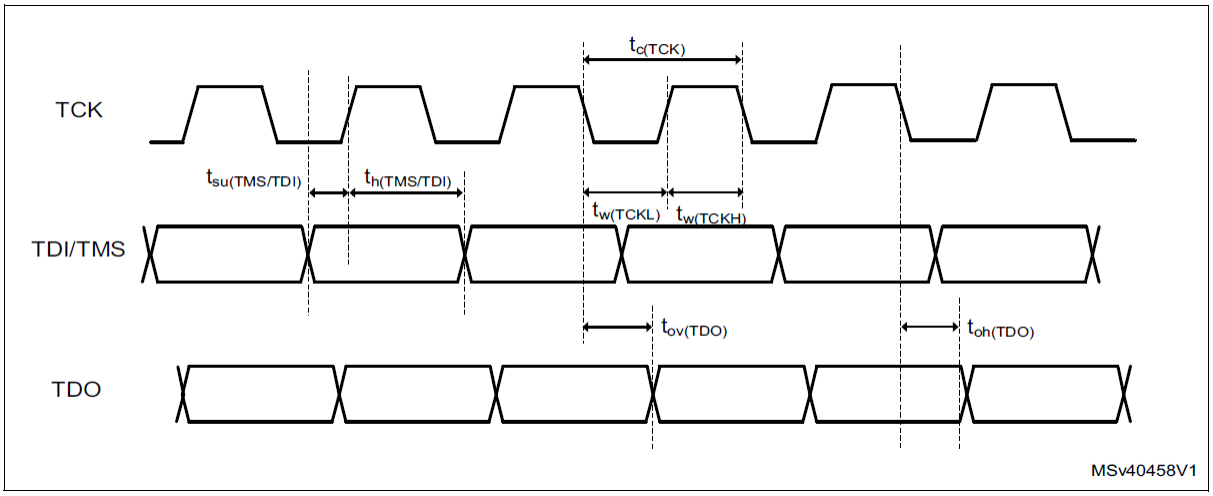


Figure 3.3-54: JTAG timing diagram

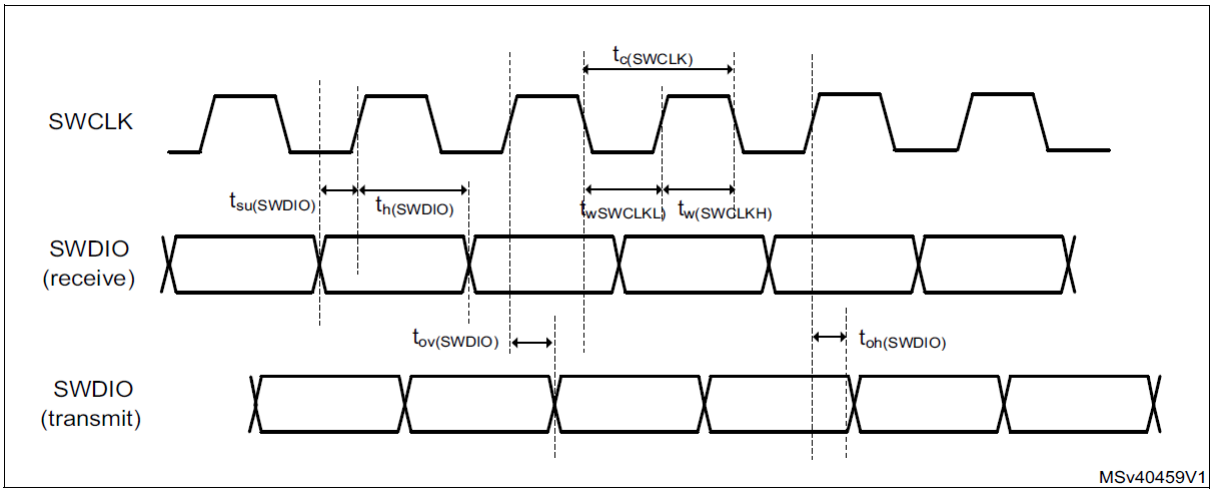


Figure 3.3-55: SWD timing diagram

3.4 ESC Sub-system DC Electrical Characteristics

3.4.1 Leakage Current and Capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IN}	Input leakage current. No pull-up or pull-down.	3.3V with 5V tolerant I/O pins. Vin = 5 or 0V.	-	< ±1	-	µA
C_{IN}	Input capacitance.	3.3V with 5V tolerant I/O pins.	-	2.3	-	pF

3.4.2 DC Characteristics of 3.3V (with 5V Tolerant) I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCC3IO	Power supply of 3.3V I/O		2.97	3.3	3.63	V
VCC33A	Analog power supply for Ethernet PHY		2.97	3.3	3.63	V
VCCK	Digital core power supply		1.08	1.2	1.32	V
VCC12A_PLL	Analog power supply for PLL		1.08	1.2	1.32	V
V_{IL}	Input low voltage.	VCC3IO=3.6V			0.8	V
V_{IH}	Input high voltage.	VCC3IO=3.6V	2.0			V
Vt-	Schmitt trigger negative going threshold voltage.	VCC3IO=3.6V	0.8	1.1		V
Vt+	Schmitt trigger positive going threshold voltage	VCC3IO=3.6V		1.6	2.0	V
Vol	Output low voltage.	Iol = 4 ~ 8mA	-	-	0.4	V
Voh	Output high voltage.	Ioh = 4 ~ 8mA	2.4	-	-	V
Vopu (1)	Output pull-up voltage for 5V tolerant IO	With internal pull-up resistor	VCC3IO – 0.9	-	-	V
Rpu	Input pull-up resistance.	For VCC3IO IO pad	40	75	190	KΩ
Rpd	Input pull-down resistance.	For VCC3IO IO pad	40	75	190	KΩ
Iin	Input leakage current.	Vin = 5 or 0V	-	±1	-	µA
	Input leakage current with pull-up resistance.	Vin = 0 V	-	-45	-	µA
	Input leakage current with pull-down resistance.	Vin = VCC3IO	-	45	-	µA
C_{IO}	I/O pin capacitance			5		pF

Note: This parameter indicates that the pull-up resistor for the 5V tolerant I/O pins cannot reach VCC3IO DC level even without DC loading current.

3.5 ESC Sub-system AC Electrical Characteristics

3.5.1 Power-on Reset for VCCK

Below figures and table show the two POR circuit spec during power ramp-up/down.

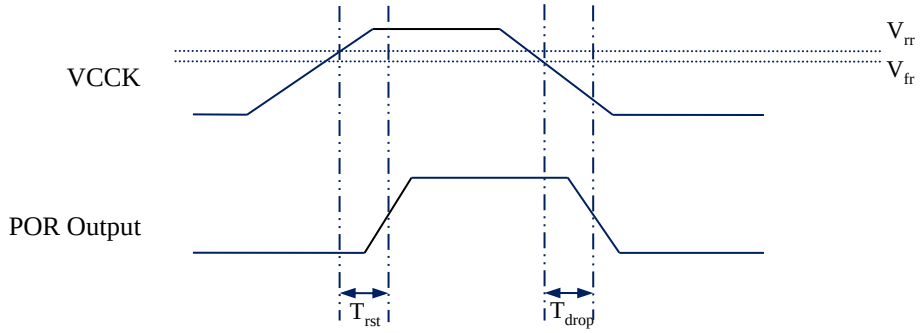


Figure 3.5-1: Power On Reset (POR) Timing Diagram

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
VCCK	Power supply voltage to be detected	-	1.0	1.2	1.32	V
V_{rr}	VCCK rise relax voltage	-	-	0.72	0.9	V
V_{fr}	VCCK fall release voltage	-	-	0.63	0.85	V
T_{rst}	Reset time after POR trigger up	VCCK slew rate = 1.0V / 1µs	1.8	2.5	4.8	µs
T_{drop}	Drop time of VCCK to reset	VCCK slew rate = 2.5V / 1µs	0.2	0.4	0.9	µs

Table 3.5-1: Power On Reset (POR) Timing Table

3.5.2 Ethernet PHY Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{PPTX}	Peak-to-peak differential output voltage	100BASE-TX mode	1.9	2.0	2.1	V
Tr/Tf	Signal rise/fall time	100BASE-TX mode	3.0	4.0	5.0	ns
	Output Jitter	100BASE-TX mode, Scrambled idle signal			1.4	ns
	Overshoot	100BASE-TX mode			5.0	%
	Error-free cable length	meter	100			m
Fiber Mode						
VOL	TX Output low voltage		1.0	1.5	2.0	V
VOH	TX Output high voltage		2.0	2.4	2.75	V
|VOD|	TX Differential threshold voltage		0.52	0.83	1.3	V
Vicm	RX Input common-mode voltage		1.67	2.0	2.33	V
|Vidth|	RX Input differential threshold voltage		0.2	0.83	1.0	V
SD	Copper mode	SD < 0.2V				
	Fiber mode without detected signal Generate far-end fault	1.0V < SD < 1.8V				
	Fiber mode with detected signal	SD > 2.4V				

3.6 Power Consumption

3.6.1 Main System

Please reference the section 3.3.7 in detail.

3.6.2 ESC Sub-system

Item	Conditions	VCCIO + VCC33A	VCCK + VCC12A_PLL	Units
Digital IO	20 I/O Output (Typ.)	160	50	mA

Note: Above current value are typical values measured on AX58400 Test board.

Table 3.6-1: Power Consumption

3.6.3 Package Thermal Characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
Θ_{JC}	Thermal resistance of junction to case		-	9.3	-	°C/W
Θ_{JA}	Thermal resistance of junction to ambient	Still air	-	23.9	-	°C/W
Θ_{JB}	Thermal resistance of junction to board		-	11.68	-	°C/W

Note: Above information is based on using 6 layers PCB.

Table 3.6-2: Thermal Characteristics

3.7 ESC Sub-system Power–up Sequence

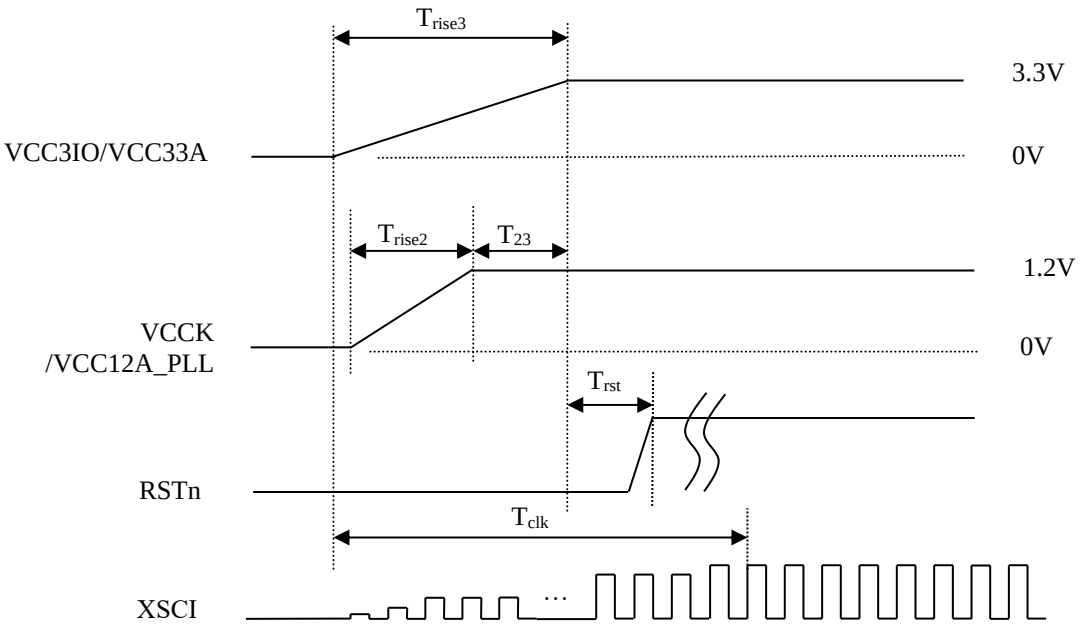


Figure 3.7-1: Power-up Sequence Timing Diagram

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{rise3}	3.3V power supply rise time.	From 0V to 3.3V.	-	400	-	us
T_{rise2}	1.2V power supply rise time.	From 0V to 1.2V.	-	200	-	us
T_{23}	VCCK rising to 1.2V to VCC3IO rising to 3.3V interval.		-	200	-	us
T_{rst}	RSTn asserted low level interval.	From VCC3IO rising to 3.3V to RSTn going high.	-	40	-	us
T_{clk}	25MHz crystal oscillator start-up time.	From VCC3IO rising to 3.3V to clock stable of 25MHz crystal oscillator.	-	-	60	ms
$T_{Startup}$	Startup time	PDI operational after power good, without I2C EEPROM loading error	-	-	70	ms

Note: The above typical timing data is measured from AX58400 test board.

Table 3.7-1: Power-up Sequence Timing Table

3.8 ESC Sub-system AC Timing Characteristics

3.8.1 ESC I2C Timing

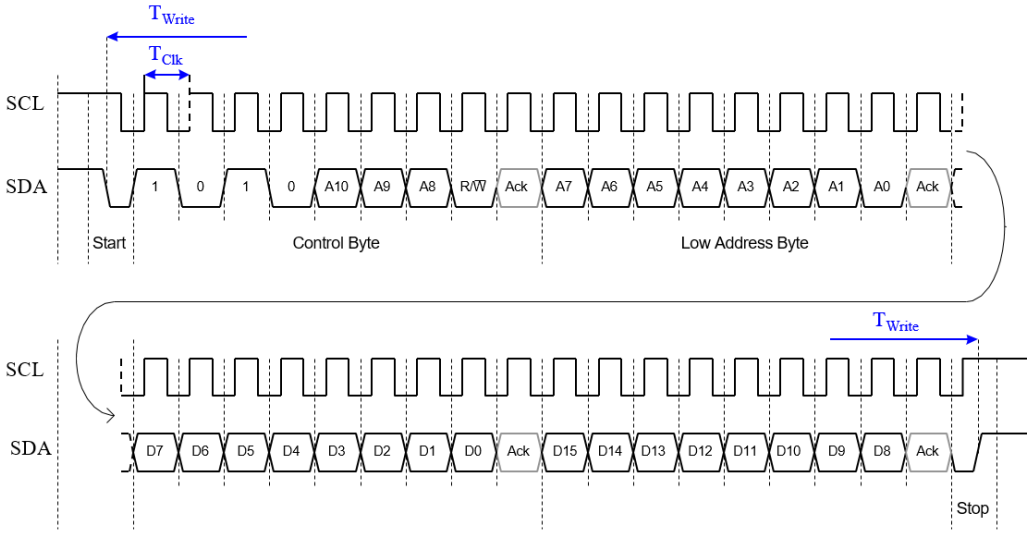


Figure 3.8-1: Write access (1 address byte, up to 16 Kbit EEPROMs)

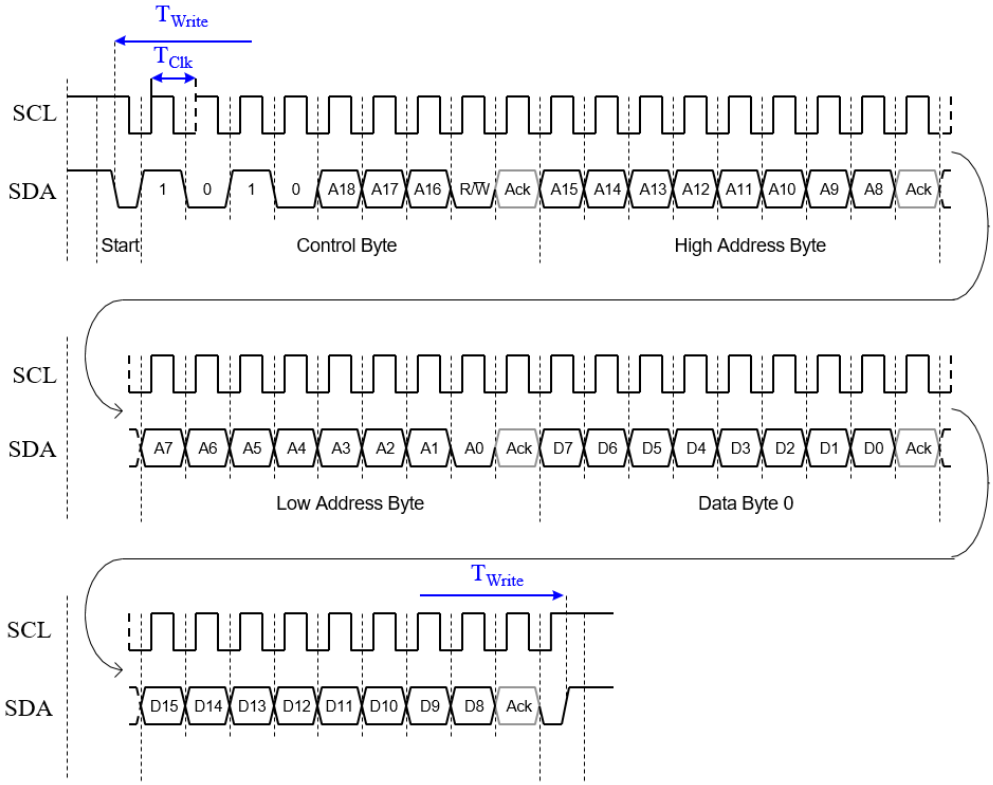


Figure 3.8-2: Write access (2 address bytes, 32 Kbit - 4 Mbit EEPROMs)

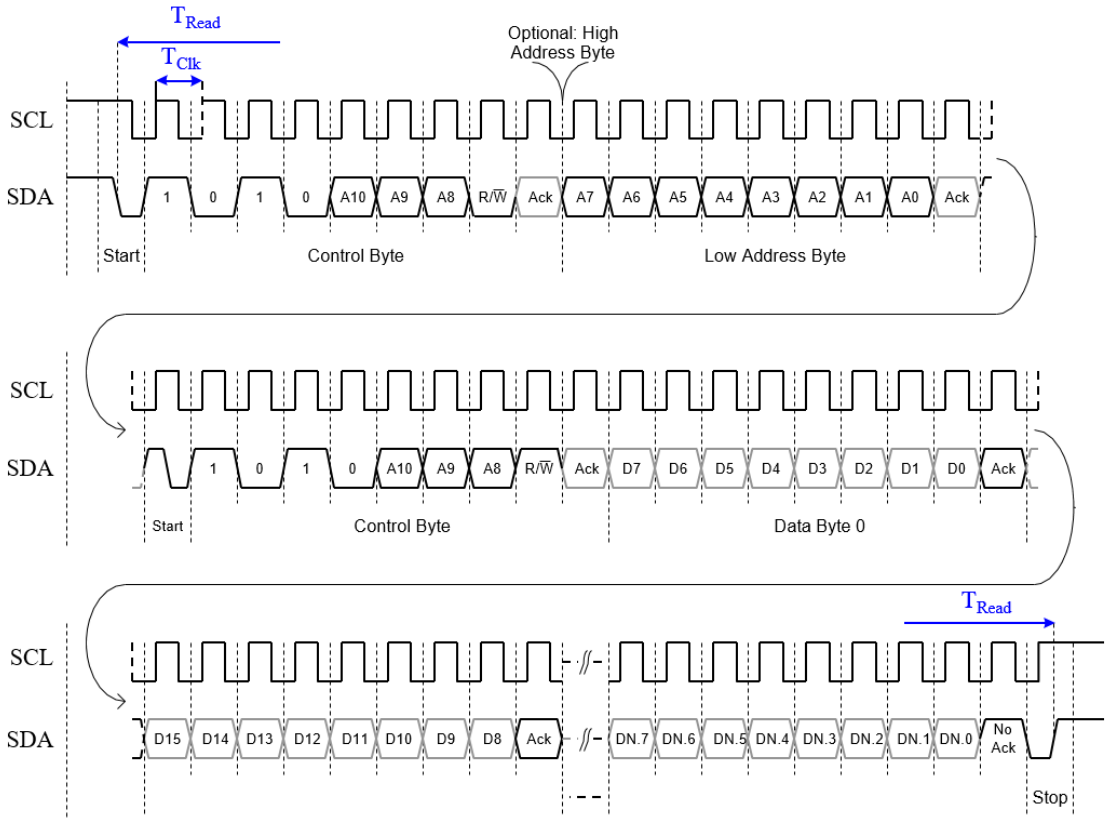


Figure 3.8-3: Read access (1 address byte, up to 16 Kbit EEPROMs)

Symbol	Parameter		Typical		Units
			Up to 16 Kbit	32 Kbit-4 Mbit	
T_{Clk}	EEPROM clock period		6.72 (≈ 150 KHz)		us
T_{Write}	Write access time (without errors)		250	310	us
T_{Read}	Read access time (without errors):	2 words	440	500	us
		configuration (8 Words)	1.16	1.22	ms
T_{Delay}	Time until configuration loading begins after Reset is gone		65.5		us

Table 3.8-1: I²C EEPROM Timing Table

3.8.2 ESC Port 2 MII Timing

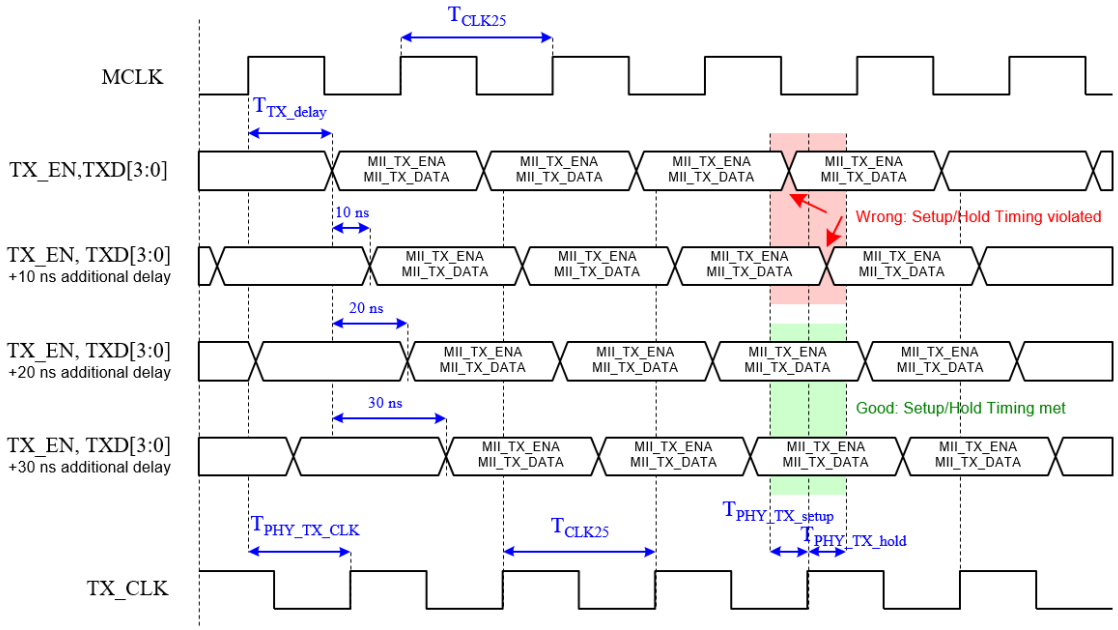


Figure 3.8-4: Port 2 MII TX Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{CLK25}	MCLK output	-	40	-	ns
T_{TX_delay}	TX_EN/TXD[3:0] delay after rising edge of MCLK	-	-	2	ns
$T_{PHY\_TX\_CLK}$	Delay between MCLK and TX_CLK output of the PHY	-	PHY dependent	-	ns
$T_{PHY\_TX\_setup}$	PHY setup time	PHY dependent	-	-	ns
$T_{PHY\_TX\_hold}$	PHY hold time	PHY dependent	-	-	ns

Table 3.8-2: Port 2 MII TX Timing Table

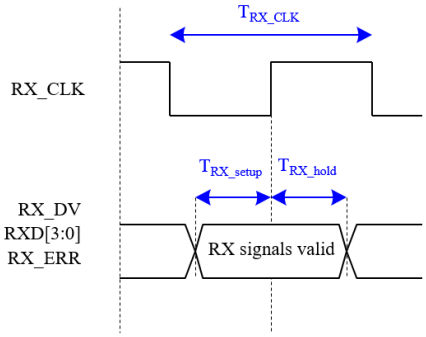


Figure 3.8-5: Port 2 MII RX Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{RX_CLK}	RX_CLK period (100 PPM with maximum FIFO Size only)	-	40	-	ns
T_{RX_setup}	RX_DV/RX_ER/RXD[3:0] valid before rising edge of RX_CLK	2.1	-	-	ns
T_{RX_hold}	RX_DV/RX_ER/RXD[3:0] valid after rising edge of RX_CLK	0.5	-	-	ns

Table 3.8-3: Port 2 MII RX Timing Table

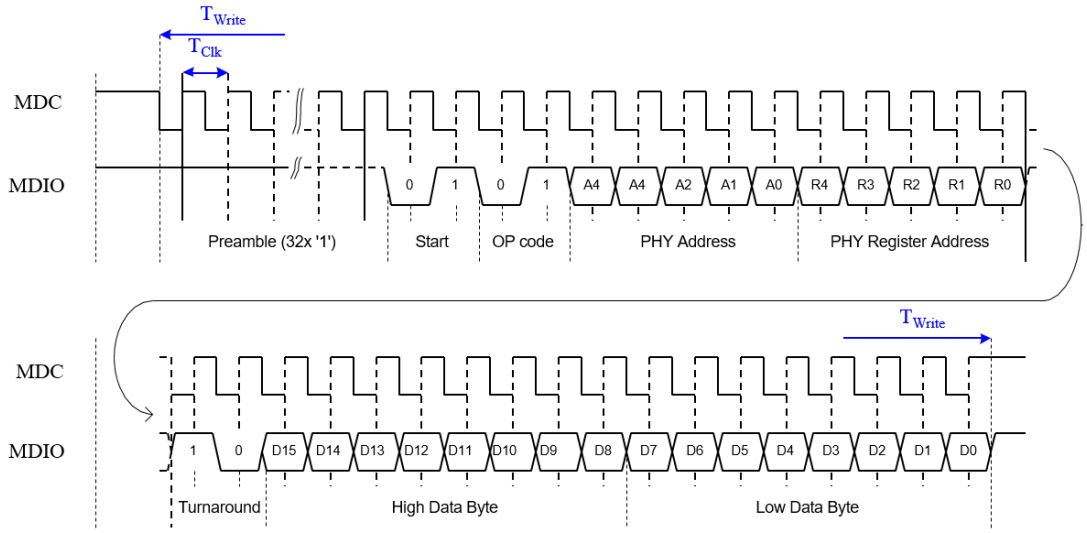


Figure 3.8-6: MDC/MDIO Write access

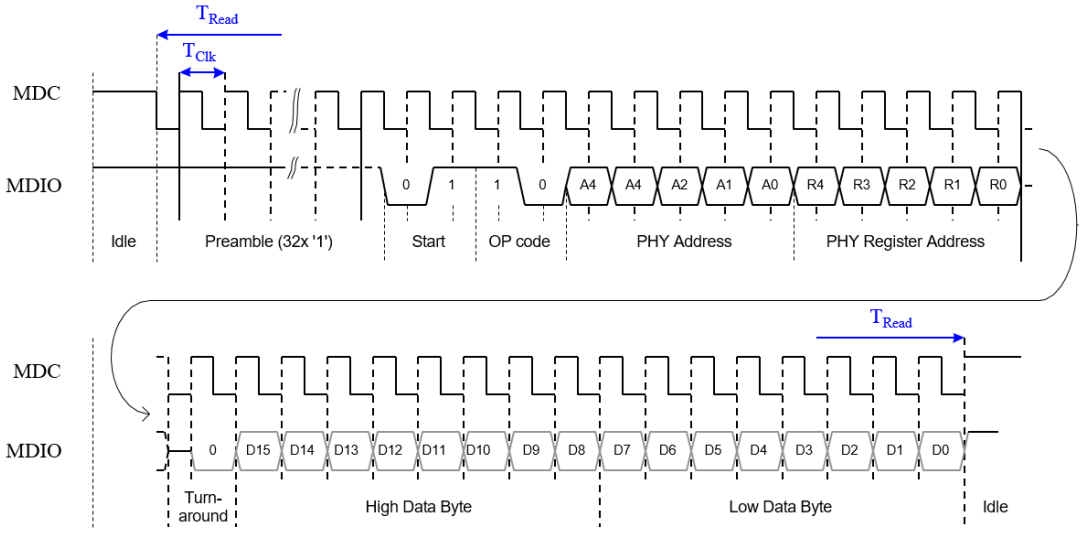


Figure 3.8-7: MDC/MDIO Read access

Symbol	Description	Min	Typ	Max	Units
T_{MDC}	MDC period		400 (≈ 2.5 MHz)		ns
T_{Write}	MI Write access time		25.6		us
T_{Read}	MI Read access time		25.4		us
$T_{MI\_startup}$	Time between reset end and the first access of MI Link detection and configuration		1.34		ms

Table 3.8-4: MDC/MDIO Timing Table

3.8.3 Distributed Clocks SYNC/LATCH

Symbol	Description	Min	Typ	Max	Units
T_{DC_LATCH}	Time between LATCH 0/1 events	12			ns
$T_{DC\_SYNC\_Jitter}$	SYNC 0/1 output jitter			12	ns

Table 3.8-5: DC SYNC/LATCH timing characteristics

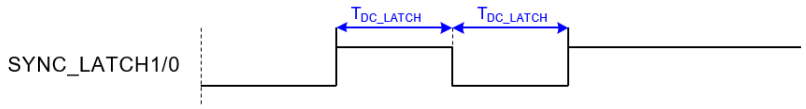


Figure 3.8-8: LATCH timing

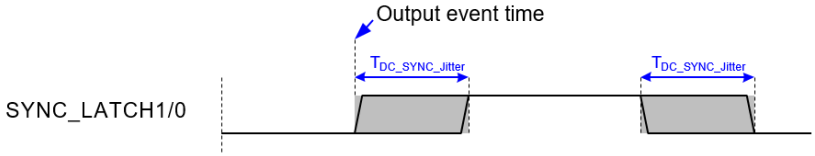


Figure 3.8-9: SYNC timing

3.8.4 ESC Digital I/O Timing

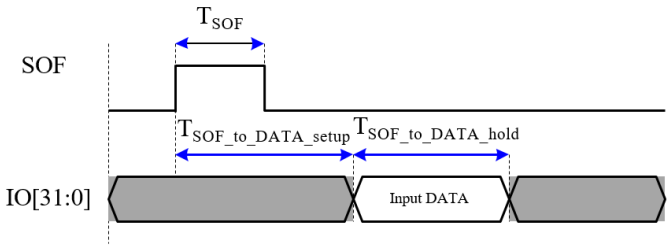


Figure 3.8-10: Digital Input: Input data sampled at SOF, IO can be read in the same frame

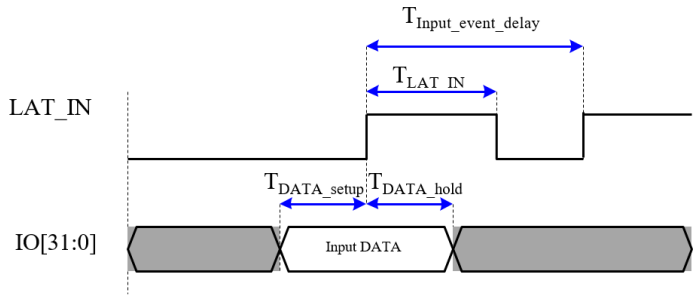


Figure 3.8-11: Digital Input: Input data sampled with LATCH_IN

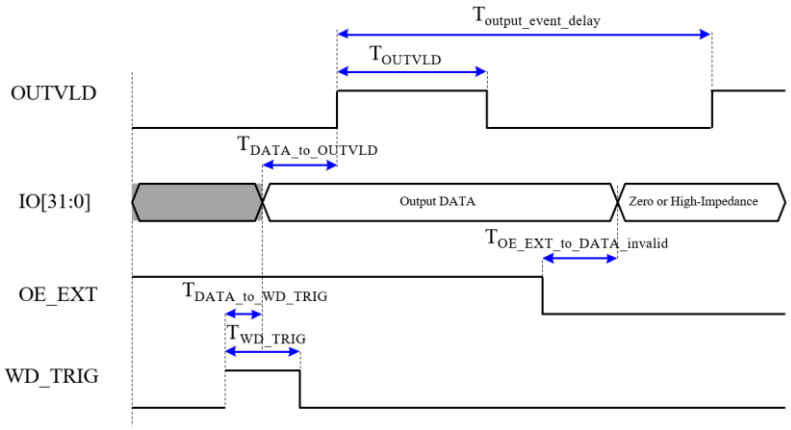


Figure 3.8-12: Digital Output timing

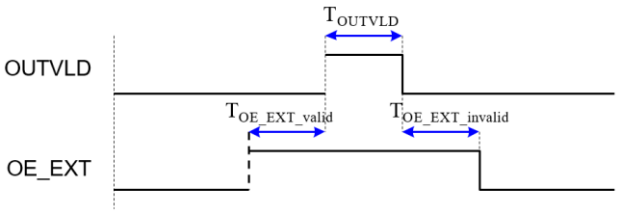


Figure 3.8-13: OE_EXT timing

Symbol	Description	Min	Typ	Max	Units
T_{DATA_setup}	Input data valid before LAT_IN	5	-	-	ns
T_{DATA_hold}	Input data valid after LAT_IN	2	-	-	ns
T_{LAT_IN}	LAT_IN high time	4	-	-	ns
T_{SOF}	SOF high time	-	40	-	ns
$T_{SOF\_to\_DATA\_setup}$	Input data valid after SOF, so that Inputs can be read in the same frame	0	-	1.2	us
$T_{SOF\_to\_DATA\_hold}$	Input data invalid after SOF	1.6	-	-	us
$T_{input\_event\_delay}$	Time between consecutive input events	440	-	-	ns
T_{OUTVLD}	OUTVLD high time	-	80	-	ns
$T_{DATA\_to\_OUTVLD}$	Output data valid before OUTVLD	79	-	-	ns
T_{WD_TRIG}	WD_TRIG high time	-	40	-	ns
$T_{DATA\_to\_WD\_TRIG}$	Output data valid after WD_TRIG	-	-	20	ns
$T_{OE\_EXT\_to\_DATA\_invalid}$	Outputs zero or Outputs hi-Z after OE_EXT set to low	0	-	9.5	ns
$T_{output\_event\_delay}$	Time between consecutive output events	320	-	-	ns
$T_{OUT\_EXT\_valid}$	OUT_EXT valid before OUTVLD	-	80	-	ns
$T_{OUT\_EXT\_invalid}$	OUT_EXT invalid after OUTVLD	-	80	-	ns

Table 3.8-6: Digital I/O timing Table

3.8.5 ESC PDI SPI Slave Timing

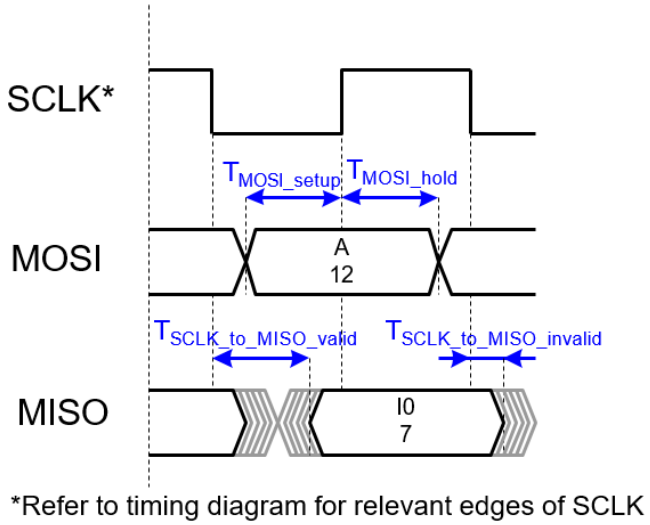


Figure 3.8-14: Basic MOSI/MISO timing

Symbol	Description		Min	Typ	Max	Units
T_{SCLK}	SCLK Period		33 (≤30MHz)	-	-	ns
$T_{SEL\_to\_CLK}$	First SCLK cycle after SCS_ESC asserted		5	-	-	ns
$T_{CLK\_to\_SEL}$	Deassertion of SCS_ESC after last SCLK cycle	SPI mode 0/2, SPI mode 1/3 with normal data out sample	5	-	-	ns
		SPI mode 1/3 with late data out sample	T_{CLK}/2+ 5			
T_{read}	Only for read access between address/command and first data byte. Can be ignored if BUSY or Wait State Bytes are used.		240	-	-	ns
T_{access_delay}	Delay between SPI accesses		40	-	-	ns
T_{MOSI_setup}	MOSI valid before SCLK edge		3	-	-	ns
T_{MOSI_hold}	MOSI valid after SCLK edge		0	-	-	ns
$T_{SCLK\_to\_MISO\_valid}$	MISO valid after SCLK edge		-	-	10.5	ns
$T_{SCLK\_to\_MISO\_invalid}$	MISO invalid after SCLK edge		0	-	-	ns
T_{IRQ_delay}	Internal delay between AL event and SINT output to enable correct reading of the interrupt registers.		-	180	-	ns

Table 3.8-7: PDI SPI Slave Timing Table

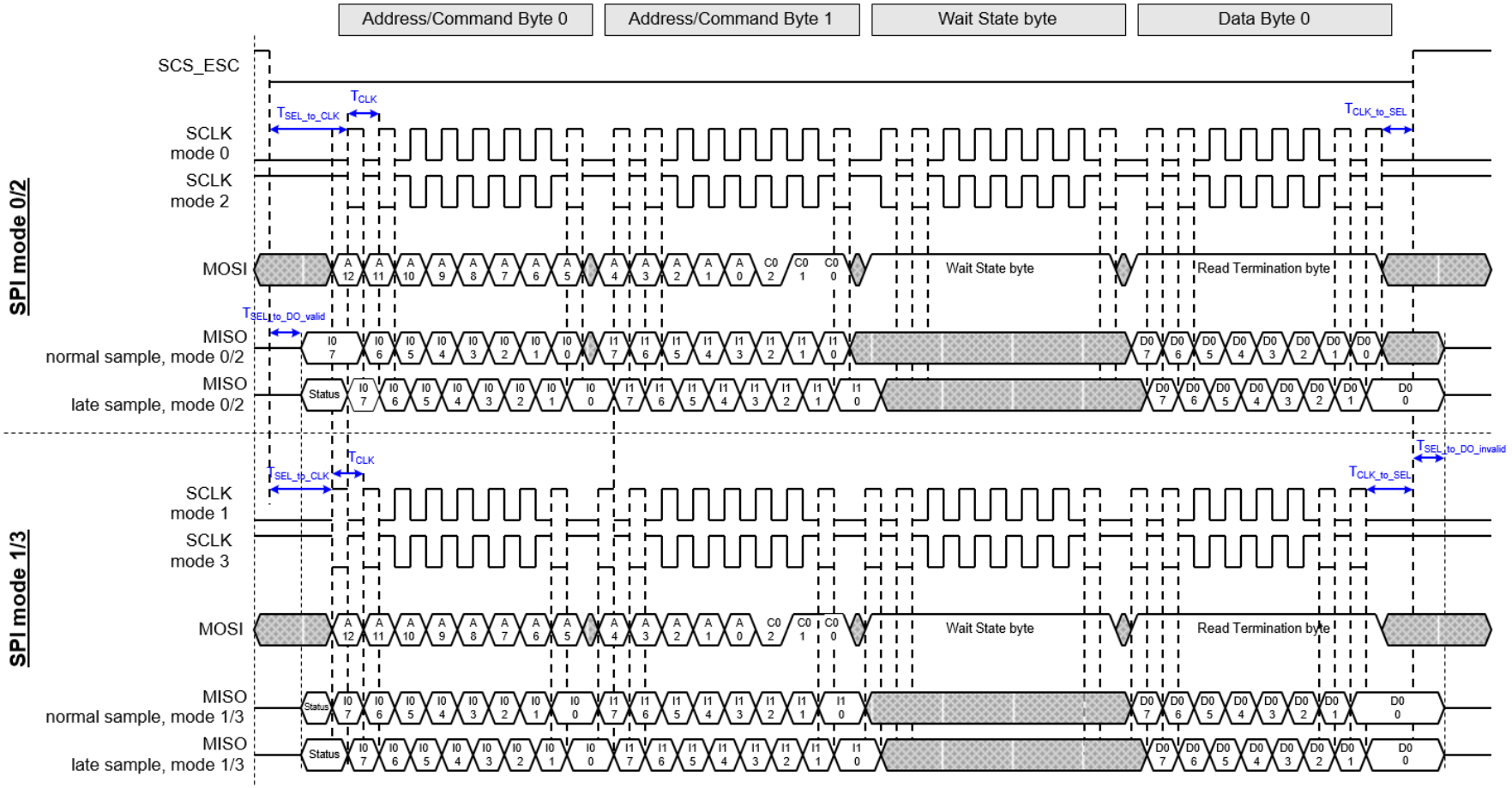


Figure 3.8-15: PDI SPI Slave read access (2 byte addressing, 1 byte read data) with Wait State byte

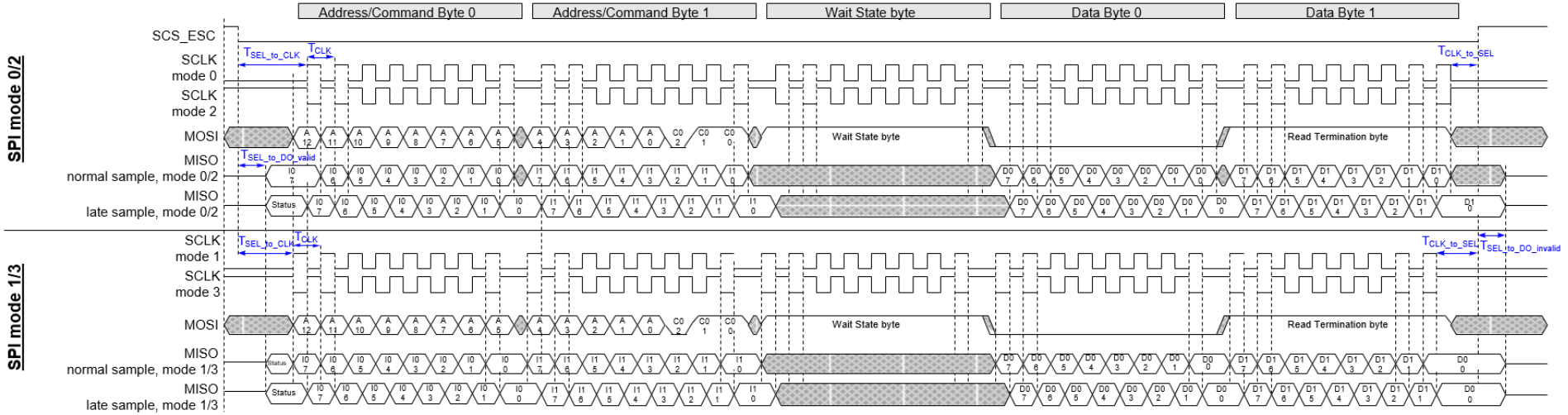


Figure 3.8-16: PDI SPI Slave read access (2 byte addressing, 2 byte read data) with Wait State byte

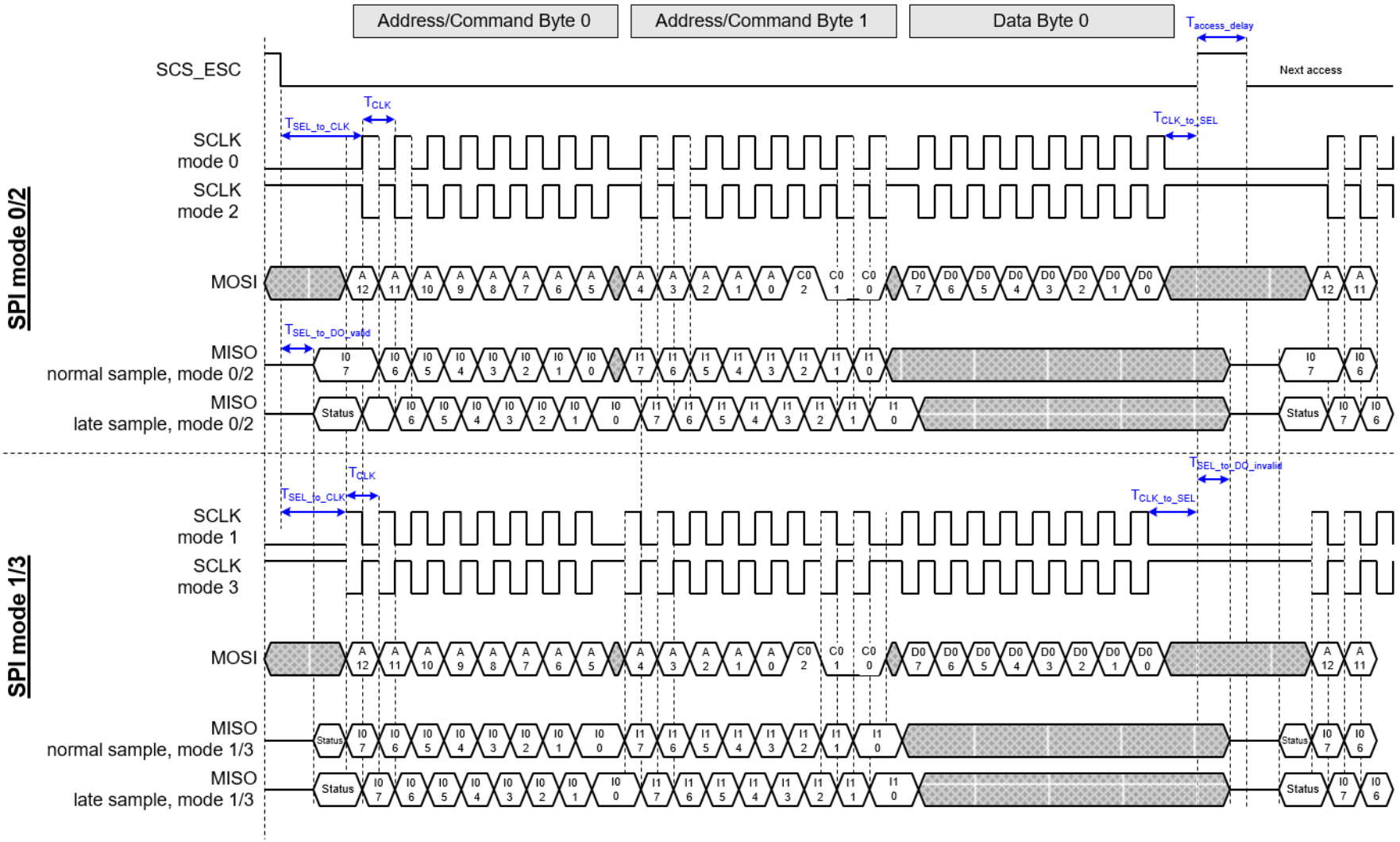


Figure 3.8-17: PDI SPI Slave write access (2 byte addressing, 1 byte write data)

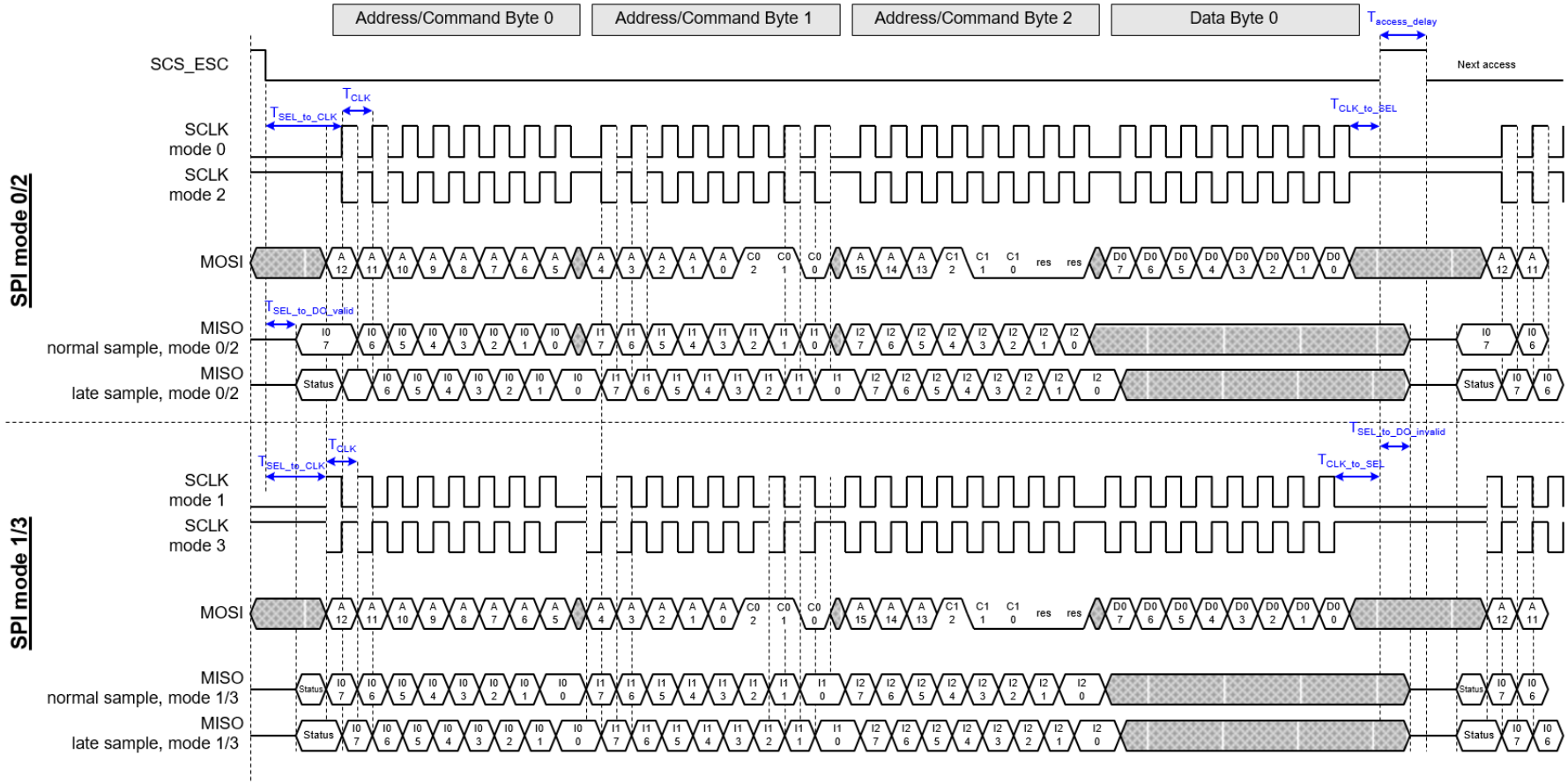


Figure 3.8-18: PDI SPI Slave write access (3 byte addressing, 1 byte write data)

3.8.6 Function SPI Slave Timing

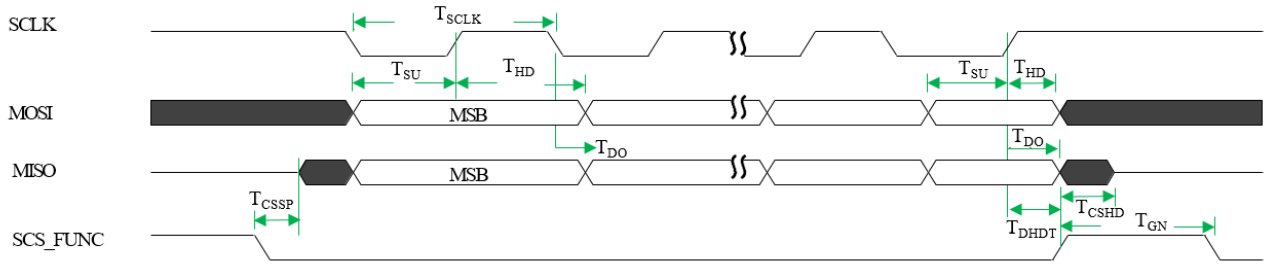


Figure 3.8-19: Function SPI Slave with share pin Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{SCLK}	SCLK clock frequency	-	-	50	MHz
T_{DO}	MISO data valid time after SCLK edge	9.2	-	-	ns
T_{SU}	MOSI data setup time before SCLK edge	2	-	-	ns
T_{HD}	MOSI data hold time after SCLK edge	2	-	-	ns
T_{CSSP}	SCS setup time before MISO active	7.6	-	-	ns
T_{DHD}	SCS hold time after SCLK edge	21	-	-	ns
T_{CSHD}	MISO data hold time after SCS de-assert	2.6	-	-	ns
T_{GN}	SCS negation to next SCS assertion time	40	-	-	ns

Table 3.8-8: Function SPI with share pin Timing Table

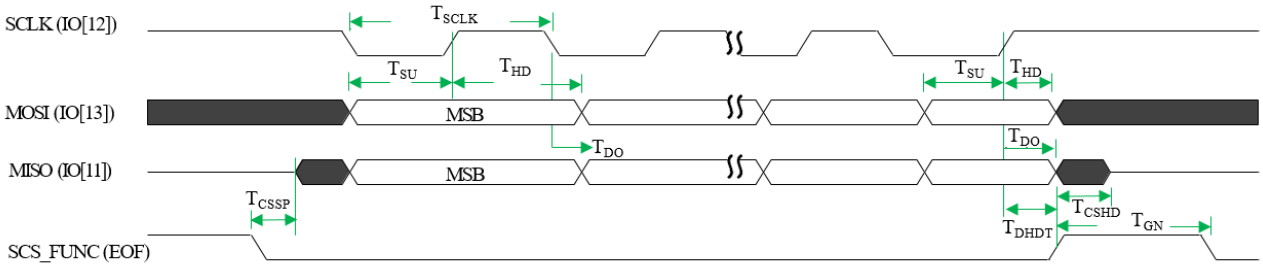


Figure 3.8-20: Function SPI Slave with individual pin Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{SCLK}	SCLK clock frequency	-	-	47	MHz
T_{DO}	MISO data valid time after SCLK edge	10.5	-	-	ns
T_{SU}	MOSI data setup time before SCLK edge	2	-	-	ns
T_{HD}	MOSI data hold time after SCLK edge	2	-	-	ns
T_{CSSP}	SCS setup time before MISO active	7.7	-	-	ns
T_{DHD}	SCS hold time after SCLK edge	21	-	-	ns
T_{CSHD}	MISO data hold time after SCS de-assert	2.5	-	-	ns
T_{GN}	SCS negation to next SCS assertion time	40	-	-	ns

Table 3.8-9: Function SPI with individual pin Timing Table

3.8.7 PWM Motor Controller Timing

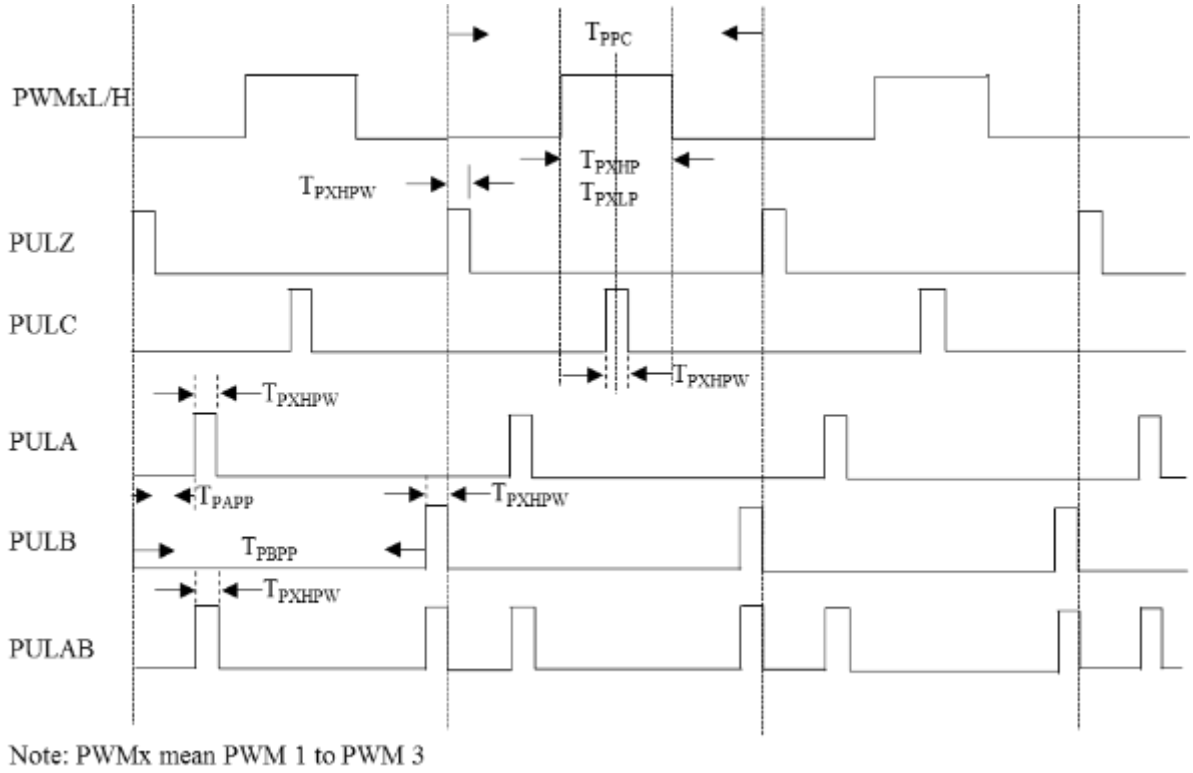


Figure 3.8-21: PWMx Timing

Symbol	Description	EN8X	Min	Typ	Max	Units
T_{PPC}	PWM Period Cycle	x1	-	PPC * 10	-	ns
		x8	-	PPC * 80	-	ns
T_{PxHP}	PWM x High pulse Width set by PxHPWR	x1	-	PxHPV * 10*1	-	ns
		x8	-	PxHPV * 80*1	-	ns
T_{PxLP}	PWM x Low pulse Width set by PxHPWR	x1	-	PxHPV * 10*1	-	ns
		x8	-	PxHPV * 80*1	-	ns
T_{PXHPW}	Pulse width for PULZ, PULC, PULA, PULB, and PULAB	x1	-	PXHPW * 10	-	ns
		x8	-	PXHPW * 80	-	ns
T_{PAPP}	PWM Trigger Pulse A Position in PWM Period Cycle	x1	-	PTAPP * 10	-	ns
		x8	-	PTAPP * 80	-	ns
T_{PBPP}	PWM Trigger Pulse B Position in PWM Period Cycle	x1	-	PTBPP * 10	-	ns
		x8	-	PTBPP * 80	-	ns

Note *1: “x” = 1 ~ 3

Table 3.8-10: PWMx Timing Table

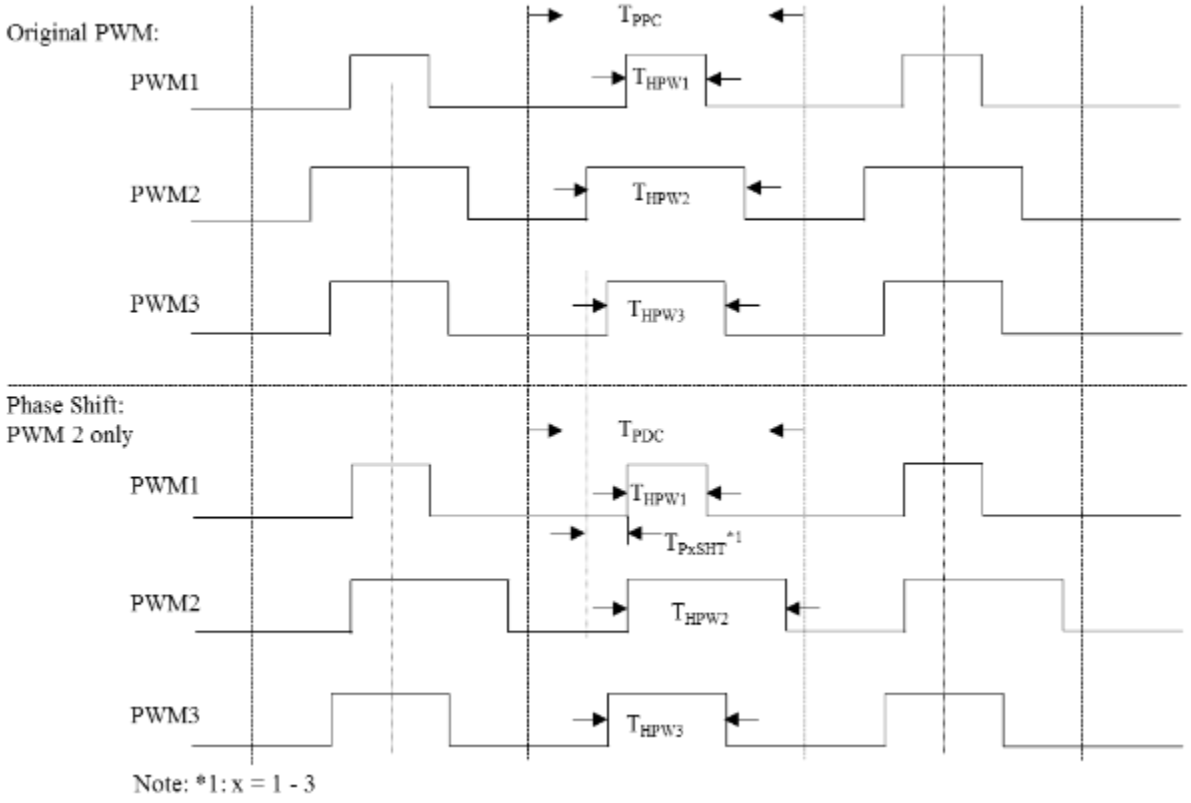


Figure 3.8-22: Only PWM Channel 2 Shift Diagram

Symbol	Description	EN8X	Min	Typ	Max	Units
T_{P1SHT}	PWM pulse was postponed raising time (addition with P1SHR) and the pulse width stays the same	x1	-	P1SHIFT * 10	-	ns
		x8	-	P1SHIFT * 80	-	ns
T_{P2SHT}	Please reference T_{P1SHT} content	x1	-	P2SHIFT * 10	-	ns
		x8	-	P2SHIFT * 80	-	ns
T_{P3SHT}	Please reference T_{P1SHT} content	x1	-	P3SHIFT * 10	-	ns
		x8	-	P3SHIFT * 80	-	ns

Table 3.8-11: PWMx Shift Timing Table

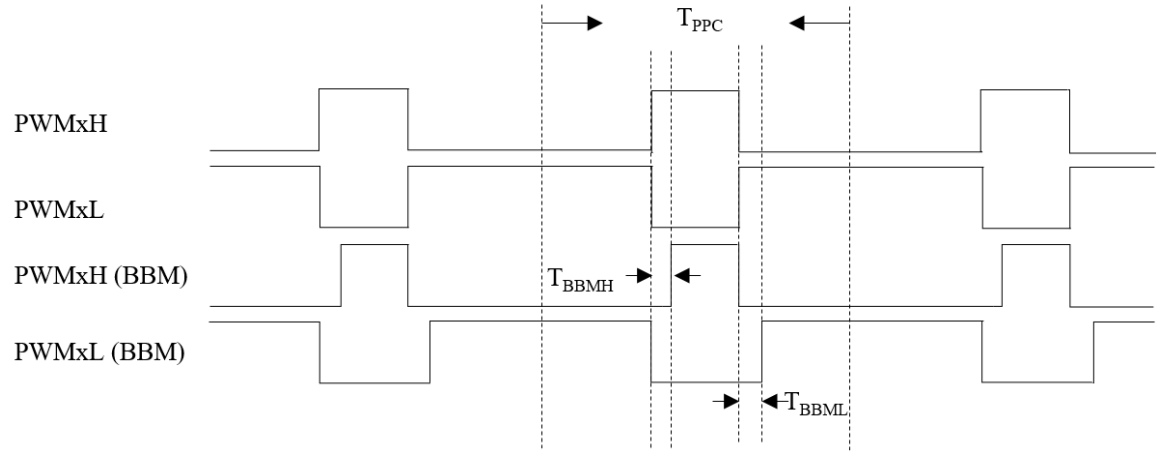


Figure 3.8-23: BBM (Break Before Make) Timing Diagram

Symbol	Description	EN8X	Min	Typ	Max	Units
T_{BBMH}	High pulse was postponed raising and reduce pulse width	x1	-	PBBMH * 10	-	ns
		x8	-	PBBMH * 80	-	ns
T_{BBML}	Low pulse was postponed falling and addition pulse width	x1	-	PBBML * 10	-	ns
		x8	-	PBBML * 80	-	ns

Table 3.8-12: PWMx BBM Timing Table

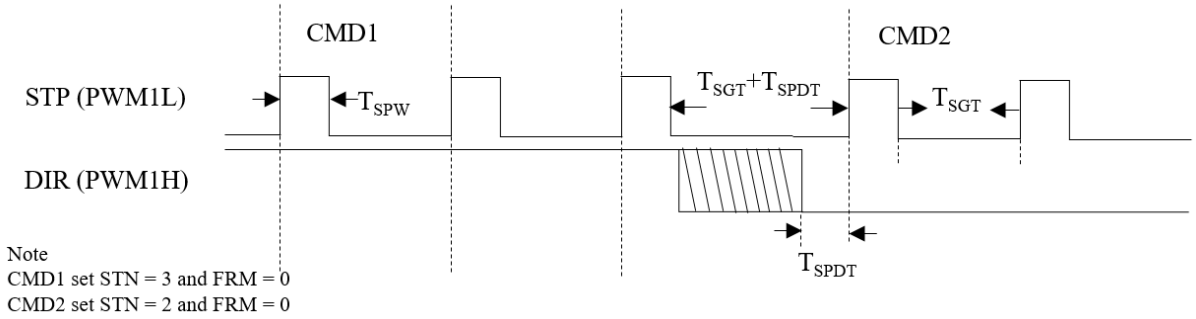


Figure 3.8-24: One Shot with multi Step Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{SGT}	Step Pulse to Pulse Gap time set by SGTLR and SGTHR	-	SGT * 10	-	ns
T_{SPW}	Step Pulse Width set by SHPWR Note: Step frequency = 1/ (T_{SPW} +T_{SGT})	-	SPW * 10	-	ns
T_{SPDY}	Direction Transform Delay Time set by TDLYR	-	SPDT * 10	-	ns

Table 3.8-13: Step function timing table

3.8.8 Incremental and Hall Encoder Interface Timing

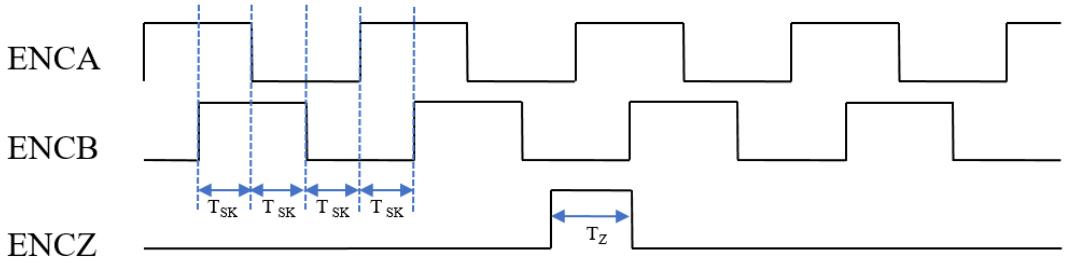


Figure 3.8-25: ABZ Timing Diagram

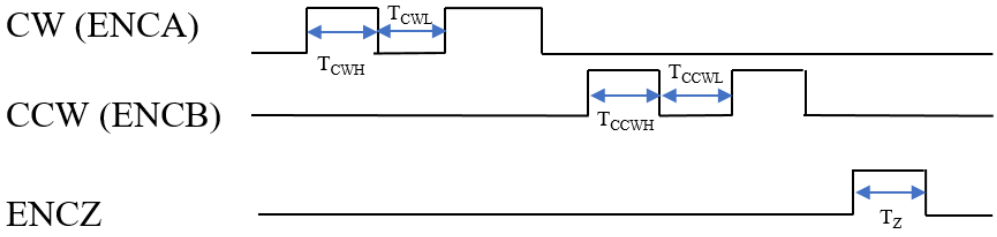


Figure 3.8-26: CW/CCW Timing Diagram

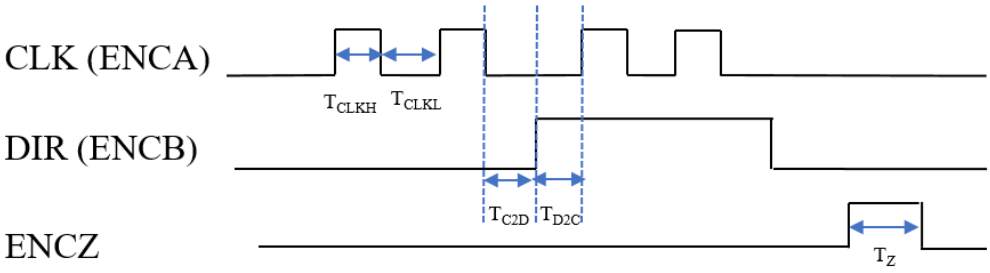


Figure 3.8-27: CLK/DIR Timing Diagram

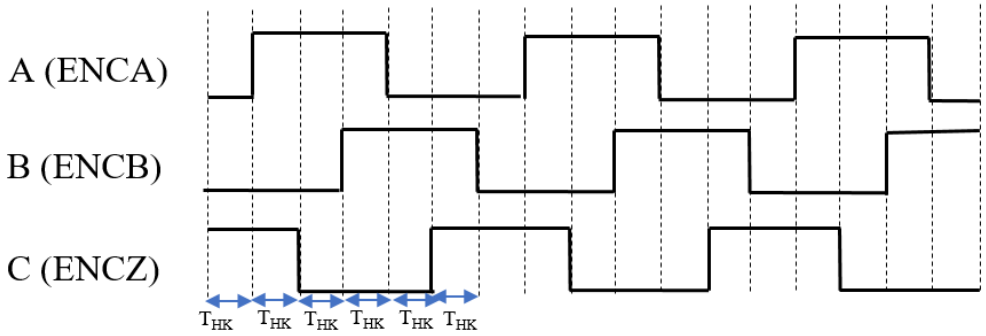


Figure 3.8-28: Hall Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{SK}	AB state keep time	30	-	-	ns
T_{Z}	Z Pulse Width	30	-	-	ns
T_{CWH}	CW high time	30	-	-	ns
T_{CWL}	CW low time	30	-	-	ns
T_{CCWH}	CCW high time	30	-	-	ns
T_{CCWL}	CCW low time	30	-	-	ns
T_{CLKH}	CLK high time	30	-	-	ns
T_{CLKL}	CLK low time	30	-	-	ns
T_{C2D}	CLK to DIR time	30	-	-	ns
T_{D2C}	DIR to CLK time	30	-	-	ns
T_{HK}	Hall state keeps time	60	-	-	ns

Table 3.8-14: Incremental and Hall Encoder Timing Table

3.8.9 ESC SPI Master Timing

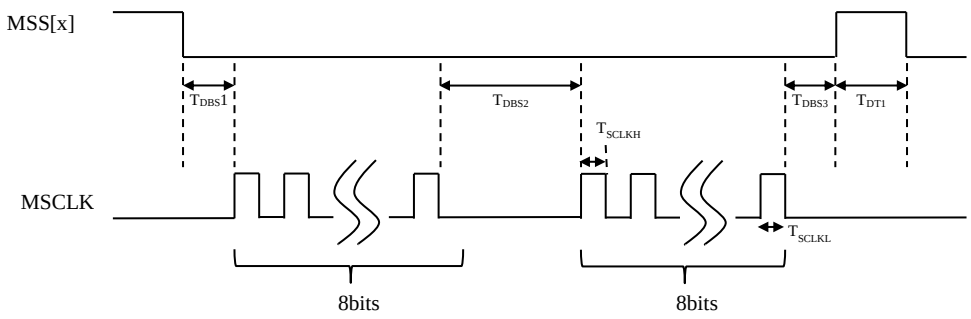


Figure 3.8-29: SPI Master Timing

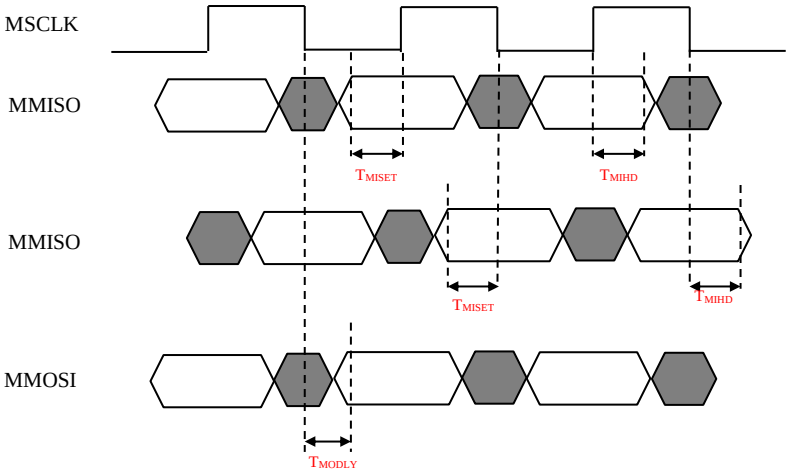


Figure 3.8-30: MMISO /MMOSIO Timing

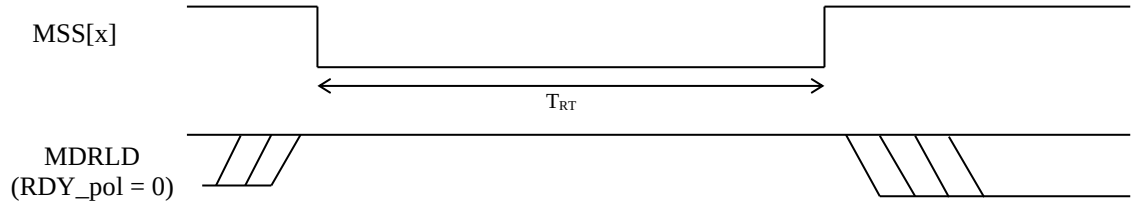


Figure 3.8-31: SPI MDRLD Ready Timeout Timing

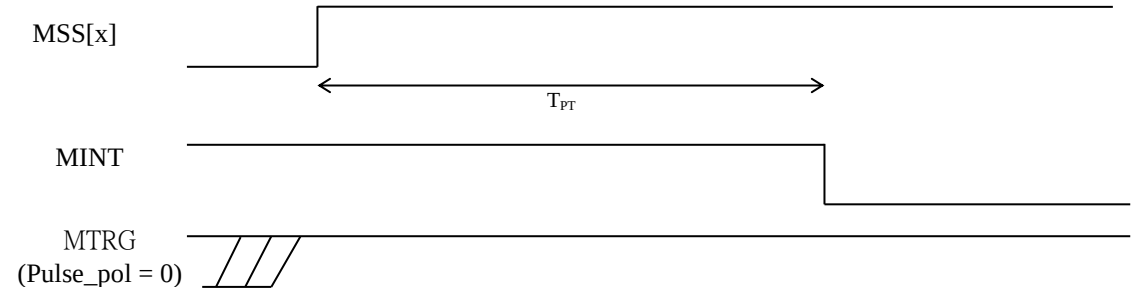


Figure 3.8-32: SPI MTRG Trigger Pulse Timeout

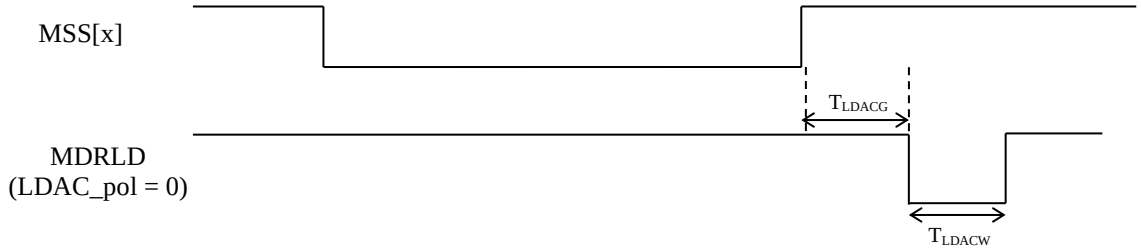
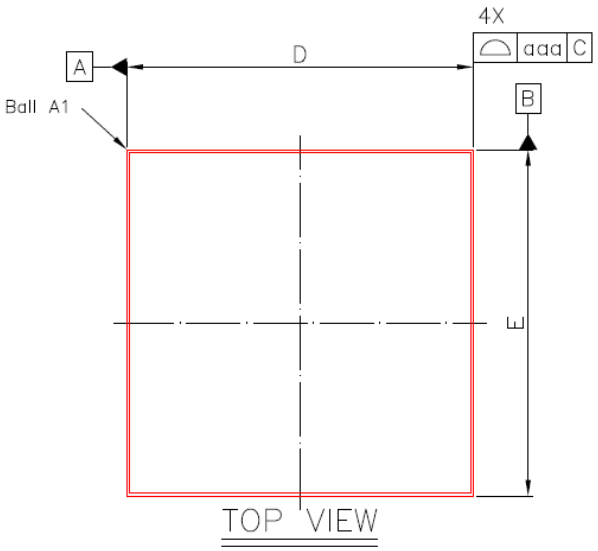


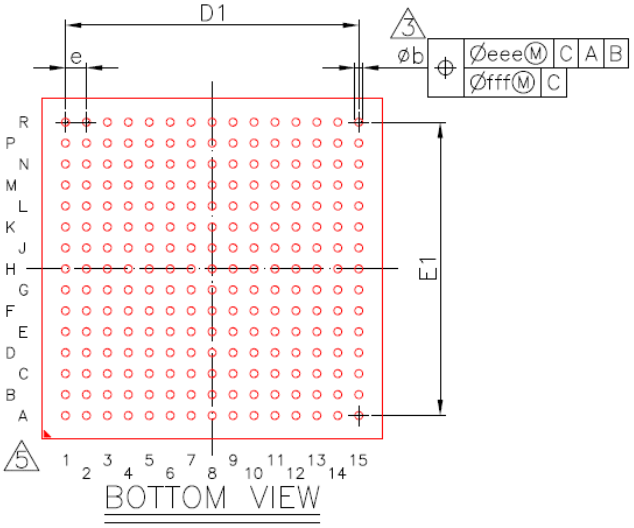
Figure 3.8-33: SPI MDRLD Trigger LDAC Gap and Width Timing

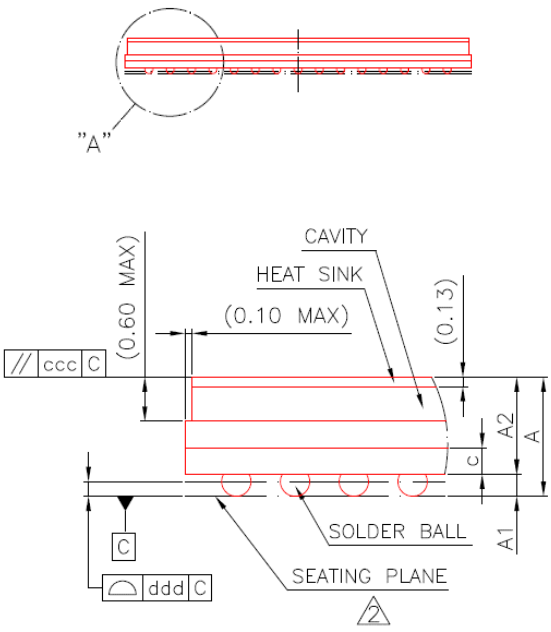
Symbol	Description	Min	Typ	Max	Units
Clock					
T_{SCLK}	MSCLK Period	-	T_{SCLKH} + T_{SCLKL}	-	ns
T_{SCLKH}	MSCLK high	-	5 * Divide	-	ns
T_{SCLKL}	MSCLK low	-	5 * Divide	-	ns
Bus Timing					
T_{DBS1}	MSS[x] to MSCLK (Mode0/1 without DBS1K)	-	(DBS + 1) * Tsclk	-	ns
	MSS[x] to MSCLK (Mode2/3 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	MSS[x] to MSCLK (Mode0/1 with DBS1K)	-	((1024 * (DBS + 1)) + 1) * Tsclk	-	ns
	MSS[x] to MSCLK (Mode2/3 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
T_{DBS2}	Byte to byte (Mode0/1 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	Byte to byte (Mode2/3 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	Byte to byte (Mode0/1 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
	Byte to byte (Mode2/3 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
T_{DBS3}	MSCLK to MSS[x] (Mode0/1 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	MSCLK to MSS[x] (Mode2/3 without DBS1K)	-	(DBS + 1.0) * Tsclk	-	ns
	MSCLK to MSS[x] (Mode0/1 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
	MSCLK to MSS[x] (Mode2/3 with DBS1K)	-	((1024 * (DBS + 1)) + 1.0) * Tsclk	-	ns
T_{DT1}	MSS[x] gap (without DT1K)	-	(DT + 2) * Tsclk	-	ns
	MSS[x] gap (with DT1K)	-	(1024 * (DT + 1) + 2) * Tsclk	-	ns
T_{MISET}	MMISO setup time	10.5	-	-	ns
T_{MIHD}	MMISO hold time	0	-	-	ns
T_{MODLY}	MMOSI output delay	-	-	0.5	ns
T_{RT}	MDRLD ready timeout (RDY mode)	-	(1 + SPIRPT) * 1024 * Tsclk	-	ns
T_{PT}	MTRG timeout	-	(1 + SPIRPT) * 1024 * Tsclk	-	ns
T_{LDACG}	MDRLD Gap (LDAC mode)	-	((LDACG1K * 1023) + 1) * (LDGAP + 1) * Tsclk	-	ns
T_{LDACW}	MDRLD Width (LDAC mode)	-	(LDACG1K * 1023 + 1) * (LDWID + 1) * Tsclk	-	ns

Table 3.8-15: SPI Master Timing Table

4 Package Information







Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.23	1.30	1.37	0.048	0.051	0.054
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	1.04	1.09	1.14	0.041	0.043	0.045
c	0.22	0.26	0.30	0.009	0.010	0.012
D	12.90	13.00	13.10	0.508	0.512	0.516
E	12.90	13.00	13.10	0.508	0.512	0.516
D1	---	11.20	---	---	0.441	---
E1	---	11.20	---	---	0.441	---
e	---	0.80	---	---	0.031	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
ccc	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	15/15					

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: ccc, ddd.
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

5 Ordering Information

Part Number	Description
AX58400 BI	225LD EHS-TFBGA RoHS compliant package, temperature range: -40 to 85˚C.

6 Revision History

Revision	Date	Comments
V0.10	2021/07/26	Preliminary release.
V1.00	2022/10/13	Modified some description in Section 3.8.5
V1.01	2022/12/29	1.Modified some description in Section 1.4.3 2.Corrected Pinout Diagram color in Figure 1.3-1
V1.02	2023/03/17	1.Modified some description in Section 2.45.4.1 2.Corrected Table 2.45-1.
V1.03	2024/11/26	Removed ESC Sub-system's register 0x518 description in Section 2.45.5.1
V1.04	2024/12/03	Modified T_{SCLK} information in Table 3.8-7 and 3.8-9

ASIX Electronics Corporation

4F, No.8, Hsin Ann RD., Hsinchu Science Park,
Hsinchu, Taiwan, R.O.C.

TEL: +886-3-5799500
FAX: +886-3-5799558

Email: support@asix.com.tw
Web: https://www.asix.com.tw