

Silicon Carbide Enhancement Mode MOSFET

Features

- Optimized package with separate driver source pin
- 8 mm of creepage distance between drain and source
- · High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Qrr)

Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Solar inverters
- EV motor drive
- EHigh voltage DC/DC converters
- Switched mode power supplies
- Load switch

S (3)

Preliminary



Package Dimensions



(Tc = 25°C unless otherwise specified)

Parameter		Symbol Ratings		Unit
Drain-Source Voltage	V _{GS} =0V I⊳=100µA	V _{DS}	1200	v
Gate-Source Voltage		V _{GS}	-4/+15	v
Drain Current-Continuous	@ T _c =25°C @ T _c =100°C	ID	115 85	А
Pulse Drain Current		I _{D,pulse}	250	Α
Power Dissipation	@ T _c =25°C @ T _J =175°C	P _D	556	w
Storage Temperature Range	T _{stg}	-55 to +175	°C	
Operating Junction Tempera	TJ	-55 to +175	°C	
Thermal Resistance, Junctio	$R heta_{Jc}$	Тур. 0.30	°C/W	
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Symbol	Dimensions in millimeters					
Symbol	Min.	Avg.	Max.			
Α	4.80	5.00	5.20			
A1	2.21	2.41	2.61			
A2	1.80	2.00	2.20			
b	1.06	1.21	1.36			
b1	2.33	2.63	2.93			
b2	1.07	1.30	1.60			
С	0.51	0.61	0.75			
D	23.30	23.45	23.60			
E	15.74	15.94	16.14			
е	2.54 BSC					
e1	5.08 BSC					
L	17.27	17.57	17.87			
L1	3.99	4.19	4.39			
Q	5.49	5.79	6.09			
Т	2.35	2.50	2.65			



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Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit					
OFF Characteristics											
Drain-Source Breakdown Voltage	BV _{DSS}	$V_{GS}=0V$, $I_{DS}=0.1mA$	1200	-	-	v					
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} =0V · V _{DS} =1200V	-	1	50	μA					
Gate-Source Leakage Current	I _{GSS}	V _{GS} =15V , V _{DS} =0V	-	10	250	nA					
ON Characteristics											
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS} + I_{DS} = 23mA$	1.8	2.5	3.6	v					
Drain-Source On-State Resistance	R _{DS(on)}	V_{GS} =15V , I_{DS} =75A	11.2	16	22.3	mΩ					
Transconductance	g _{fs}	V _{DS} =20V • I _{DS} =75A	-	53	-	S					
Dynamic Characteristics											
Input Capacitance	C _{iss}	V _{DS} =1000V	-	6085	-	pF					
Output Capacitance	C _{oss}	V _{GS} =0V V =25mV	-	230	-						
Reverse Transfer Capacitance	C _{rss}	Freq.=1MHz	-	13	-						
C _{oss} Stored Energy	E _{oss}	V _{GS} =0V • V _{DS} =1000V Freq.=1MHz • V _{AC} =25mV	-	130	-	μJ					
Turn-On Switching Energy	Eon	V _{DD} =800V • V _{GS} =-4V/+15V	-	2.3	-	mJ					
Turn-Off Switching Energy	E _{off}	I _D =75A • R _{G(ext)} =2.5Ω L=65.7μH • T」=175°C	-	0.6	-						
Switching Characteristics											
Turn-On Delay Time	t _{d(on)}	V_{DS} =800V V_{GS} =-4/+15V I_{DS} =75A • L=65.7µH $R_{G(ext)}$ =2.5 Ω Timing relative to V _{DS} , Inductive load	-	34	-	ns					
Rise Time	tr		-	33	-						
Turn-Off Delay Time	t _{d(off)}		-	65	-						
Fall Time	t _f		-	13	-						
Total Gate Charge	Qg	V _{DS} =800V	-	211	-	nC					
Gate to Source Charge	Q_{gs}	V _{GS} =-4/+15V	-	67	-						
Gate to Drain Charge	Q _{gd}	I _D =75A	-	61	-						
Body Diode Characteristics				•							
Inverse Diode Forward Voltage	V _{SD}	V _{GS} =-4V • I _{SD} =37.5A T _J =25°C	-	4.6	-	v					
Continuous Diode Forward Current	Is	Vgs=-4V • Tc=25°C	-	-	112	Α					
Reverse Recovery Time	Trr	V _{GS} =-4V	-	30	-	ns					
Reverse Recovery Charge	Qrr	IsD=75A • VDS=800V, di/dt=4000A/US	-	1238	-	nC					
Peak Reverse Recovery Current	Irrm	Tj=175°C	-	64	-	Α					

Electrical Characteristics @ Tc =25°C (unless otherwise specified)



DAC016N120P2

Typical Device Performance



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Fig 13. Body diode characteristic at 175 °C



Fig 15. Capacitance vs. Drain-source voltage (0-200 V)



Fig 17. Output capacitance stored energy







Fig 16. Capacitance vs. Drain-source voltage (0-1200 V)



Fig 18. Gate charge characteristics

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Fig 25. Clamped inductive switching energy vs. $R_{G(ext)}$



Fig 27. Switching times vs. R_{G(ext)}



Fig 26. Clamped inductive switching energy vs. Temperature



Fig 28. Switching times definition



Fig 29. Clamped inductive switching waveform test circuit



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