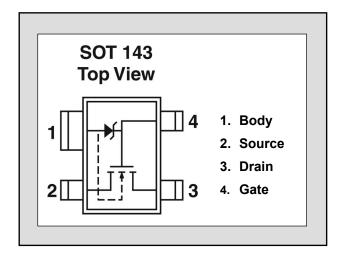


# Linear Integrated Systems

FEATURES	
HIGH SWITCHING SPEED	t <sub>ON</sub> = 2.0ns
LOW ON RESISTANCE	$r_{DS(ON)} = 5\Omega$
LOW GATE NODE CAPACITANCE	C = 25pF
LOW GATE LEAKAGE CAPACITANCE	$I_{G(ON)} = 0.05 \mu A$
ABSOLUTE MAXIMUM RATINGS <sup>1</sup>	
@ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +125 °C
Maximum Power Dissipation	
Continuous Power Dissipation <sup>2</sup>	P <sub>D</sub> = 300mW
Maximum Currents	
Pulsed Drain Current <sup>3</sup>	I <sub>DS</sub> = 1A
Continuous Drain Current <sup>2</sup>	I <sub>DS</sub> = 200mA

# **SST823 SST824**

## **HIGH SPEED N-CHANNEL LATERAL DMOS SWITCH ZENER PROTECTED**



Maximum Voltages								
$V_{DSO}$	Drain to Source		+25V		$V_{SB}$	Source to Body	SST823	+22.5V
V	SDO Source to Drain	SST823	+15V		V SB	Source to Body	SST824	+25V
V SDO		SST824	+20V		$V_{GB}$	Gate to Body		+30V
V <sub>DB</sub> Drain to Body		SST823	+22.5V		$V_{GS}$	Gate to Source		±22.5V
$V_{DB}$	SST	SST824	+30V		$V_{GD}$	Gate to Drain		±22.5V

## ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
$BV_DS$	Breakdown Voltage		25			V	$I_D = 10\mu A, V_{GS} = V_{BS} = 0$
D V DS	Drain to Source		15			V	$I_D = 100 \text{nA}, V_{GS} = V_{BS} = -5 \text{V}$
D) /	Breakdown Voltage	SST823	15			V	I <sub>S</sub> = 100nA. V <sub>GD</sub> = V <sub>BD</sub> = -5V
BV <sub>SD</sub>	Source to Drain	SST824	20			V	IS - 10011A, V <sub>GD</sub> - V <sub>BD</sub> 3V
D\/	Breakdown Voltage	SST823	22.5			V	L = 100nA V = 0 Source Open
BV <sub>DB</sub>	Drain to Body	SST824	25			V	$I_D = 100$ nA, $V_{GB} = 0$ , Source Open
D\/	Breakdown Voltage	SST823	22.5			V	L = 100nA V = 0 Drain Open
BV <sub>SB</sub>	Source to Body	SST824	25			V	$I_S = 100$ nA, $V_{GB} = 0$ , Drain Open
V <sub>GS(OFF)</sub>	Cutoff Voltage Gate to Source		0.1		2	٧	$V_{DS} = V_{GS}, V_{SB} = 0V, I_D = 10\mu A$
F	On Resistance Drain to Source <sup>4</sup>				7.5	Ω	$V_{GS} = 5.0V$ , $I_D = 50mA$ , $V_{SB} = 0$
r <sub>DS(ON)</sub>	On Resistance Drain to Source				5.0	5.0	$V_{GS} = 10V$ , $I_D = 500mA$ , $V_{SB} = 0$
g <sub>fs</sub>	Forward Transconductance <sup>4</sup>		100	120		mmho	$V_{DS} = 15V, I_D = 200mA$
I <sub>D(OFF)</sub>	Leakage Current Drain Node				100	nA	$V_{GS} = V_{BS} = -5V, V_{DS} = 15V$
I <sub>S(OFF)</sub>	Leakage Current Source Node				100	nA	V <sub>GD</sub> = V <sub>BD</sub> = -5V, V <sub>DS</sub> = 15V
I <sub>G(OFF)</sub>	Leakage Current Gate Node (OFF)				100	nA	$V_{GB} = 0V$ , $V_{GS} = V_{GD} = -22.5V$
I <sub>G(ON)</sub>	Leakage Current Gate Node (C	ON)			10	μA	V <sub>GB</sub> = 30V, V <sub>GS</sub> = V <sub>GD</sub> = 22.5V

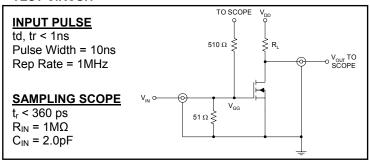
#### **ELECTRICAL CHARACTERISTICS CONT.**

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS	
$C_{(GS+GD+GB)}$	Capacitance Gate Node		25	30	pF		
$C_{(GD+DB)}$	Capacitance Drain Node		13	15	pF	V <sub>DS</sub> = 10V. V <sub>GS</sub> = V <sub>BS</sub> = -15V. f = 1MHz	
C <sub>(GS+SB)</sub>	Capacitance Source Node		35	40	pF	$V_{DS} = 10V$ , $V_{GS} = V_{BS} = -15V$ , $T = 11VIHZ$	
$C_{DG}$	Capacitance Reverse Transfer		3	5	pF		
t <sub>ON</sub>	Turn On Time <sup>5</sup>		2.0	3.0	ns	$V_{DD} = 10V, V_{G(ON)} = 10V,$	
t <sub>OFF</sub>	Turn Off Time <sup>5</sup>		3.0	4.0	ns	$R_L = 133\Omega$ , $R_G = 51\Omega$	

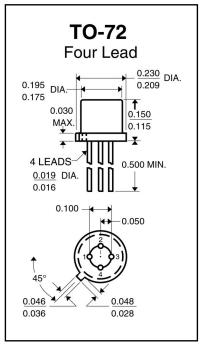
#### **SWITCHING CHARACTERISTICS**

$V_{GG}$	V <sub>DD</sub>	$R_L$	t <sub>d(ON)</sub>	t <sub>r</sub> TYP	t <sub>OFF</sub>
	5V	100Ω	<1ns	1ns	3ns
5V	10V	200Ω	<1ns	1ns	3ns
	20V	300Ω	<1ns	1ns	3ns
10V	5V	67Ω	<1ns	1ns	3ns
	10V	133Ω	<1ns	1ns	3ns
	20V	270Ω	<1ns	1ns	3ns

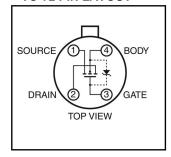
#### **TEST CIRCUIT**



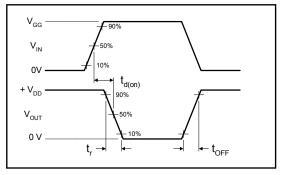
#### **PACKAGE OPTION**



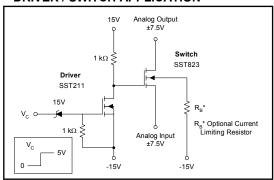
#### **TO-72 PIN LAYOUT**



#### **SWITCHING WAVEFORMS**



#### **DRIVER / SWITCH APPLICATION**



### **NOTES**

- Absolute maximum ratings are limiting values above which serviceability may be impaired. 1.
- For SOT143 package only. 2.
- Pulsed @ 80 µs, 1% duty cycle.
- 4. See test conditions in Electrical Characteristics section.
- See Switching Characteristics and Test Circuit for detail.

Information furnished by Linear Integrated Systems is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent o