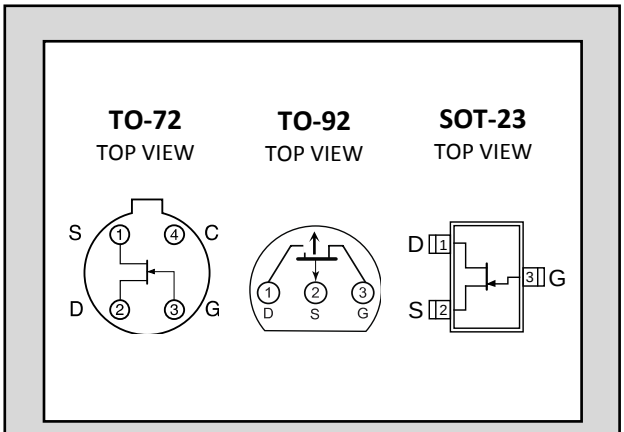
LINEAR SYSTEMS

Twenty-Five Years Of Quality Through Innovation

LS846

LOW NOISE LOW LEAKAGE SINGLE N-CHANNEL JFET AMPLIFIER

FEATURES	
ULTRA LOW NOISE	e_n = 3nV/√Hz
LOW INPUT CAPACITANCE	C_{ISS} = 4pF
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Operating Junction Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation TA=25°C	300mW[3]
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSO} = 60V
Gate to Drain	V_{GDO} = 60V



*For equivalent Monolithic Dual, see LS843 Family

SYMBOL	CHARACTERISTIC[2]	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-60			V	V_{DS} = 0, I_D = 1nA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-1		-3.5	V	V_{DS} = 15V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage	-0.5		-3.5	V	V_{DS} = 15V, I_D = 500µA
I_{DSS}	Drain to Source Saturation Current	1.5	5	15	mA	V_{DS} = 15V, V_{GS} = 0
I_G	Gate Operating Current		-15	-50	pA	V_{DG} = 15V, I_D = 500µA
I_G	Gate Operating Current Reduced V_{DG}		-5	-30	pA	V_{DG} = 3V, I_D = 500µA
I_{GSS}	Gate to Source Leakage Current			-100	pA	V_{GS} = 15V, V_{DS} = 0
G_{fss}	Full Conductance Transconductance	1500			µS	V_{DS} = 15V, V_{GS} = 0, *f* = 1kHz
G_{fs}	Typical Operation Transconductance	1000	1500		µS	V_{DS} = 15V, I_D = 200µA
G_{OSS}	Full Output Conductance			40	µS	V_{DS} = 15V, V_{GS} = 0
G_{OS}	Typical Operation Output Conductance		2.0	2.70	µS	V_{DS} = 15V, I_D = 200µA
NF	Noise Figure			0.5	dB	V_{DS} = 15V, V_{GS} = 0, R_G = 10MΩ, *f* = 100Hz, NBW = 6Hz
e_n	Noise Voltage		3	7	nV/√Hz	V_{DS} = 15V, I_D = 500µA, *f* = 1kHz, NBW = 1Hz
e_n	Noise Voltage			11	nV/√Hz	V_{DS} = 15V, I_D = 500µA, *f* = 10Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance			8	pF	V_{DS} = 15V, I_D = 500µA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.			3	pF	

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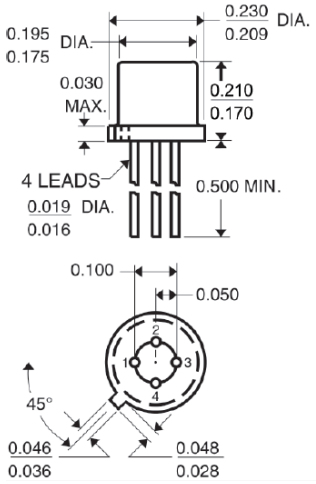
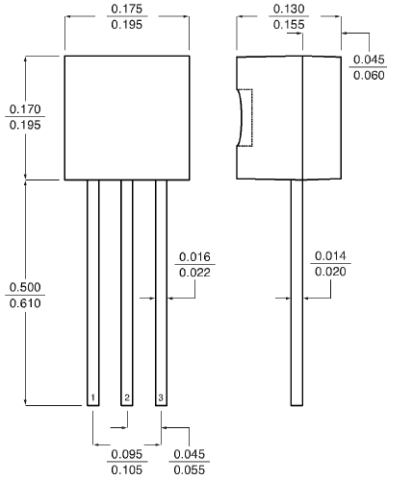
STANDARD PACKAGE DIMENSIONS:

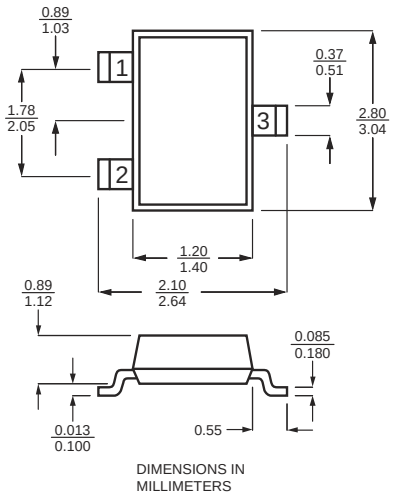
TO-72
Four Lead



TO-92



SOT-23



*Dimensions in inches

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate negative electrical polarity only.
3. Derate 2.8mW/ºC above 25ºC.

Linear Integrated Systems (LIS) is a 25-year-old, third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company President John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, Co-Founder and Vice President of R&D at Intersil, and Founder/President of Micro Power Systems.